Regarding the change of names mentioned in the document, such as Hitachi Electric and Hitachi XX, to Renesas Technology Corp.

The semiconductor operations of Mitsubishi Electric and Hitachi were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Hitachi, Hitachi, Ltd., Hitachi Semiconductors, and other Hitachi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Renesas Technology Home Page: http://www.renesas.com

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Cautions

Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corporation product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corporation or a third party.
2. Renesas Technology Corporation assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corporation without notice due to product improvements or other reasons.   It is therefore recommended that customers contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor for the latest product information before purchasing a product listed herein.
The information described here may contain technical inaccuracies or typographical errors.
Renesas Technology Corporation assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
Please also pay attention to information published by Renesas Technology Corporation by various means, including the Renesas Technology Corporation Semiconductor home page (http://www.renesas.com).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products.   Renesas Technology Corporation assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corporation semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake.   Please contact Renesas Technology Corporation or an authorized Renesas Technology Corporation product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corporation is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corporation for further details on these materials or the products contained therein.

HM62V16258B Series

4 M SRAM (256-kword × 16-bit)

Description

The Hitachi HM62V16258B Series is 4-Mbit static RAM organized 262,144-word × 16-bit. HM62V16258B Series has realized higher density, higher performance and low power consumption by employing Hi-CMOS process technology. It offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is packaged in standard 44-pin plastic TSOPII.
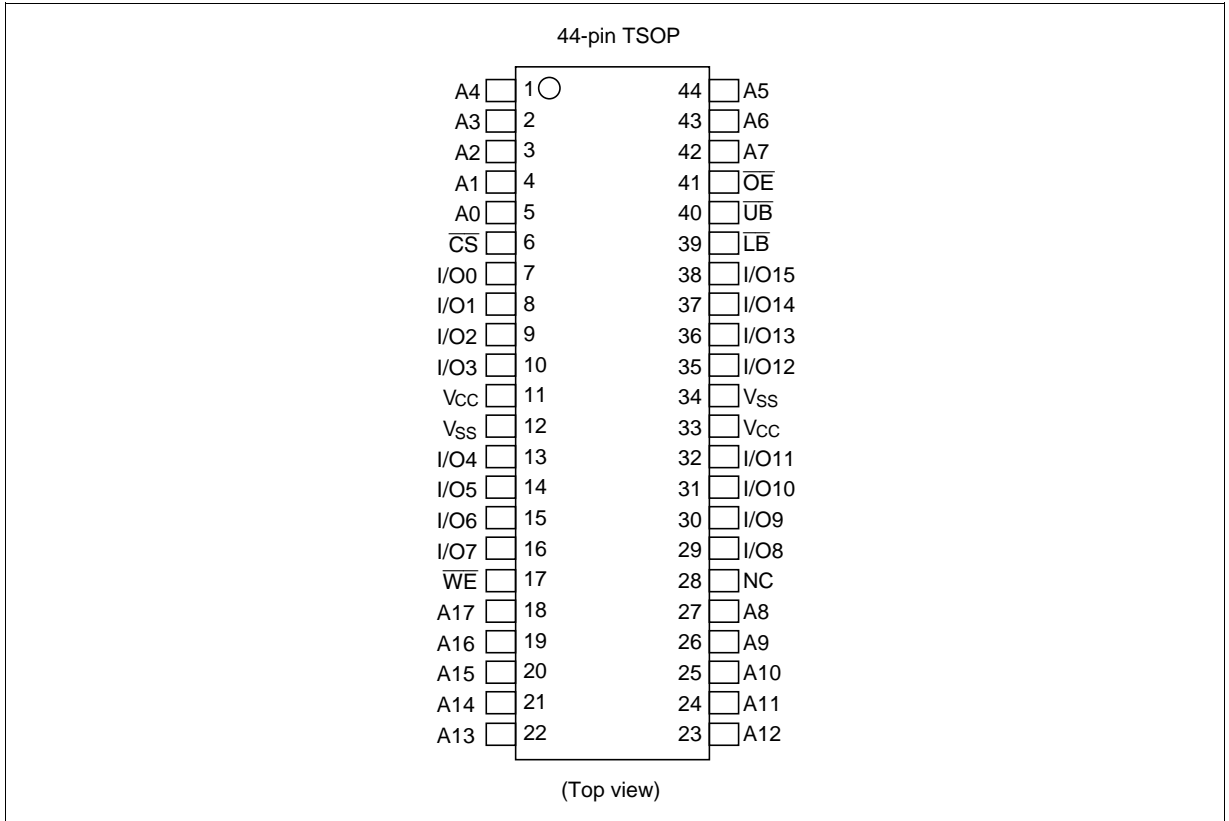
Features

- Single 3.0 V supply: 2.7 V to 3.6 V
- Fast access time: 70 ns/85 ns (max)
- Power dissipation:
    — Active: 9 mW (typ)
    — Standby: 3 μW (typ)
- Completely static memory.
    — No clock or timing strobe required
- Equal access and cycle times
- Common data input and output.
    — Three state output
- Battery backup operation.

Ordering Information

| Type No.	Access time	Package
HM62V16258BLTT-7	70 ns	400-mil 44-pin plastic TSOPII (normal-bend type) (TTP-44DB)
HM62V16258BLTT-8	85 ns	
HM62V16258BLTT-7SL	70 ns	
HM62V16258BLTT-8SL	85 ns	

Pin Arrangement

44-pin TSOP

A4	1 ○	44	A5
A3	2	43	A6
A2	3	42	A7
A1	4	41	$\overline{OE}$
A0	5	40	$\overline{UB}$
$\overline{CS}$	6	39	$\overline{LB}$
I/O0	7	38	I/O15
I/O1	8	37	I/O14
I/O2	9	36	I/O13
I/O3	10	35	I/O12
Vcc	11	34	Vss
Vss	12	33	Vcc
I/O4	13	32	I/O11
I/O5	14	31	I/O10
I/O6	15	30	I/O9
I/O7	16	29	I/O8
$\overline{WE}$	17	28	NC
A17	18	27	A8
A16	19	26	A9
A15	20	25	A10
A14	21	24	A11
A13	22	23	A12

(Top view)

Pin Description

Pin name	Function
A0 to A17	Address input
I/O0 to I/O15	Data input/output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
$\overline{LB}$	Lower byte select
$\overline{UB}$	Upper byte select
V_{cc}	Power supply
V_{ss}	Ground
NC	No connection

RENESAS

Block Diagram
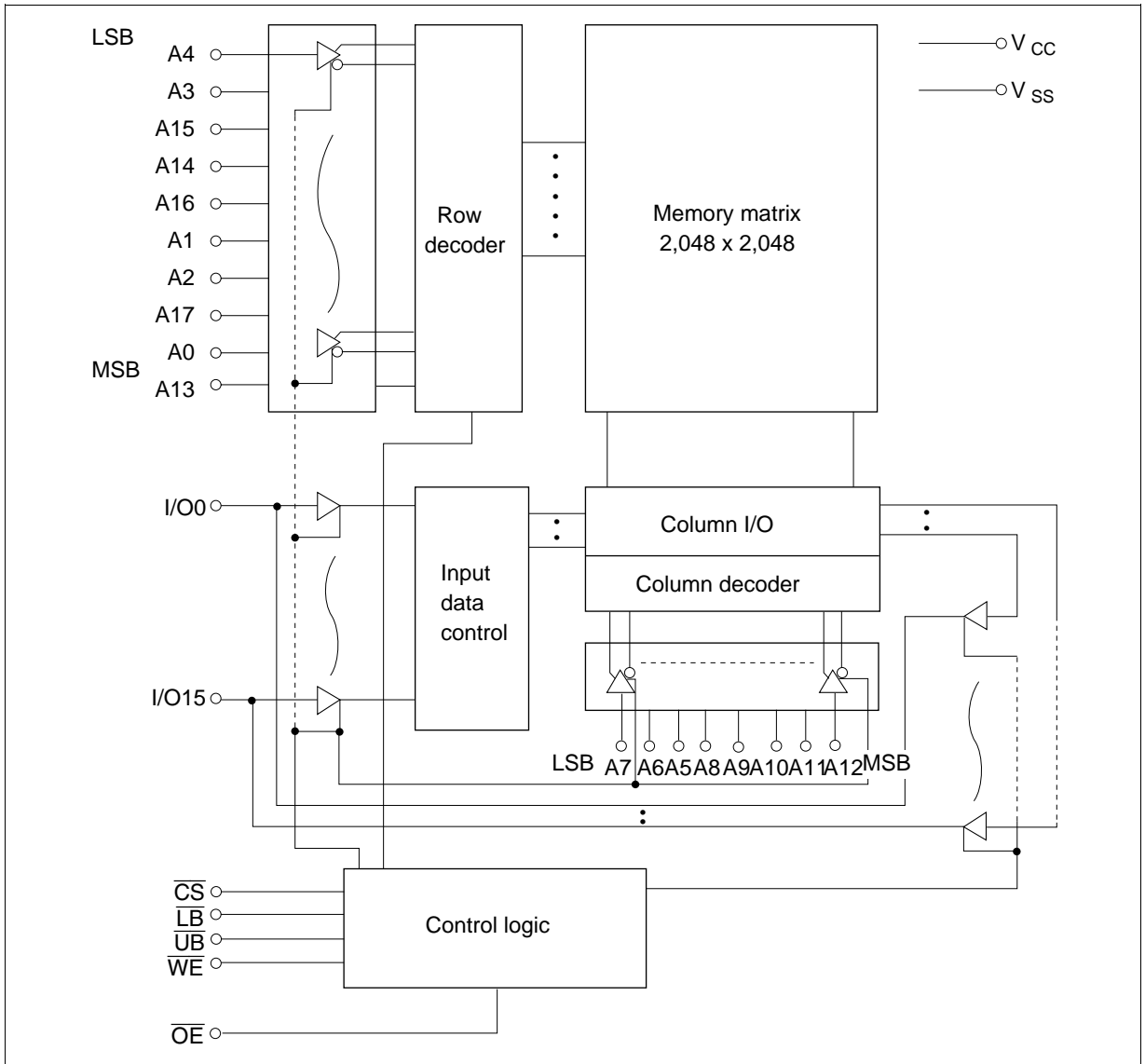
Operation Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	I/O0 to I/O7	I/O8 to I/O15	Operation
H	×	×	×	×	High-Z	High-Z	Standby
×	×	×	H	H	High-Z	High-Z	Standby
L	H	L	L	L	Dout	Dout	Read
L	H	L	H	L	Dout	High-Z	Lower byte read
L	H	L	L	H	High-Z	Dout	Upper byte read
L	L	×	L	L	Din	Din	Write
L	L	×	H	L	Din	High-Z	Lower byte write
L	L	×	L	H	High-Z	Din	Upper byte write
L	H	H	×	×	High-Z	High-Z	Output disable

Note: H: V_{IH}, L: V_{IL}, ×: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage relative to V_{ss}	V_{CC}	−0.5 to + 4.6	V
Terminal voltage on any pin relative to V_{ss}	V_T	−0.5[*1] to V_{CC} + 0.3[*2]	V
Power dissipation	P_T	1.0	W
Storage temperature range	Tstg	−55 to +125	°C
Storage temperature range under bias	Tbias	−10 to +85	°C

Notes: 1. V_T min: −3.0 V for pulse half-width ≤ 30 ns.
2. Maximum voltage is +4.6 V.

DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{CC}	2.7	3.0	3.6	V	
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V	
Input low voltage	V_{IL}	−0.3	—	0.6	V	1
Ambient temperature range	Ta	0	—	70	°C	

Note: 1. V_{IL} min: −3.0 V for pulse half-width ≤ 30 ns.

DC Characteristics

Parameter		Symbol	Min	Typ*1	Max	Unit	Test conditions
Input leakage current		$|I_{LI}|$	—	—	1	μA	Vin = V_{SS} to V_{CC}
Output leakage current		$|I_{LO}|$	—	—	1	μA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} or, $\overline{LB}$ = $\overline{UB}$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating current		I_{CC}	—	—	20	mA	$\overline{CS}$ = V_{IL}, Others = V_{IH}/V_{IL}, $I_{I/O}$ = 0 mA
Average operating current	HM62V16258B-7	I_{CC1}	—	—	70	mA	Min. cycle, duty = 100%, $I_{I/O}$ = 0 mA, $\overline{CS}$ = V_{IL}, Others = V_{IH}/V_{IL}
	HM62V16258B-8	I_{CC1}	—	—	65	mA	
		I_{CC2}	—	3	15	mA	Cycle time = 1 μs, duty = 100%, $I_{I/O}$ = 0 mA, $\overline{CS} \leq 0.2$ V, $V_{IH} \geq V_{CC} - 0.2$ V, $V_{IL} \leq 0.2$ V
Standby current		I_{SB}	—	—	0.3	mA	$\overline{CS}$ = V_{IH}
Standby current		I_{SB1}*2	—	1	40	μA	0 V ≤ Vin $\overline{CS} \geq V_{CC} - 0.2$ V
		I_{SB1}*3	—	1	20	μA	
Output high voltage		V_{OH}	2.4	—	—	V	I_{OH} = −1 mA
			$V_{CC} - 0.2$	—	—	V	I_{OH} = −100 μA
Output low voltage		V_{OL}	—	—	0.4	V	I_{OL} = 2 mA
			—	—	0.2	V	I_{OL} = 100 μA

Notes: 1. Typical values are at V_{CC} = 3.0 V, Ta = +25°C and not guaranteed.
2. This characteristic is guaranteed only for L version.
3. This characteristic is guaranteed only for L-SL version.

Capacitance (Ta = +25°C, f = 1.0 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Input capacitance	Cin	—	—	8	pF	Vin = 0 V	1
Input/output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0 V	1

Note: 1. This parameter is sampled and not 100% tested.

RENESAS

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 2.7 V to 3.6 V, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{IL} = 0.4 V, V_{IH} = 2.2 V
- Input rise and fall time: 5 ns
- Input timing reference levels: 1.4 V
- Output timing reference levels: 1.4 V
- Output load: 1 TTL + 30 pF (HM62V16258B-7) (Including scope and jig)
              1 TTL + 100 pF (HM62V16258B-8) (Including scope and jig)

Read Cycle

| Parameter | Symbol | HM62V16258B | | | | Unit | Notes |
		-7		-8			
		Min	Max	Min	Max		
Read cycle time	t_{RC}	70	—	85	—	ns	
Address access time	t_{AA}	—	70	—	85	ns	
Chip select access time	t_{ACS}	—	70	—	85	ns	
Output enable to output valid	t_{OE}	—	40	—	45	ns	
Output hold from address change	t_{OH}	10	—	10	—	ns	
$\overline{LB}$, $\overline{UB}$ access time	t_{BA}	—	70	—	85	ns	
Chip select to output in low-Z	t_{CLZ}	10	—	10	—	ns	2, 3
$\overline{LB}$, $\overline{UB}$ enable to low-z	t_{BLZ}	5	—	5	—	ns	2, 3
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	ns	2, 3
Chip deselect to output in high-Z	t_{CHZ}	0	25	0	25	ns	1, 2, 3
$\overline{LB}$, $\overline{UB}$ disable to high-Z	t_{BHZ}	0	25	0	25	ns	1, 2, 3
Output disable to output in high-Z	t_{OHZ}	0	25	0	25	ns	1, 2, 3

RENESAS

Write Cycle

| Parameter | Symbol | HM62V16258B | | | | Unit | Notes |
| | | -7 | | -8 | | | |
		Min	Max	Min	Max		
Write cycle time	t_{WC}	70	—	85	—	ns	
Address valid to end of write	t_{AW}	60	—	70	—	ns	
Chip selection to end of write	t_{CW}	60	—	70	—	ns	5
Write pulse width	t_{WP}	50	—	55	—	ns	4
$\overline{LB}$, $\overline{UB}$ valid to end of write	t_{BW}	55	—	70	—	ns	
Address setup time	t_{AS}	0	—	0	—	ns	6
Write recovery time	t_{WR}	0	—	0	—	ns	7
Data to write time overlap	t_{DW}	30	—	35	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	ns	
Output active from end of write	t_{OW}	5	—	5	—	ns	2
Output disable to output in High-Z	t_{OHZ}	0	25	0	25	ns	1, 2
Write to output in high-Z	t_{WHZ}	0	25	0	25	ns	1, 2

Notes: 1. t_{CHZ}, t_{OHZ}, t_{WHZ} and t_{BHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.

2. This parameter is sampled and not 100% tested.

3. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.

4. A write occures during the overlap of a low $\overline{CS}$, a low $\overline{WE}$ and a low $\overline{LB}$ or a low $\overline{UB}$. A write begins at the latest transition among $\overline{CS}$ going low, $\overline{WE}$ going low and $\overline{LB}$ going low or $\overline{UB}$ going low. A write ends at the earliest transition among $\overline{CS}$ going high, $\overline{WE}$ going high and $\overline{LB}$ going high or $\overline{UB}$ going high. t_{WP} is measured from the beginning of write to the end of write.

5. t_{CW} is measured from the later of $\overline{CS}$ going low to the end of write.

6. t_{AS} is measured from the address valid to the beginning of write.

7. t_{WR} is measured from the earliest of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
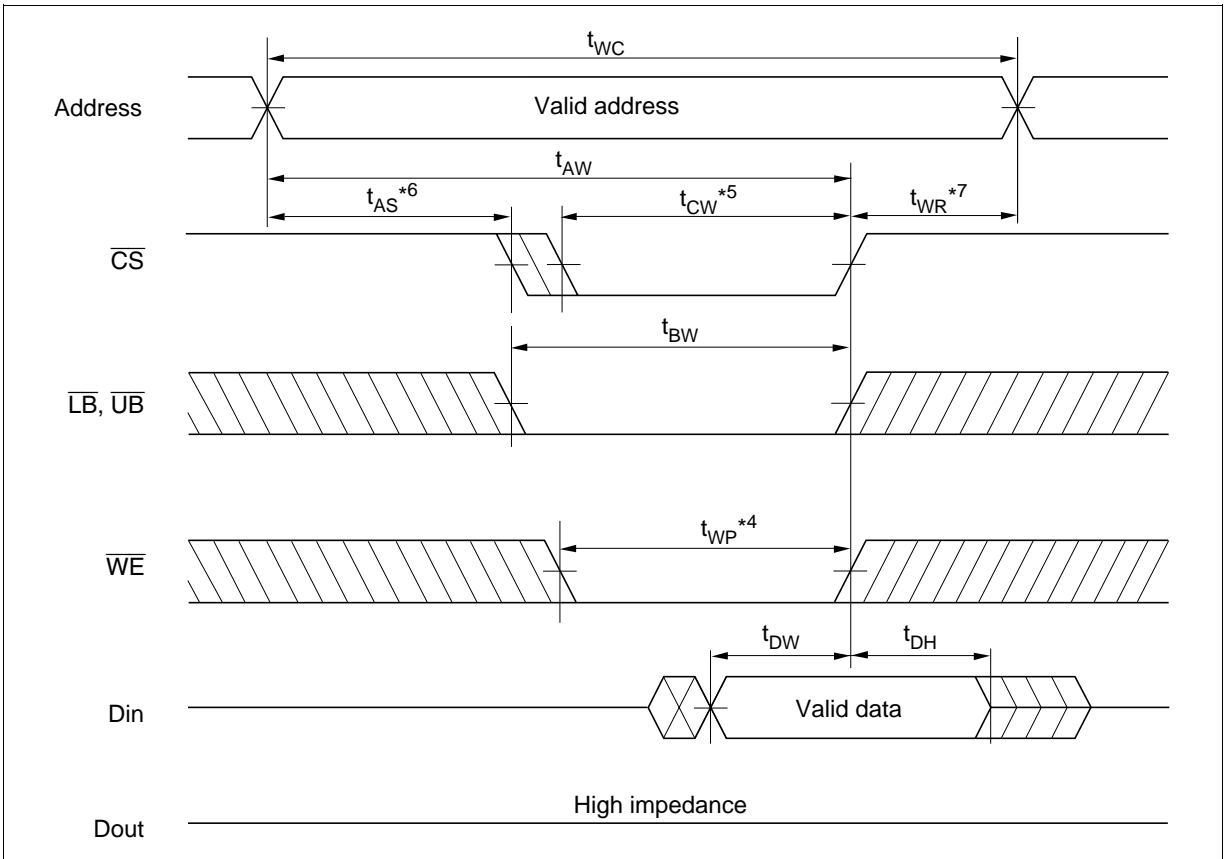
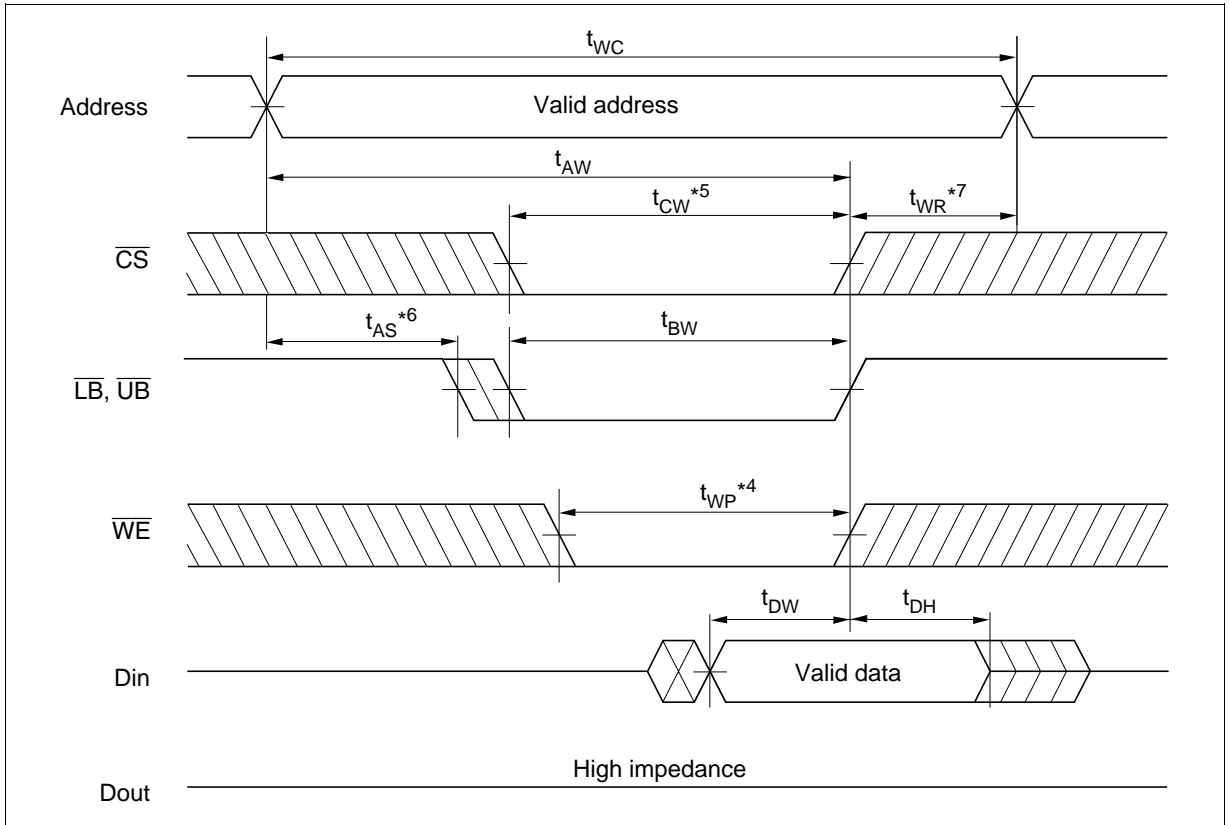RENESAS

Timing Waveform

Read Cycle
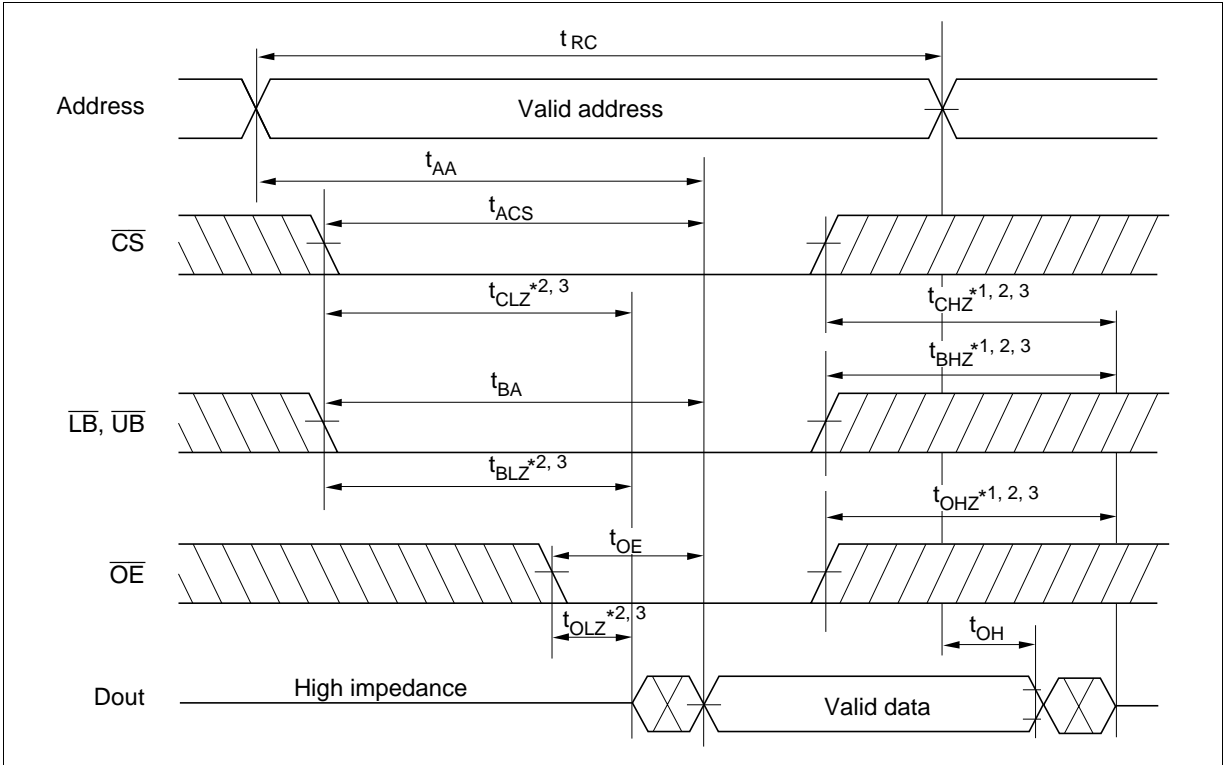
Write Cycle (1) ($\overline{\text{WE}}$ Clock)
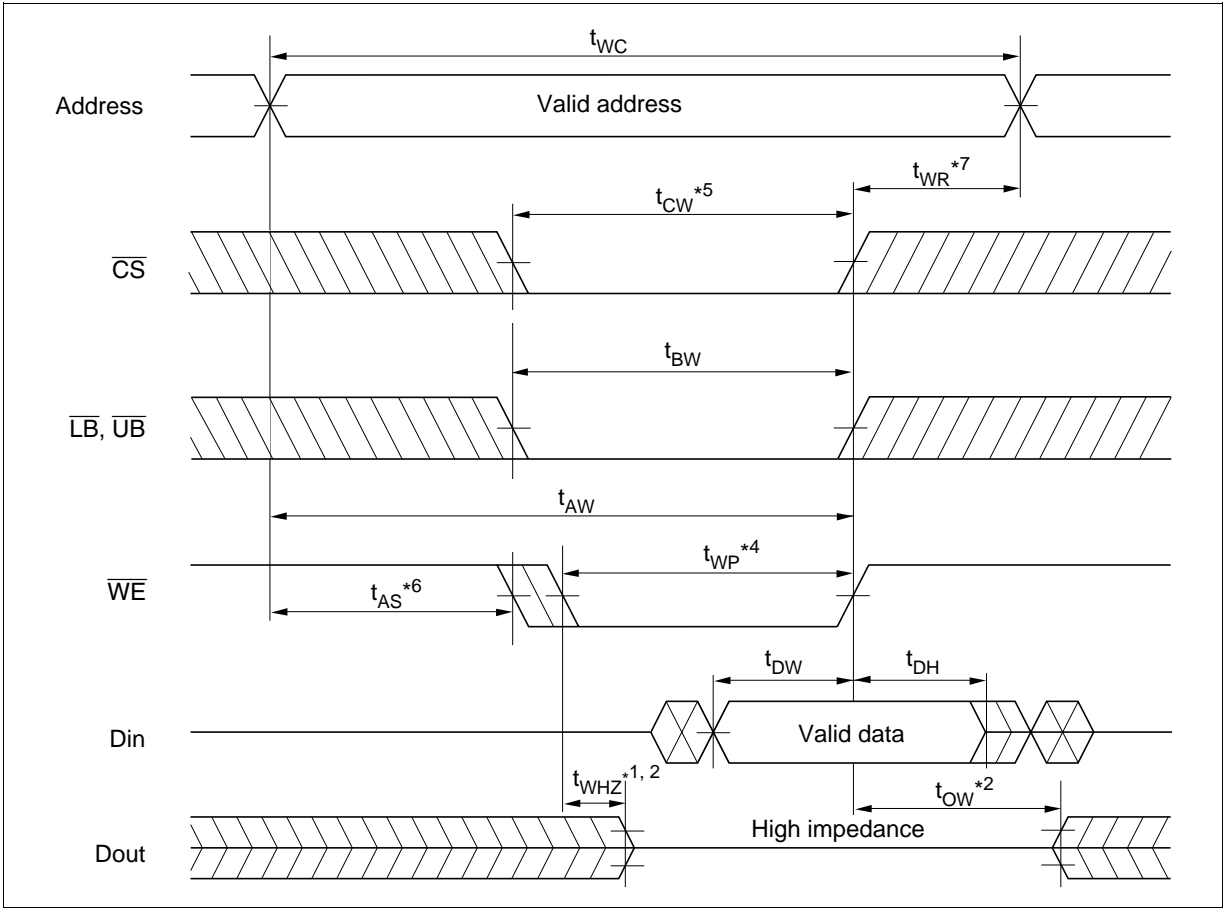
Write Cycle (2) ($\overline{\text{CS}}$ Clock, $\overline{\text{OE}} = V_{IH}$)

Write Cycle (3) ($\overline{\text{LB}}$, $\overline{\text{UB}}$ Clock, $\overline{\text{OE}} = V_{\text{IH}}$)

RENESAS

Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ[4]	Max	Unit	Test conditions[3]
V_{CC} for data retention	V_{DR}	2.0	—	—	V	Vin ≥ 0V (1) $\overline{CS} \geq V_{CC}$ – 0.2 V or (2) $\overline{LB} = \overline{UB} \geq V_{CC}$ – 0.2 V $\overline{CS} \leq$ 0.2 V
Data retention current	I_{CCDR} [1]	—	0.8	20	μA	V_{CC} = 3.0 V, Vin ≥ 0V (1) $\overline{CS} \geq V_{CC}$ – 0.2 V or (2) $\overline{LB} = \overline{UB} \geq V_{CC}$ – 0.2 V $\overline{CS} \leq$ 0.2 V
	I_{CCDR} [2]	—	0.8	10	μA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC} [5]	—	—	ns	

Notes: 1. This characteristic is guaranteed only for L-version, 10 μA max. at Ta = 0 to +40°C.

2. This characteristic is guaranteed only for L-SL version, 5 μA max. at Ta = 0 to +40°C.

3. $\overline{CS}$ controls address buffer, $\overline{WE}$ buffer, $\overline{OE}$ buffer, $\overline{LB}$, $\overline{UB}$ buffer and Din buffer. If $\overline{CS}$ controls data retention mode, Vin levels (address, $\overline{WE}$, $\overline{OE}$, $\overline{LB}$, $\overline{UB}$, I/O) can be in the high impedance state. If $\overline{LB}$, $\overline{UB}$ controls data retention mode, $\overline{LB}$, $\overline{UB}$ must be $\overline{LB} = \overline{UB} \geq V_{CC}$ – 0.2 V, $\overline{CS}$ must be $\overline{CS} \leq$ 0.2 V. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

4. Typical values are at V_{CC} = 3.0 V, Ta = +25°C and not guaranteed.

5. t_{RC} = read cycle time.

RENESAS

Low V$_{CC}$ Data Retention Timing Waveform (1) ($\overline{CS}$ Controlled)

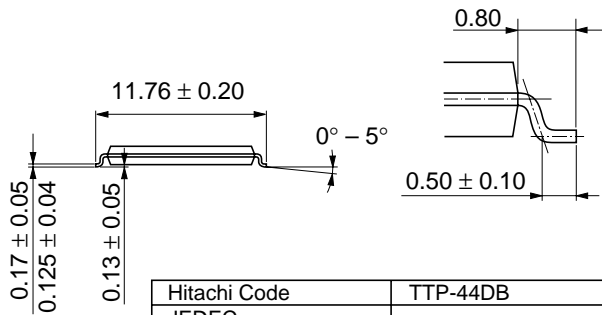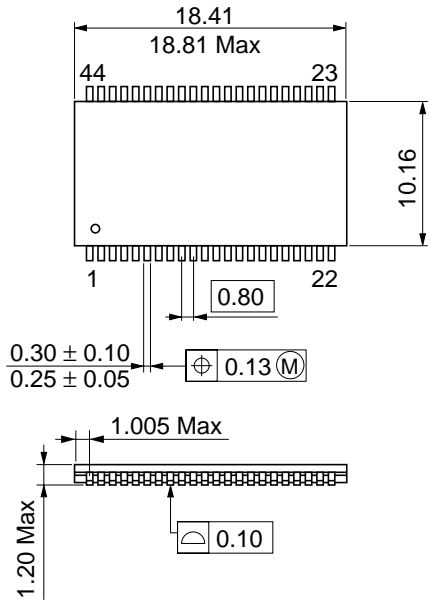Data retention mode

t$_{CDR}$ ... t$_R$

V$_{CC}$
2.7 V

V$_{DR}$
2.0 V

$\overline{CS}$
0 V

$\overline{CS} \geq V_{CC} - 0.2$ V
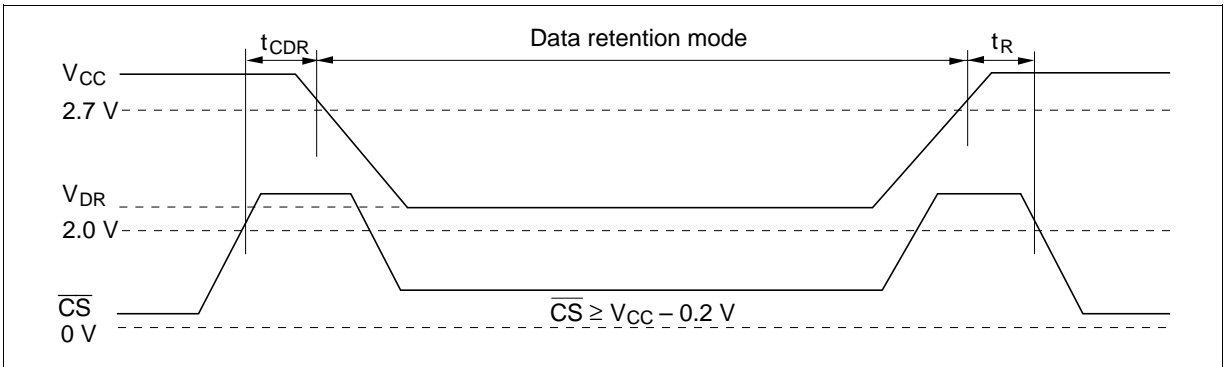
Low V$_{CC}$ Data Retention Timing Waveform (2) ($\overline{LB}$, $\overline{UB}$ Controlled)

Data retention mode

t$_{CDR}$ ... t$_R$

V$_{CC}$
2.7 V

V$_{DR}$
2.0 V

$\overline{LB}$, $\overline{UB}$
0 V

$\overline{LB}$, $\overline{UB} \geq V_{CC} - 0.2$ V

RENESAS
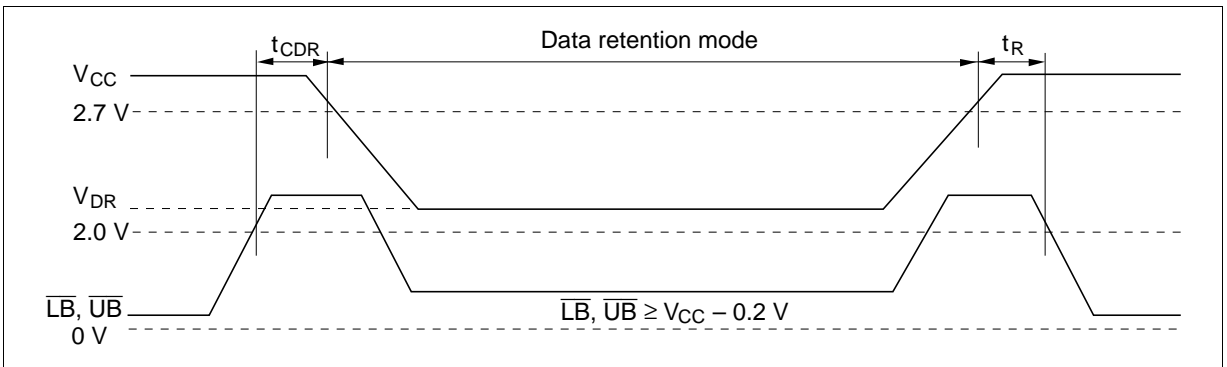
Package Dimensions

HM62V16258BLTT Series (TTP-44DB)

Unit: mm

18.41
18.81 Max

44   23

1   22

10.16

0.80

0.30 ± 0.10
0.25 ± 0.05

⊕ 0.13 Ⓜ

1.005 Max

1.20 Max

▱ 0.10

11.76 ± 0.20

0° − 5°

0.17 ± 0.05
0.125 ± 0.04

0.13 ± 0.05

0.80

0.50 ± 0.10

Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-44DB
JEDEC	—
EIAJ	—
Weight (reference value)	0.43 g

RENESAS

Cautions

1. Hitachi neither warrants nor grants licenses of any rights of Hitachi's or any third party's patent, copyright, trademark, or other intellectual property rights for information contained in this document. Hitachi bears no responsibility for problems that may arise with third party's rights, including intellectual property rights, in connection with use of the information contained in this document.

2. Products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.

3. Hitachi makes every attempt to ensure that its products are of high quality and reliability. However, contact Hitachi's sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.

4. Design your application so that the product is used within the ranges guaranteed by Hitachi particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. Hitachi bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safes, so that the equipment incorporating Hitachi product does not cause bodily injury, fire or other consequential damage due to operation of the Hitachi product.

5. This product is not designed to be radiation resistant.

6. No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without written approval from Hitachi.

7. Contact Hitachi's sales office for any questions regarding this document or Hitachi semiconductor products.

HITACHI

RENESAS