To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

M32172F2VFP
M32173F2VFP

SINGLE-CHIP 32-BIT CMOS MICROCOMPUTER

Description

The M32172F2VFP and M32173F2VFP are 32-bit single-chip RISC microcomputers designed for use in high-reliability vehicle mounted, general industrial, and household equipment. These microcomputers especially are suitable for equipment that requires motor control and communication functions.

For these purposes of use, the microcomputer contains various peripheral functions ranging from 16-channel output related and 18-channel input related timers, two independent channels of A-D and D-A converters, 2-channel Full CANs, and 8-channel serial I/Os. Also included are 10-channel DMAs, 1-channel real-time debugger, and JTAG(boundary scan function). With lower power consumption and low noise characteristics also considered, these microcomputers are ideal for embedded equipment applications.

Features

M32R RISC CPU core

- Uses the M32R family RISC CPU core (Instruction set common to all microcomputers in the M32R family)
- Five-stage pipelined processing
- Sixteen 32-bit general-purpose registers
- 16-bit/32-bit instructions implemented
- DSP function instructions (sum-of-products calculation using 56-bit accumulator)
- Built-in flash memory 256KB
- Built-in flash programming boot program
- Built-in RAM M32172F2VFP 16KB
  M32173F2VFP 32KB
- PLL clock generating circuit ..... Built-in x4 PLL circuit
- Maximum operating frequency of the CPU clock
  40MHz(when operating at -40 to +85 °C)
  32MHz(when operating at -40 to +125 °C)

34-channel input/output related timers

The microcomputer incorporates output related timers capable of 2-channel three-phase motor control and input related timers that can interface the microcomputer to position/phase sensors.

- 16-bit output related timers 16ch
- 16-bit input related timers 14ch
- 32-bit input related timers 4ch

- The internal DMAC and A-D converter can be started by a timer.
- Can be interfaced to two channels of PD (Phase Digital) sensors by using eight channels of input related timers.
- The two channels of input related timers have a pulse encoder function allowing the microcomputer to be interfaced to two channels of position/phase sensors.

Real-time Debugger

- Includes dedicated clock-synchronized serial I/O that can read and write the contents of the internal RAM independently of the CPU.
- Can look up and update the data table in real time while the program is running.
- Can generate a dedicated interrupt based on RTD communication.

Abundant internal peripheral functions

In addition to the timers and real-time debugger, the microcomputer contains the following peripheral functions.

- Position/phase sensor interface circuit ..... 2 channels
- DMAC ..... 10 channels
- A-D converter ..... 10-bit converter x 8 channels
  10-bit converter x 4 channels
- D-A converter ..... 8-bit converter x 2 channels
- Serial I/O ..... 8 channels
- Interrupt controller: 32 interrupt sources, 8 priority levels
- Wait controller
- Full CAN ..... 2 channels
- JTAG (boundary scan function, Mitsubishi original SDI debug function)

Note: SDI is the acronym of Scalable Debug Interface

Designed to operate at high temperatures

To meet the need for use at high temperatures, the microcomputer is designed to be able to operate in the temperature range of –40 to +125°C when CPU clock operating frequency = 32 MHz. When CPU clock operating frequency = 40 MHz, the microcomputer can be used in the temperature range of –40 to +85°C.

Note: This does not guarantee continuous operation at 125°C. If you are considering use of the microcomputer at 125°C, please consult Mitsubishi.

Applications

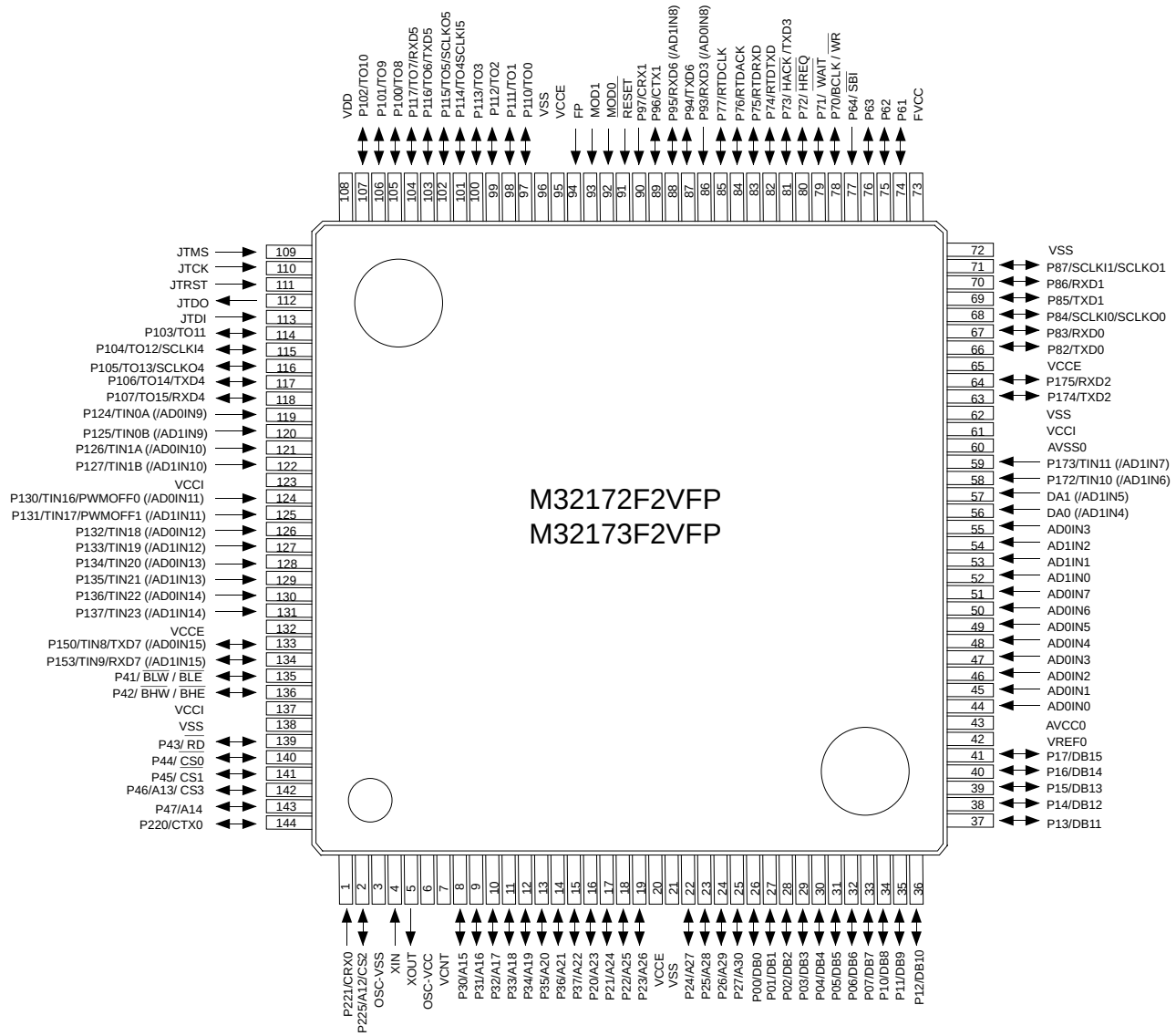
Automobile equipment control (e.g., EV, HEV, and EPS), industrial equipment system control, and high-function OA equipment (e.g., PPC)

Note : The microcomputers presented here are under development and, therefore, are subject to change of specifications, etc.

M32172F2VFP
M32173F2VFP

SINGLE-CHIP 32-BIT CMOS MICROCOMPUTER

Pin Assignment(top view)



Package 144P6Q-A

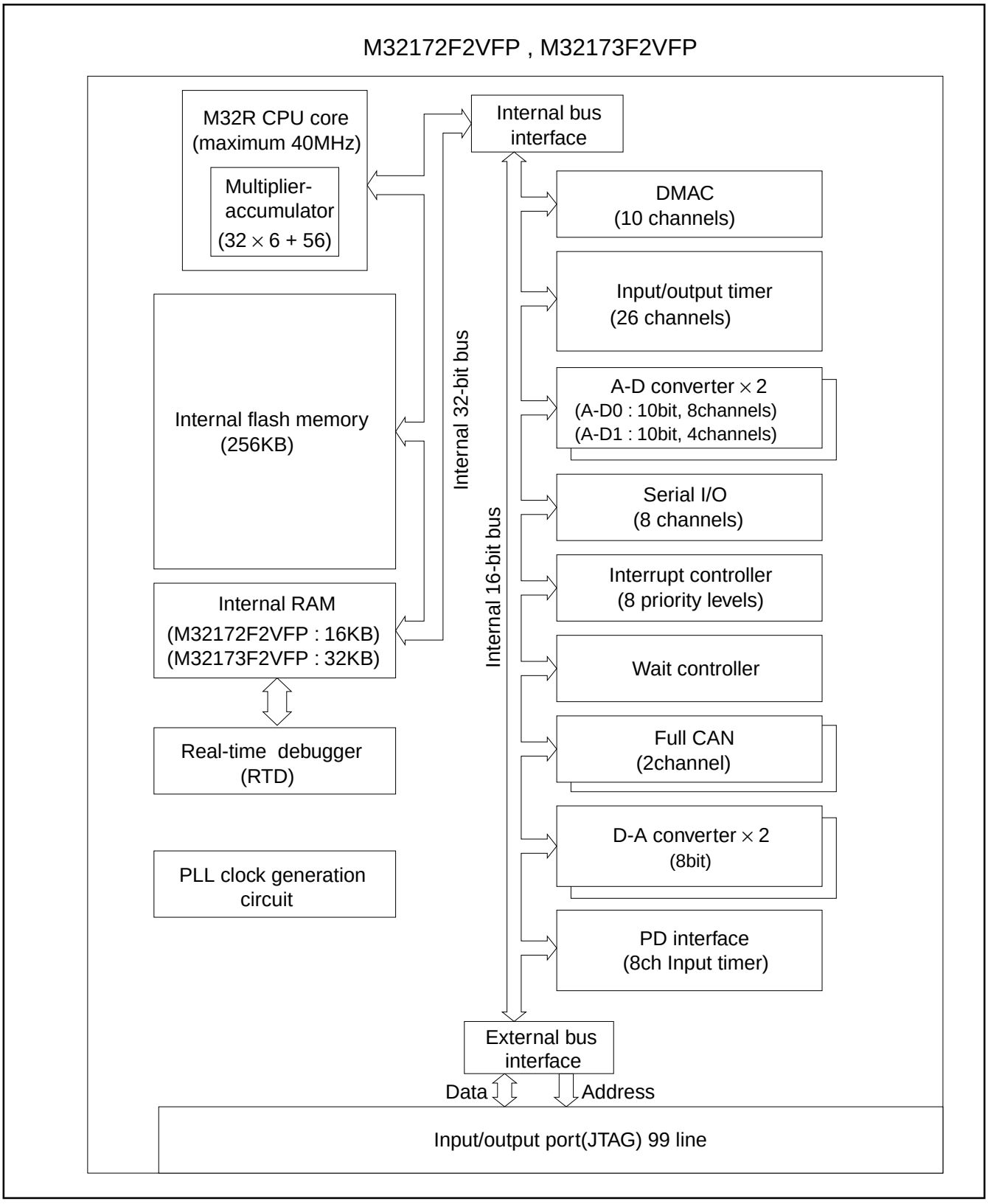


Fig.1 Block diagram

Table 1 Outline Performance (1/2)

Functional Block	Features
M32R CPU core	M32R family CPU core, internally configured in 32 bits Built-in multiplier-accumulator (32 × 16 + 56) Basic bus cycle : 25 ns (CPU clock frequency at 40 MHz, Internal peripheral clock frequency at 20 MHz) Logical address space : 4G bytes, linear General-purpose register : 32-bit register × 16,Control register: 32-bit register × 5 accumulator : 56 bits
External data bus	16 bits data bus
Instruction set	16-bit/32-bit instruction formats 83 instructions/ 9 addressing modes
Internal flash memory	256K bytes Rewrite durability : 100 times
Internal RAM	M32172F2VFP : 16K bytes M32173F2VFP : 32K bytes
DMAC	10 channels (DMA transfers between internal peripheral I/Os, between internal peripheral I/O and internal RAM, and between internal RAMs) Channels can be cascaded and can operate in combination with internal peripheral I/O
Multijunction timer	26 channels of multijunction timers. •16-bit output-related timers ×16 channels (continuous, single-shot, single-shot PWM or PWM) •16-bit input-related timers × 6 channels (measurement, event count mode, × 4 event count , up/down event count) •32-bit input-related timers × 4 channels (measurement, new/old captured data retention function available)
A-D converter	2 independent 10-bit multifunction A-D converters •Input 8 channel × 1, Input 4channel × 1 •Capable of interrupt conversion during scan •8-bit/10-bit readout function available
Serial I/O	8 channels (The serial I/Os can be set for synchronous serial I/O or UART. SIO2,3,6,7 are UART mode only)
Real-time debugger (RTD)	1-channels dedicated clock-synchronized serial The entire internal RAM can be read or rewritten from the outside without CPU intervention
Interrupt controller	Controls interrupts from internal peripheral I/Os (Priority can be set to one of 8 levels including interrupt disabled)
Wait controller	Controls wait when accessing 4-channel external extended area (1 to 4 wait cycles inserted + prolonged by external WAIT signal input)
D-A converter	2channel of 8-bit resolution D-A converters D-A 0 converter : D-A output, any data continuous output function, and 256-byte parameter table available D-A 1 converter : D-A output only

Table 1 Outline Performance (2/2)

Function Block	Features
PD interface	Two-channel PD sensor interface circuits Built-in 8 channel timers (When not using phase sensors, these timers can be used as ordinary input measurement timer or input event counter)
CAN	two channels, each having 16-channel message slots
JTAG	Boundary-Scan function, Built-in SDI debugger function in MITSUBISHI
Clock	Maximum CPU clock : 40MHz (access to CPU, internal ROM, and internal RAM) Maximum internal peripheral clock : 20MHz (access to internal peripheral module) Maximum external input clock : 10.0MHz, Built-in × 4 PLL circuit
Power Supply Voltage	5V (±0.5V) : External I/O 3.3V (±0.3V) : Internal logic
Operating temperature rang	-40 to +125°C(CPU clock 32MHz , internal peripheral clock 16MHz) -40 to +85°C(CPU clock 40MHz , internal peripheral clock 20MHz)
Package	0.5mm pitches / 144-pin plastic LQFP

Outline of the CPU core

The microcomputer uses the M32R RISC CPU core, and has an instruction set which is common to all microcomputers in the M32R family.

Instructions are processed in five pipelined stages consisting of instruction fetch, decode, execution, memory access, and write back. Thanks to its “out-of-order-completion” mechanism, the M32R CPU allows for clock cycle efficient, instruction execution control.

The M32R CPU internally has sixteen 32-bit general-purpose registers. The instruction set consists of 83 discrete instructions, which come in either a 16-bit instruction or a 32-bit instruction format. Use of the 16-bit instruction format helps to reduce the code size of a program. Also, the availability of 32-bit instructions facilitates programming and increases the performance at the same clock speed, as compared to architectures with segmented address spaces.

Sum-of-products instructions comparable to DSP

The M32R CPU contains a multiplier/accumulator that can execute 32 bits × 16 bits in one cycle. Therefore, it executes a 32 bit × 32 bit integer multiplication instruction in three cycles. Also, the M32R CPU supports the following four sum-of-products instructions (or multiplication instructions) for DSP function use.

(1) 16 high-order register bits × 16 high-order register bits
(2) 16 low-order register bits × 16 low-order register bits
(3) All 32 register bits × 16 high-order register bits
(4) All 32 register bits × 16 low-order register bits

Furthermore, the M32R CPU has instructions for rounding the value stored in the accumulator to 16 or 32 bits, and instructions for shifting the accumulator value to adjust digits before storing in a register. Because these instructions also can be executed in one cycle, DSP comparable data processing capability can be obtained by using them in combination with high-speed data transfer instructions such as Load & Address Update or Store & Address Update.

Built-in clock multiplier circuit

The clock multiplier circuit multiplies the frequency of the input clock signal by 4 to produce the internal operating clock. When the maximum CPU clock frequency = 40 MHz, the input clock frequency is 10.0 MHz.

Three operation modes

The microcomputer has three operation modes: single-chip mode, external extended mode, and processor mode. These operation modes are changed from one to another by setting the MOD0 and MOD1 pins.

Address space

The logical address is always handled in width of 32 bits, providing a linear address space of up to 4 Gbytes. The address space is divided into the following spaces.

User space

A 2-Gbyte area from H’0000 0000 to H’7FFF FFFF is the user space. Located in this space are the user ROM area, external extended area, internal RAM area, and SFR (Special Function Register) area (internal peripheral I/O registers). Of these, the user ROM area and external extended area are located differently depending on mode settings.

Boot program space

A 1-Gbyte area from H’8000 0000 to H’BFFF FFFF is the boot program area. This space contains the on-board programming program (boot program) used in blank state by the internal flash memory.

System space

A 1-Gbyte area from H’C000 0000 to H’FFFF FFFF is the system area. This space is reserved for use by development tools such as an in-circuit emulator and debug monitor, and cannot be used by the user.

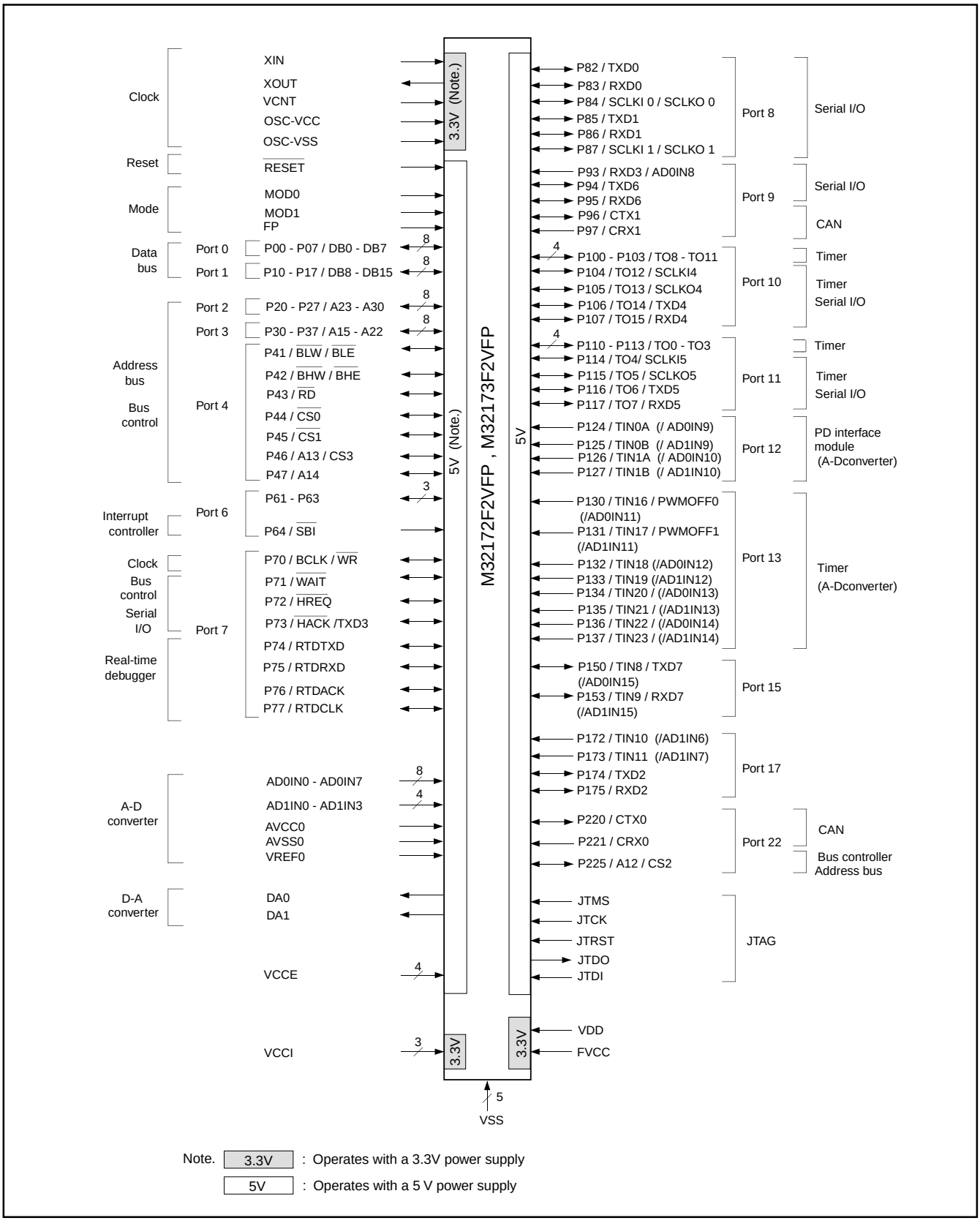


Figure 2. Pin Function Diagram

Table 2 Description of Pin Function (1/4)

Type	Pin Name	Description	Input/Output	Function
Power supply	VCCE	Power supply	—	Supplies power (5 V) to external I/O ports.
	VCCI	Power supply	—	Supplies power (3.3 V) to the internal logic.
	VDD	RAM power supply	—	Internal RAM backup power supply (3.3 V).
	FVCC	Flash power supply	—	Internal flash memory backup power supply (3.3 V).
	VSS	Ground	—	Connect all VSS pins to ground (GND).
Clock	XIN, XOUT	Clock	Input Output	Clock input/output pins. These pins contain a PLL-based frequency multiply-by-4, so input the clock whose frequency is quarter the operating frequency. (XIN input = 10 MHz when CPU clock operates at 40 MHz)
	BCLK / $\overline{WR}$	System clock	Output	When this signal is System Clock(BCLK), it outputs a clock whose is twice that of external inpout clock. (BCLK output = 20 MHz when CPU clock operates at 40 MHz). Use this clock when circuits are synchronized externally. When this signal is Write($\overline{WR}$),during external write access it indicates the valid data on the data bus to transfer.
	OSC-VCC	Power supply	—	Power supply to the PLL circuit. Connect OSC-VCC to the power supply
	OSC-VSS	Ground	—	Connect OSC-VSS to ground.
	VCNT	PLL control	Input	This pin controls the PLL circuit. Connect a resistor and capacitor to this pin.
Reset	$\overline{RESET}$	Reset	Input	This pin resets the internal circuits.
Mode	MOD0 MOD1	Mode	Input	These pins set an operation mode.
Address bus	A12 – A30	Address bus	Output	19 lines of address bus (A12 – A30) are provided to accommodate two channels of 1 MB memory space (max.) connected external to the chip. A31 is not output. A12 and A13 are shared with $\overline{CS2}$ and $\overline{CS3}$, so that when $\overline{CS2}$, $\overline{CS3}$ are selected memory space is reduced , but up to 4 channels of memory space can be added.
Data bus	DB0 – DB15	Data bus	Input/output	This 16-bit data bus connects to external device. In the write cycle, of the 16-bit data bus the valid byte positions to write are output as $\overline{BHW}$/ $\overline{BHE}$ and $\overline{BLW}$/ $\overline{BLE}$. In read cycle, data on the entire 16-bit data bus is read. However, only the data at the valid byte positions are transferred to the M32R's internal circuit.

FP	MOD0	MOD1	Mode
X	0	0	Single-chip mode
X	0	1	Expanded external mode
0	1	0	Processor mode
1	1	0	Boot mode
X	1	1	(Reserved)

Table 2. Description of Pin Function (2/4)

Type	Pin type	Description	Input/Output	Function
Bus control	$\overline{CS0}$, $\overline{CS1}$ $\overline{CS2}$, $\overline{CS3}$	Chip select	output	Chip select signals for external devices. $\overline{CS2}$ and $\overline{CS3}$ are shared with A12 and A13.
	$\overline{RD}$	Read	output	This signal is output when reading external devices.
	$\overline{BHW}$/ $\overline{BHE}$	Byte high write	output	Indicates the byte positions to which valid are transferred when writing to external devices.$\overline{BHW}$/ $\overline{BHE}$ and $\overline{BLW}$/ $\overline{BLE}$ correspond to the upper address side(D0-D7 effective) and the lower address side(D8-D15 effective),respectivel.
	$\overline{BLW}$/ $\overline{BLE}$	Byte low write	output	
	$\overline{WAIT}$	Wait	input	If $\overline{WAIT}$ input is low when the M32R accesses external devices, the wait cycle extended.
	$\overline{HREQ}$	Hold request	input	This pin is used by an external device to request control of the external bus. The M32R goes to a hold state when $\overline{HREQ}$ input is pulled low.
	$\overline{HACK}$	Hold acknowledge	output	This signal indicates to the external device that the M32R has entered a hold state and relinquished control of the external bus.
Timer	TIN8 -TIN11, TIN16 -TIN23	Timer input	input	Timer input pins
	TO0 - TO15	Timer output	output	Timer output pins
PD interface	TIN0A, TIN0B	Timer input	input	Timer input pins for PD interface 0.
	TIN1A, TIN1B	Timer output	output	Timer output pins for PD interface1
D-A converter	DA0	Analog output	output	Analog output pin of the D-A0 converter.
	DA1	Analog output	output	Analog output pin of the D-A1 converter.
A-D	AVCC0	Analog power upply	—	AVCC0 is the power supply for the A-D and D-A converters. Connect AVCC0 to the power supply (5V).
	AVSS0	Analog ground	—	AVSS0 is the analog ground for the A-D and D-A converters. Connect AVCC0 to ground.
	VREF0	Reference voltage input	input	VREF0 is the reference voltage input pin (5V) for the A-D and D-A converters.
	AD0IN0 - AD0IN7	Analog input	input	8-channel analog input pin for A-D0 converter
	AD1IN0 - AD1IN3	Analog input	input	4-channel analog input pin for A-D1 converter
	AD0IN8 - AD0IN15, AD1IN4 - AD1IN15	Analog input	nput	20-channel analog input pin for pin level monitor

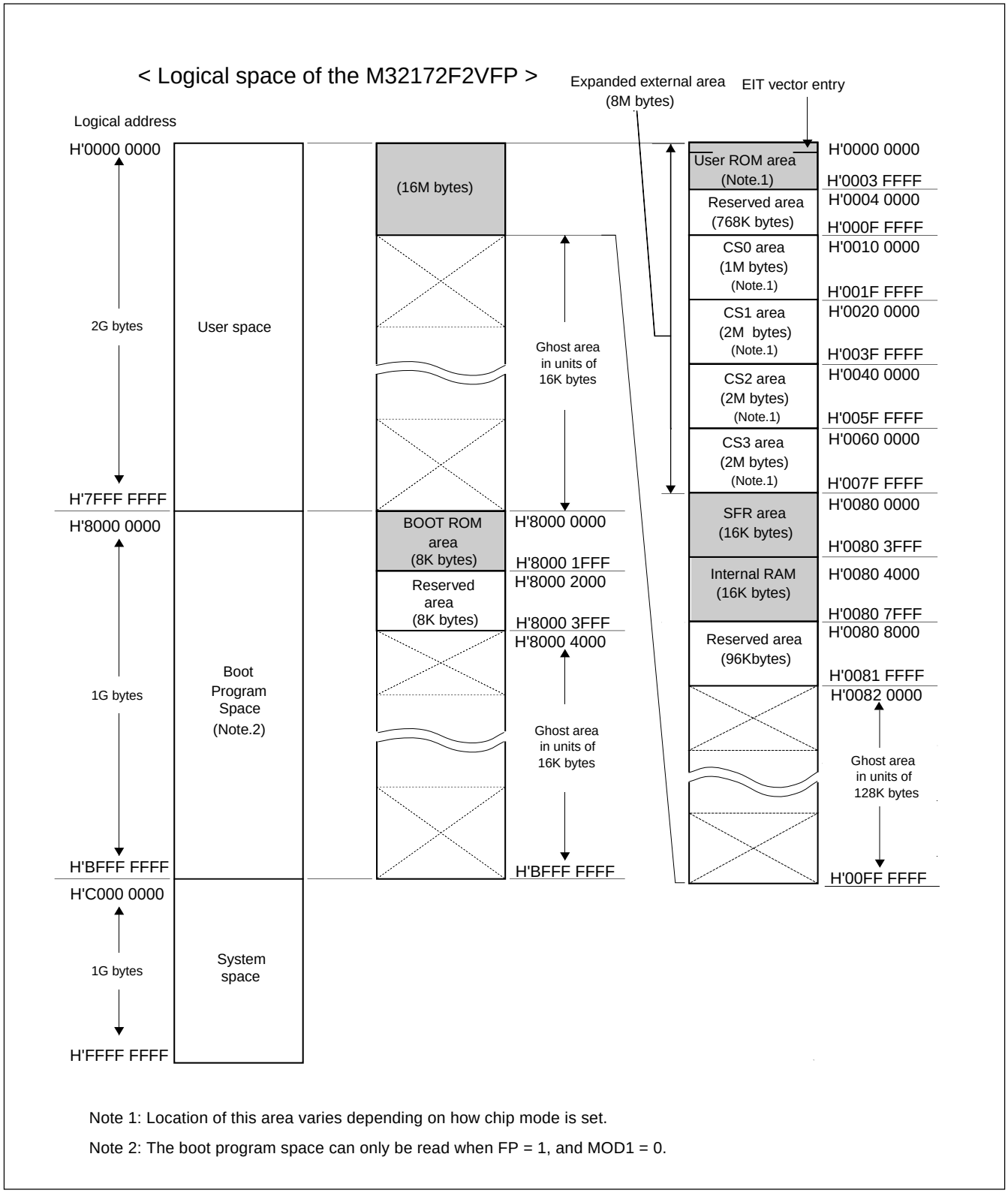
Table 2. Description of Pin Functions (3/4)

Type	Pin name	Description	Input/output	Function
Interrupt controller	$\overline{SBI}$	System break interrupt	Input	System break interrupt(SBI) input pin of the interrupt controller
Serial I/O	SCLKI0/ SCLKO0 - SCLKI1/ SCLKO1	UART transmit/receive clock output or CSIO transmit/receive clock input/output	Input/output	For UART mode: Clock output derived from BRG output by dividing it by 2 For CSIO mode: Transmit/receive clock input when external clock is selected Transmit/receive clock output when internal clock is selected
	SCLKI4, SCLKI5	Clock input	Input	For UART mode: Use inhibited (input state) For CSIO mode: Transmit/receive clock input when external clock is selected
	SCLKO4, SCLKO5	Clock output	output	For UARTmode: Clock output derived from BRG output by dividing it by 2 For CSIO mode: Transmit/receive clock output
	TXD0 - TXD7	Transmit data	output	Transmit data output pin of serial I/O
	RXD0 - RXD7	Receive data	input	Receive data input pin of serial I/O
Real-Time Debugger	RTDTXD	Transmit data	output	Serial data output pin of the real-time debugger
	RTDRXD	Receive data	input	Serial data input pin of the real-time debugger
	RTDCLK	Clock input	input	Serial data transmit/receive clock input pin of the real-time debugger
	RTDACK	Acknowledge	output	This pin outputs a low pulse synchronously with the real-time debugger's first clock of serial data output word. The low pulse width indicates the type of the command/data the realtime debugger has received.
Flash-only	FP	Flash protect	Input	This pin protects the flash memory against E/W in hardware.
CAN	CTX0, CTX1	Transmit data	output	Data output pin from CAN module.
	CRX0, CRX1	Receive data	Input	Data input pin to CAN module.

Table 2. Description of Pin Functions (4/4)

Type	Pin name	Description	Input/output	Function
JTAG	JTMS	Test mode	Input	Test select input for controlling the test circuit's state transition
	JTCK	Clock	Input	Clock input to the debugger module and test circuit.
	JTRST	Test reset	Input	Test reset input for initializing the test circuit asynchronously.
	JTDO	Serial output	Output	Serial output of test instruction code or test data.
	JTDI	Serial input	Input	Serial input of test instruction code or test data.
Input/	P00-P07	Input/output port0	Input/output	Programmable input/output port.
output	P10-P17	Input/output port1	Input/output	Programmable input/output port.
port	P20-P27	Input/output port2	Input/output	Programmable input/output port.
(Note)	P30-P37	Input/output port3	Input/output	Programmable input/output port.
	P41-P47	Input/output port4	Input/output	Programmable input/output port.
	P61-P64	Input/output port6	Input/output	Programmable input/output port. (However, P64 is an input-only port)
	P70-P77	Input/output port7	Input/output	Programmable input/output port.
	P82-P87	Input/output port8	Input/output	Programmable input/output port.
	P93-P97	Input/output port9	Input/output	Programmable input/output port. (However, P93,P97 is an input-only port)
	P100 -P107	Input/output port10	Input/output	Programmable input/output port.
	P110 -P117	Input/output port111	Input/output	Programmable input/output port.
	P124 -P127	Input/output port112	Input	Input-only port
	P130 -P137	Input/output port113	Input	Input-only port
	P150,P153	Input/output port115	Input/output	Programmable input/output port.
	P172 -P175	Input/output port117	Input/output	Programmable input/output port. (However, P172,P173 is an input-only port)
	P220, P221,P225	Input/output port122	Input/output	Programmable input/output port. (However, P221 is an input-only port)

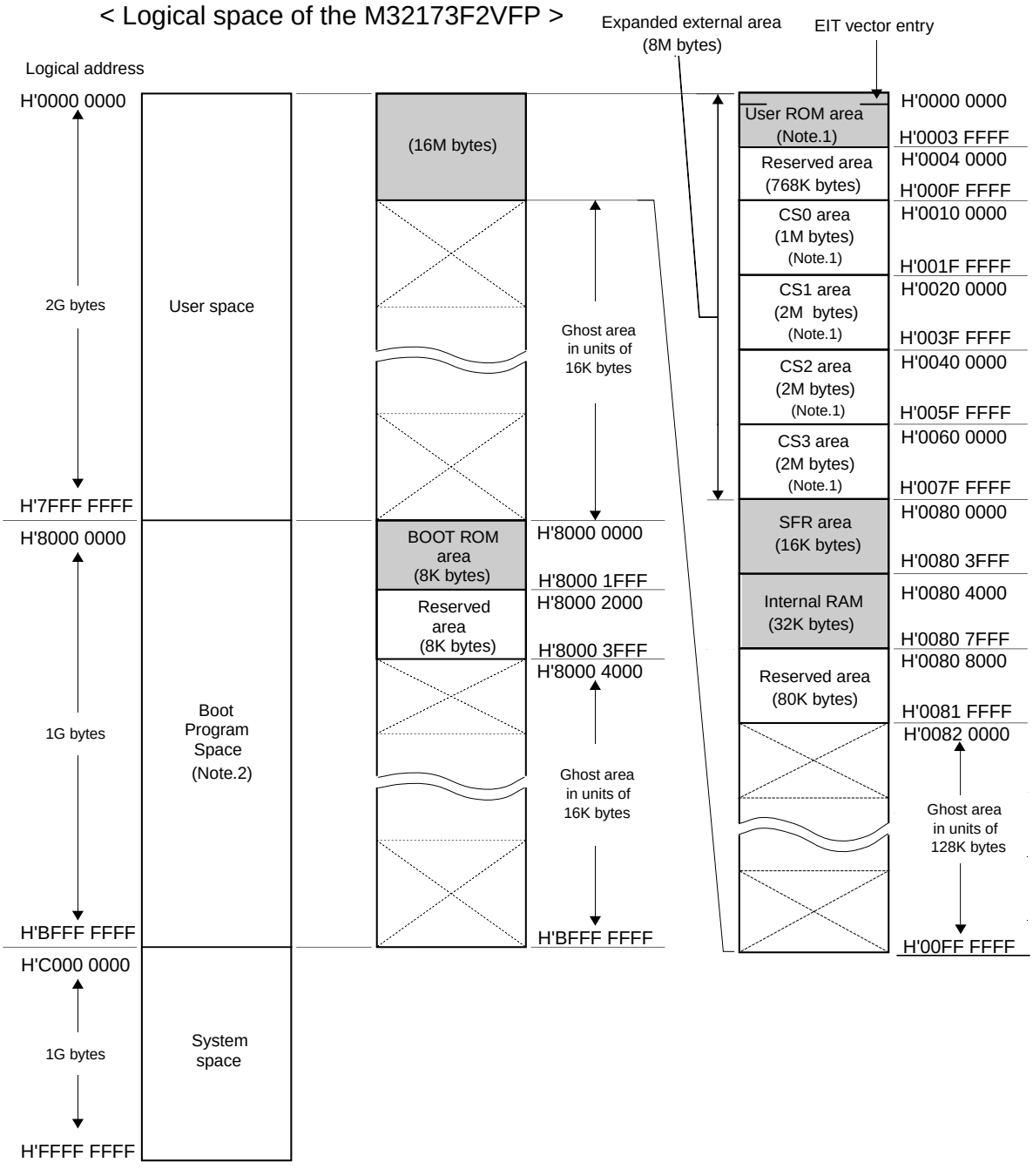
Note. Input/output port 5 is reserved for future use.
Input/output ports 14,16,18,19,20,and 21do not exist.



Note 1: Location of this area varies depending on how chip mode is set.

Note 2: The boot program space can only be read when FP = 1, and MOD1 = 0.

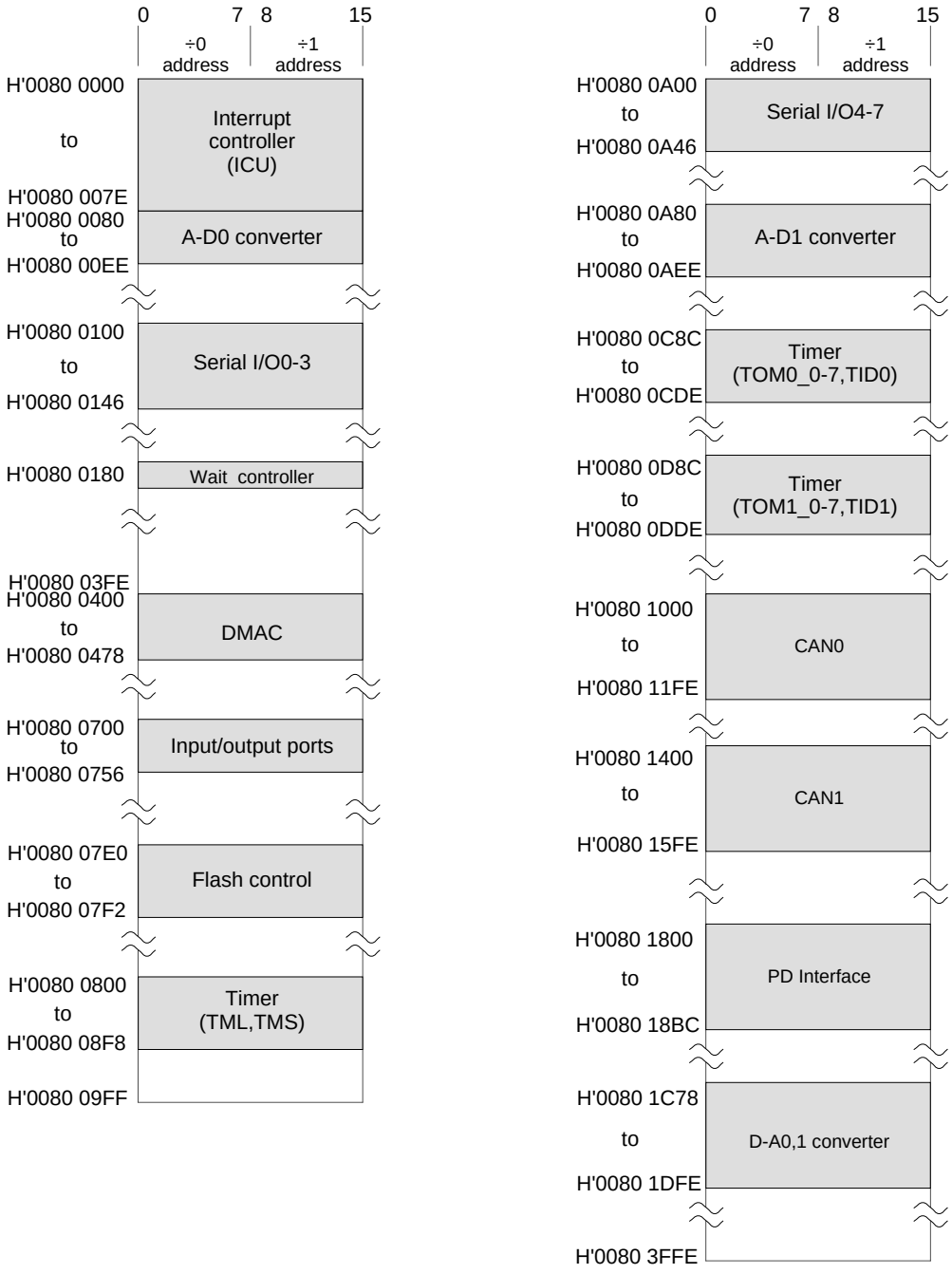
Figure 3: Address Space of the M3172F2VFP



Note 1: Location of this area varies depending on how chip mode is set.

Note 2: The boot program space can only be read when FP = 1, and MOD1 = 0.

Figure 4: Address Space of the M32173F2VFP



Note. The real-time debugger (RTD) is an independent module operated from external circuits, and is transparent to the CPU.

Figure 5. SFR Area

Built-in Flash Memory and RAM

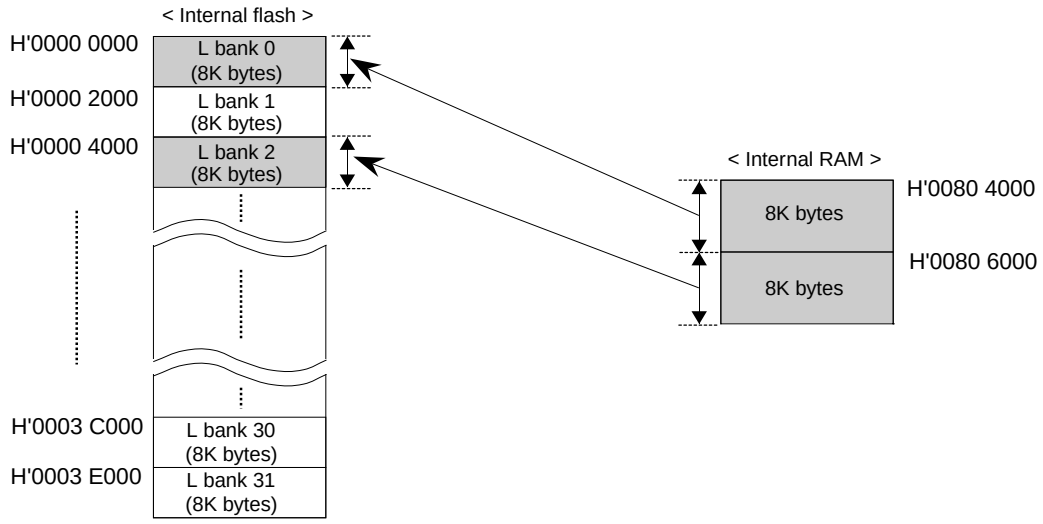
The M32172F2VFP contains 256-Kbyte flash memory and 16-Kbyte RAM. The M32173F2VFP contains 256-Kbyte flash memory and 32-Kbyte RAM.

The internal flash memory can be programmed on-board (i.e., while being mounted on the printed circuit board). This means that the same chip as will be used in mass-production can be used directly from the development stage on, allowing for system development without having to change the printed circuit board when proceeding from trial production to mass-production.

Built-in Pseudo-flash Emulation Function

A function is provided that can map 8-Kbyte blocks of the internal RAM beginning with the first address (up to two blocks for the M32172F2VFP or up to 3 blocks for the M32173F2VFP) into areas of the internal flash memory which are divided in units of 8 Kbytes (L banks). In addition, the M32173F2VFP has the function to map 4-Kbyte blocks of the internal RAM beginning with the H'0080 A000 area (up to two blocks) into areas of the internal flash memory which are divided in units of 4 Kbytes (S banks).

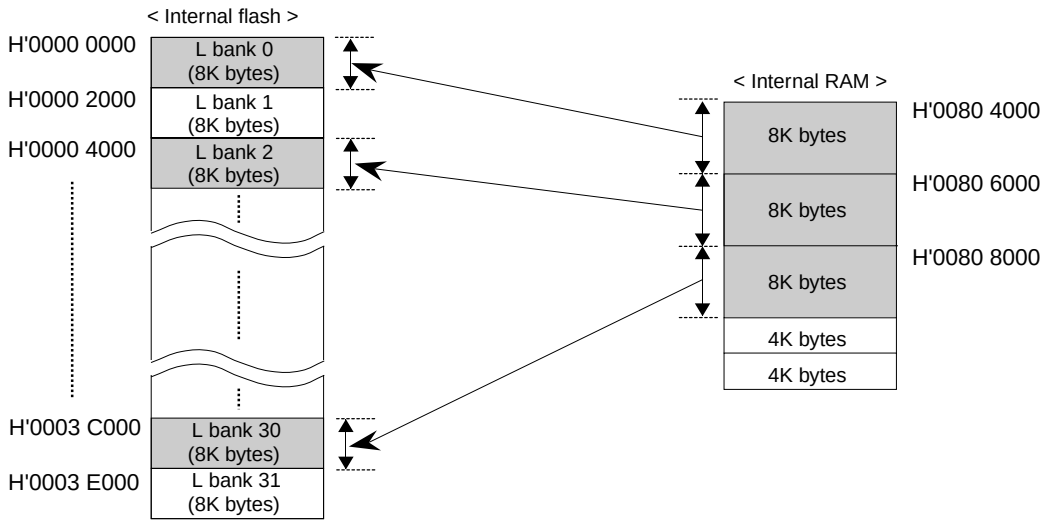
This function allows parts of the program which are frequently changed during development to be altered or evaluated without having to reset the microcomputer each time. What's more, when combined with the realtime debugger, this function helps to reduce the program evaluation period, because data in the RAM can be rewritten without requiring any CPU load.



Note 1: If the same bank area is set in multiple pseudo-flash bank registers and the pseudo-flash emulation enable bit is enabled, the corresponding internal RAM area is assigned to either bank register according to the priority FELBANK0 > FELBANK1.

Note 2: When access is made to the 8-Kbyte area (L bank) specified with pseudo-flash bank registers 0 and 1, the internal RAM area is accessed. During pseudo-flash emulation mode, RAM data can read and written to and from both the internal RAM area and the pseudo-flash setup area.

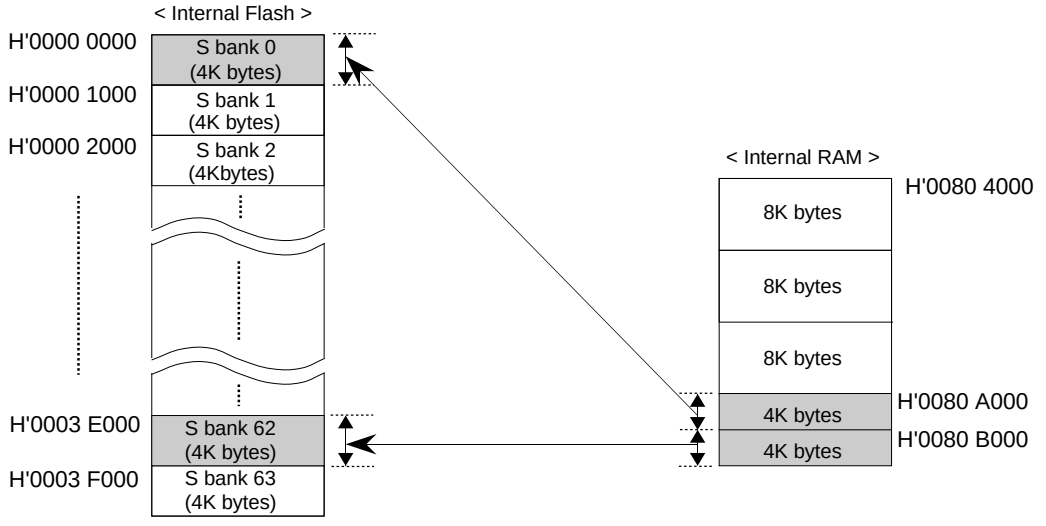
Figure 6. Pseudo-Flash Emulation Areas of the M32172F2VFP (Replaced in Units of 8 Kbytes)



Note 1: If the same bank area is set in multiple pseudo-flash bank registers and the pseudo-flash emulation enable bit is enabled, the corresponding internal RAM area is assigned to either bank register according to the priority FELBANK0 > FELBANK1 > FELBANK2 > FELBANK0 > FELBANK1.

Note 2: When access is made to the 8-Kbyte area (L bank) specified with pseudo-flash bank registers 0 - 2, the internal RAM area is accessed. During pseudo-flash emulation mode, RAM data can read and written to and from both the internal RAM area and the pseudo-flash setup area.

Figure 6. Pseudo-Flash Emulation Areas of the M32173F2VFP (Replaced in Units of 8 Kbytes)



Note 1: If the same bank area is set in multiple pseudo-flash bank registers and the pseudo-flash emulation enable bit is enabled, the corresponding internal RAM area is assigned to either bank register according to the priority FELBANK0 > FELBANK1 > FELBANK2 > FELBANK0 > FELBANK1 .

Note 2: When access is made to the 4-Kbyte area (S bank) specified with pseudo-flash bank registers 0 and 1, the internal RAM area is accessed. During pseudo-flash emulation mode, RAM data can read and written to and from both the internal RAM area and the pseudo-flash setup area.

Figure 6. Pseudo-Flash Emulation Areas of the M32173F2VFP (Replaced in Units of 4 Kbytes)

Input/output Ports

The microcomputer has a total of 99 input/output ports P0-P22. (However, P5 is reserved for future use, and ports P14, P16, and P18-21 do not exist.) The input/output ports can be used as input ports or output ports by setting up their direction registers.

Each input/output port is a dual-function pin shared with otherinternal peripheral I/O or external extended bus signal lines. These pin functions are selected by using the chip operation mode select or the input/output port operation mode registers. These input/output ports are interfaced using a dedicated power supply to allow for connections to the peripheral circuits operating with 5V.

Table3. Outline of Input/output Ports

Item	Specification
Number of Port (Note1)	Total 99 ports P0 : P00 - P07 (8 lines) P1 : P10 - P17 (8 lines) P2 : P20 - P27 (8 lines) P3 : P30 - P37 (8 lines) P4 : P41 - P47 (7 lines) P6 : P61 - P64 (4 lines) P7 : P70 - P77 (8 lines) P8 : P82 - P87 (6 lines) P9 : P93 - P97 (5 lines) P10 : P100 - P107 (8 lines) P11 : P110 - P117 (8 lines) P12 : P124 - P127 (4 lines) P13 : P130 - P137 (8 lines) P15 : P150,P153 (2 lines) P17 : P172 - P175 (4 lines) P22 : P220,P221,P225 (3 lines)
Port function	The input/output ports can be set for input or output mode bitwise by using the input/output port direction control register. (However, P64 is an SBI# input-only port, P97 and P221 are CAN0 input-only ports, and P93, P124–P127, P130–P137, P172, and P173 are input-only ports.)
Pin function	Dual-functions shared with peripheral I/O or external extended signals (or multi-functions shared with peripheral I/Os which have multiple functions)
Pin function changeover	P0-4,P225 : Changed by setting CPU operation mode (MOD0 and MOD1 pins) P6-22 : Changed by setting the input/output port operation mode register (However, peripheral I/O pin functions are selected using the peripheral I/O register.)

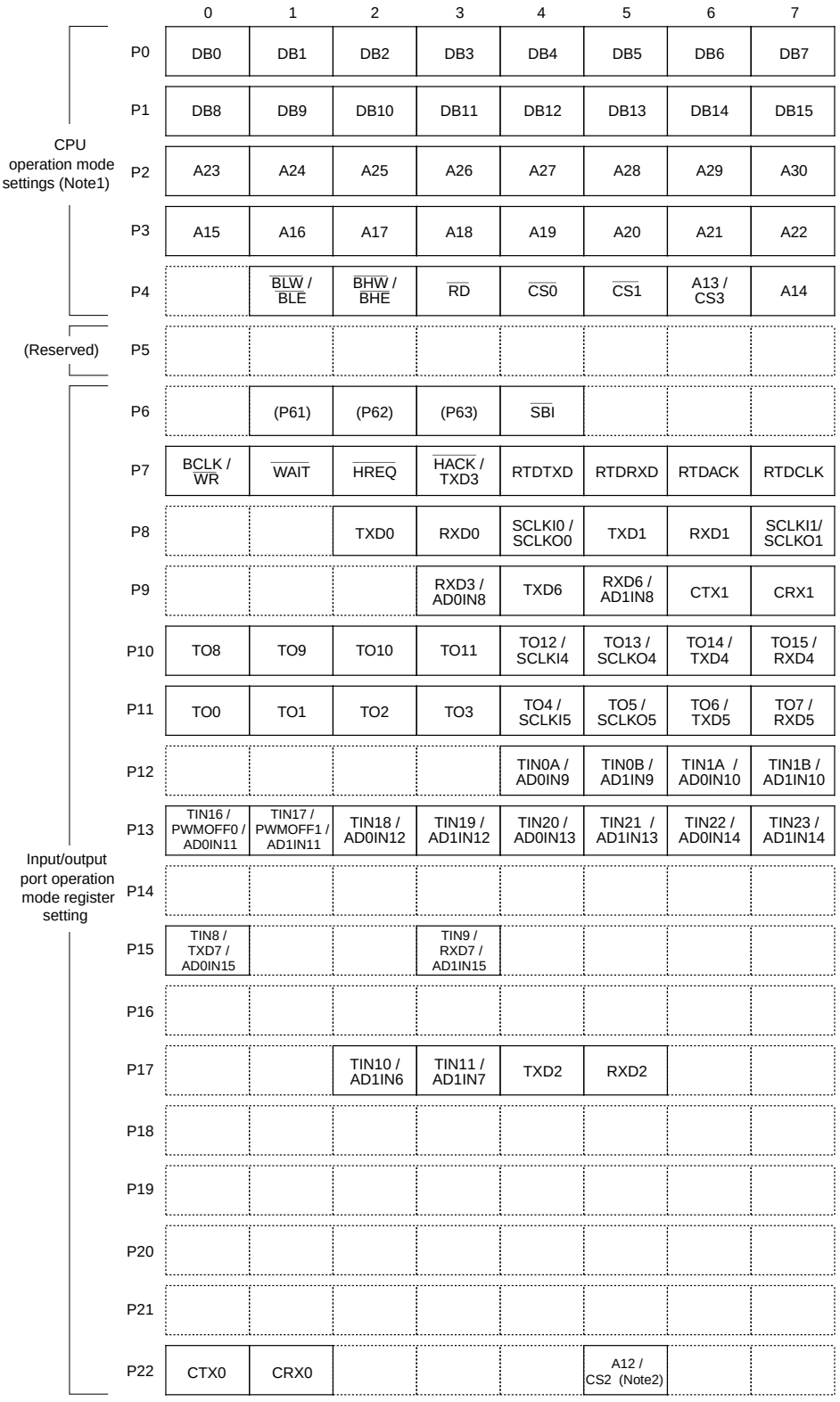
Note 1: P14, P16, and P18–21 do not exist.

Note 2: P0–P4 (except P46) can have their pin functions changed by setting the operation mode register only when the CPU is operating in external extended mode. (When the CPU is operating in single-chip or processor mode, the pin functions are changed by setting CPU operation mode.)

Table 4. CPU Operation Modes and P0–P4 Pin Functions

MOD0	MOD1	Operation mode	P0-P4 pin function
VSS	VSS	Single-chip mode	Input/output port pin
VSS	VCC	External extended mode	External extended signal pin
VCC	VSS	Processor mode (FP pin = VSS)	
VCC	VCC	Reserved (use inhibited)	

Note: VCC and VSS are connected to +5 V and GND, respectively.



Note1: The pin function are selected by setting the MOD0 and MOD1 pins.
Note2: The pin function are selected by setting the MOD0 and MOD1 pins.
These pins have debug event function.

Figure 9. Input/output Ports and Pin Function Assignments

Built-in 10-Channel DMAC

The microcomputer contains 10 channels of DMAC, allowing for data transfer between internal peripheral I/Os, between internal RAM and internal peripheral I/O, and between internal RAMs.

DMA transfer requests can be issued from the user-created software, as well as can be triggered by a signal generated by the internal peripheral I/O (A-D converter, timer, or serial I/O).

The microcomputer also supports cascaded connection between DMA channels (starting DMA transfer on a channel at end of transfer on another channel). This makes advanced transfer processing possible without causing any additional CPU load.

Table 5. Outline of the DMAC

Item	Content
Number of channels	10 channels
Transfer request	•Software trigger •Request from internal peripheral I/O: A-D converter, timer, or serial I/O (reception •completed, transmit buffer empty) •Cascaded connection between DMA channels possible (Note)
Maximum number of times transferred	256 times
Transferable address space	•64 Kbytes (address space from H'0080 0000 to H'0080 FFFF) •Transfers between internal peripheral I/Os, between internal RAM and internal peripheral IO, and between internal RAMs are supported
Transfer data size	16 bits or 8 bits
Transfer method	Single transfer DMA (control of the internal bus is relinquished for each transfer performed), dual-address transfer
Transfer mode	Single transfer mode
Direction of transfer	One of three modes can be selected for the source and destination of transfer: •Address fixed •Address increment •32-channel ring buffer
Channel priority	Channel 0 > channel 1 > channel 2 > channel 3 > channel 4 > channel 5 > channel 6 > channel 7 > channel 8 > channel 9 (Fixed priority)
Maximum transfer rate	13.3 Mbytes per second (when internal peripheral clock = 20 MHz)
Interrupt request	Group interrupt request can be generated when each transfer count register underflows
Transfer area	64 Kbytes from H'0080 0000 to H'0080 FFFF (Transfer is possible in the entire internal RAM/SFR area)

Note: The following DMA channels can be cascaded.

DMA transfer on channel 1 started at end of one DMA transfer on channel 0
DMA transfer on channel 2 started at end of one DMA transfer on channel 1
DMA transfer on channel 0 started at end of one DMA transfer on channel 2
DMA transfer on channel 4 started at end of one DMA transfer on channel 3
DMA transfer on channel 6 started at end of one DMA transfer on channel 5
DMA transfer on channel 7 started at end of one DMA transfer on channel 6
DMA transfer on channel 5 started at end of one DMA transfer on channel 7
DMA transfer on channel 9 started at end of one DMA transfer on channel 8
DMA transfer on channel 1-9 started at end of one DMA transfer on channel 9
DMA transfer on channel 5 started at end of all DMA transfers on channel 0 (underflow of transfer count register)
DMA transfer on channel 0-9 started at end of all DMA transfers on channel 1 (underflow of transfer count register)
DMA transfer on channel 8 started at end of all DMA transfers on channel 3 (underflow of transfer count register)

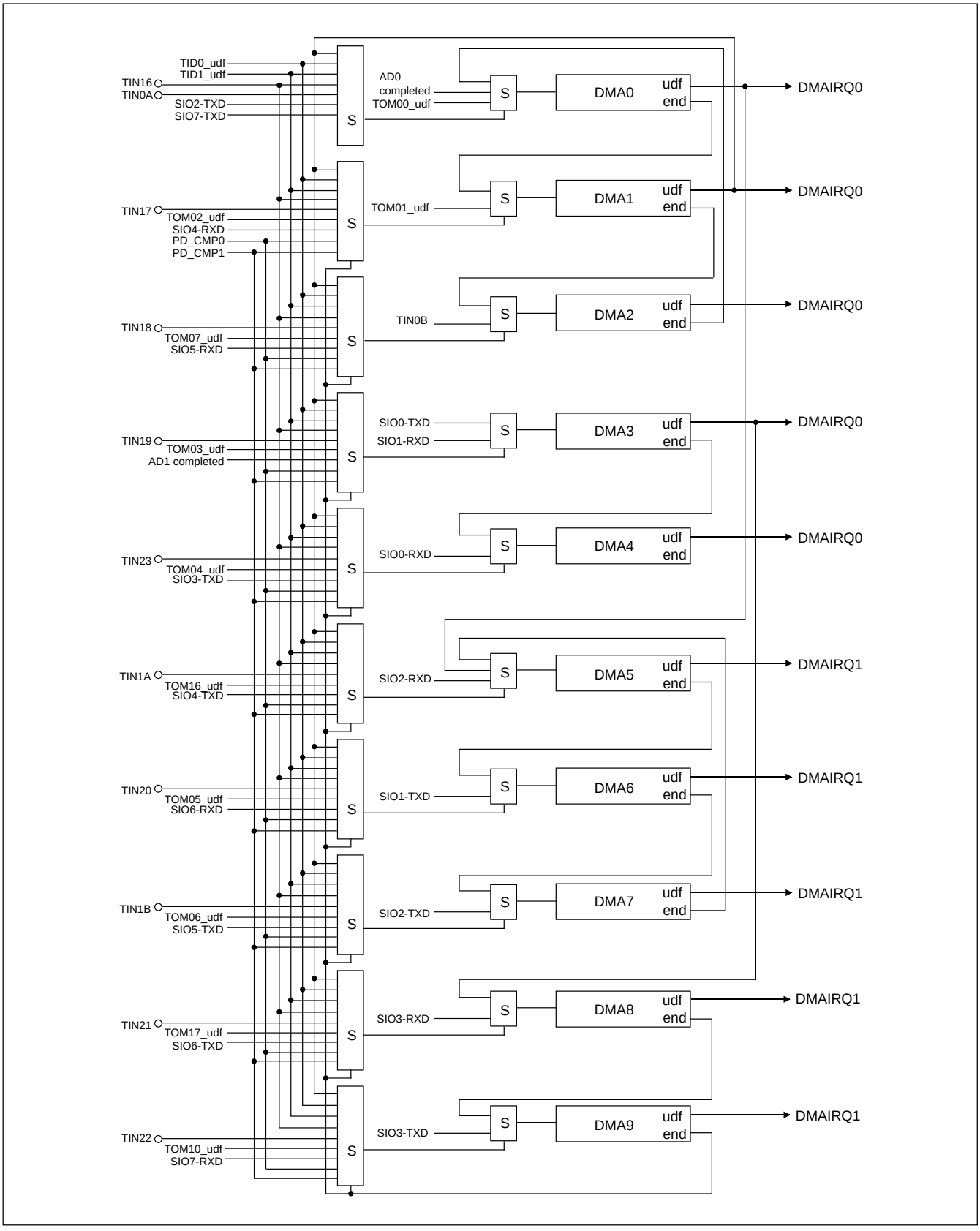


Figure10. Block Diagram of the DMAC

Built-in 26-Channel Timers

The microcomputer has total 26 channels of timers, consisting of 16-bit output related timer x 16 channels, 16-bit input related timer x 6 channels, and 32-bit input related timer x 4 channels. Each timer has multiple modes which can be selected according to the purpose of use.

Table 6. Outline of Timers

Name	Type	Number of channels	Content
TMS (Timer Measure Small)	Input related 16-bit timer (up counter)	4	6-bit input measurement timer. New and old captured data hold function available.
TML (Timer Measure Large)	Input related 32-bit timer (up counter)	4	16-bit input measurement timer. New and old captured data hold function available.
TID (Timer Input Derivation)	Input related 16-bit timer (up counter)	2	One of three input modes can be selected in software. • Fixed cycle mode • Event count mode • Multiply-by-4 event count mode • Up/down event count mode
TOM (Timer output Modification)	output related 16-bit timer (up counter)	16	One of four output modes can be selected in software. <No correction function> • PWM output mode • One-shot PWM output mode • One-shot output mode • Continuous output mode

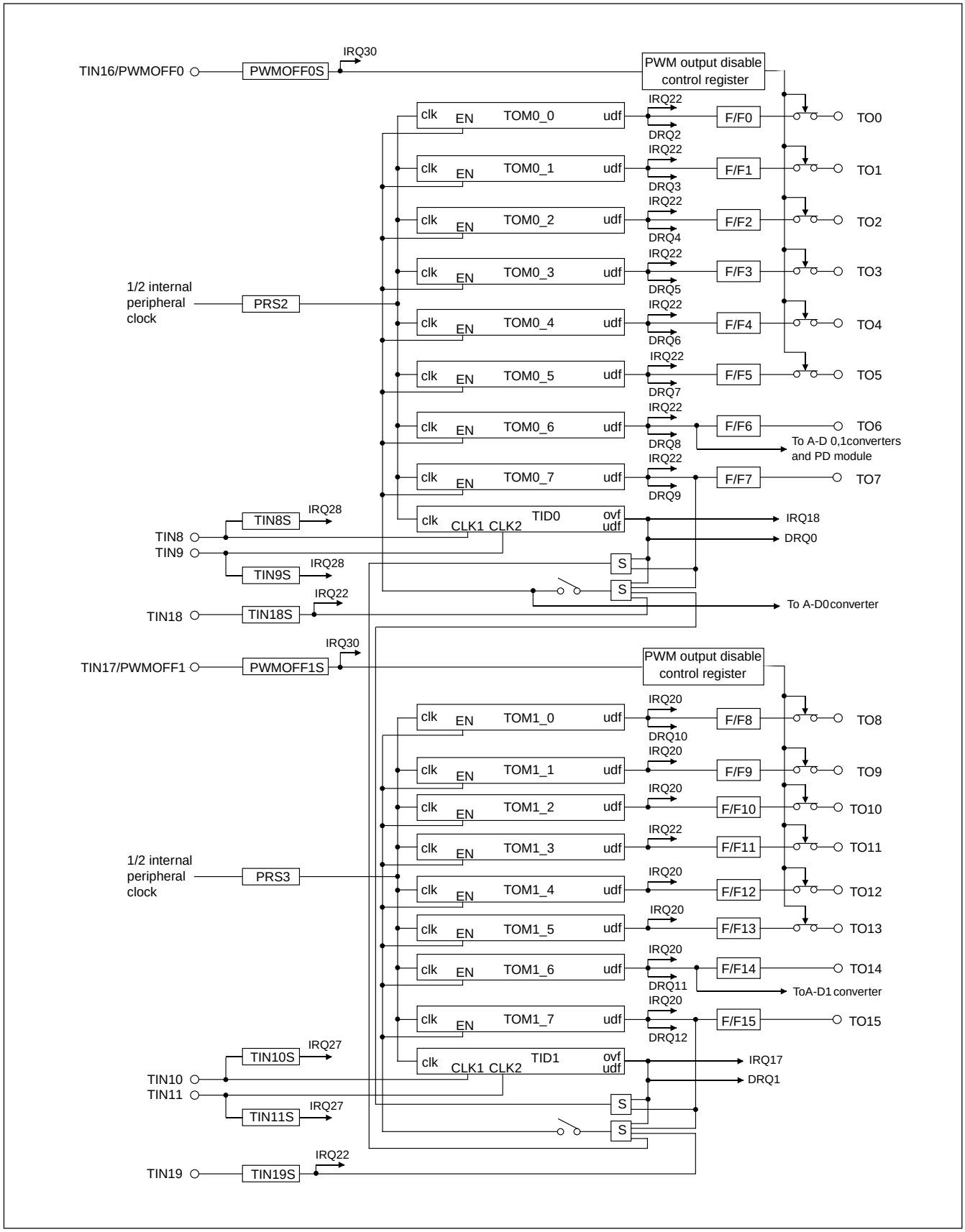


Figure 11. Block Diagram of Timers (1/2)

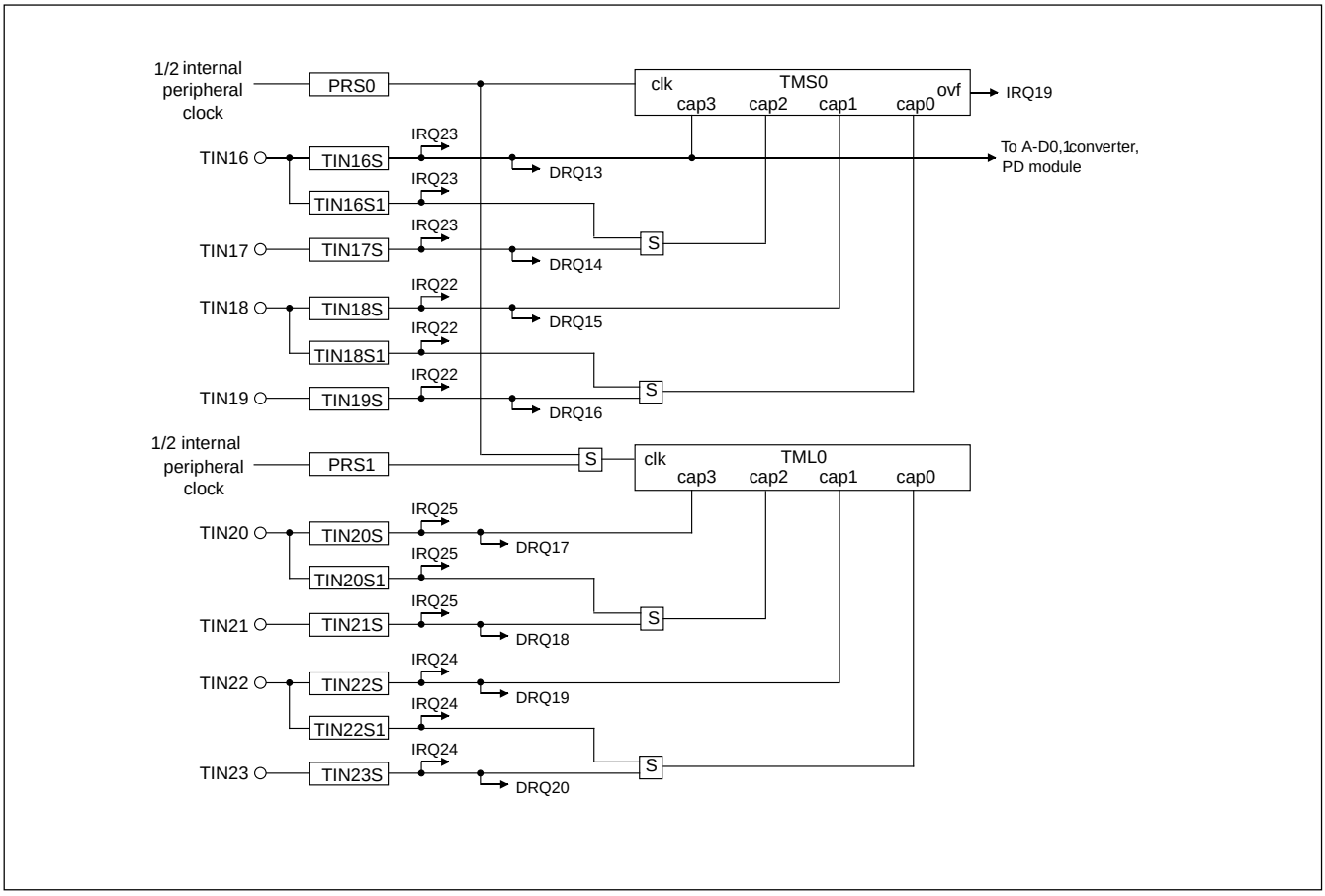


Figure 12. Block Diagram of Timers (2/2)

Built-in Two Independent A-D Converters

The microcomputer contains two A-D converters with 10-bit resolution (8-channel A-D0 converter and 4-channel A-D1 converter). In addition to individual conversion on each channel, these converters are capable of successive A-D conversions from channel 0 to channel n which are grouped into one. The A-D converted value can be read out in either 10 bits or 8 bits.

In addition to ordinary A-D conversion, the converters support comparator mode in which the set value and A-D converted value are compared to determine which is larger or smaller than the other.

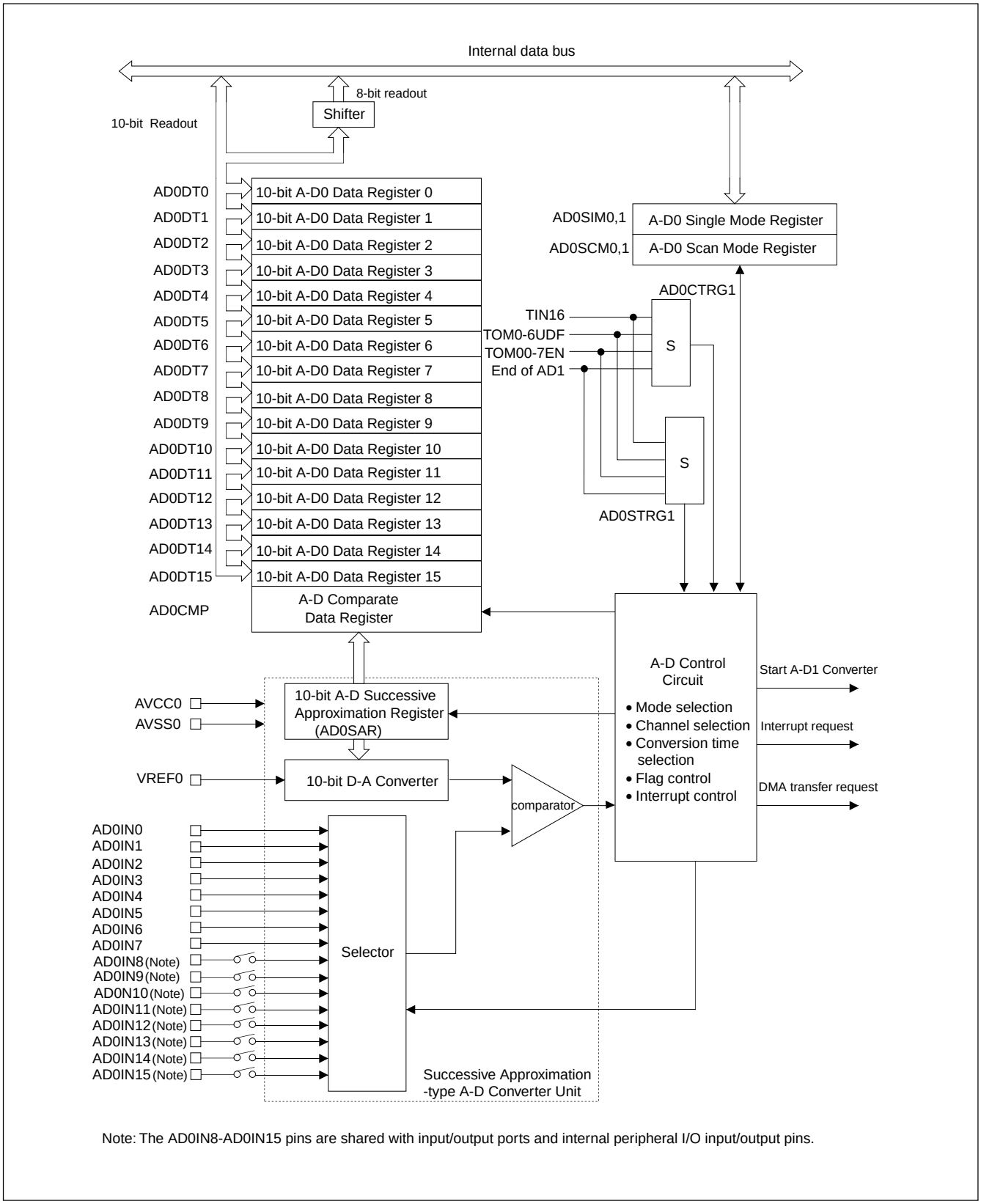
When A-D conversion is finished, the converters can generated a DMA transfer request, as well as an interrupt.

The A-D converters are interfaced using a dedicated power supply to allow for connections to the peripheral circuits operating with 5 V.

Table 7. Outline of the A-D Converters

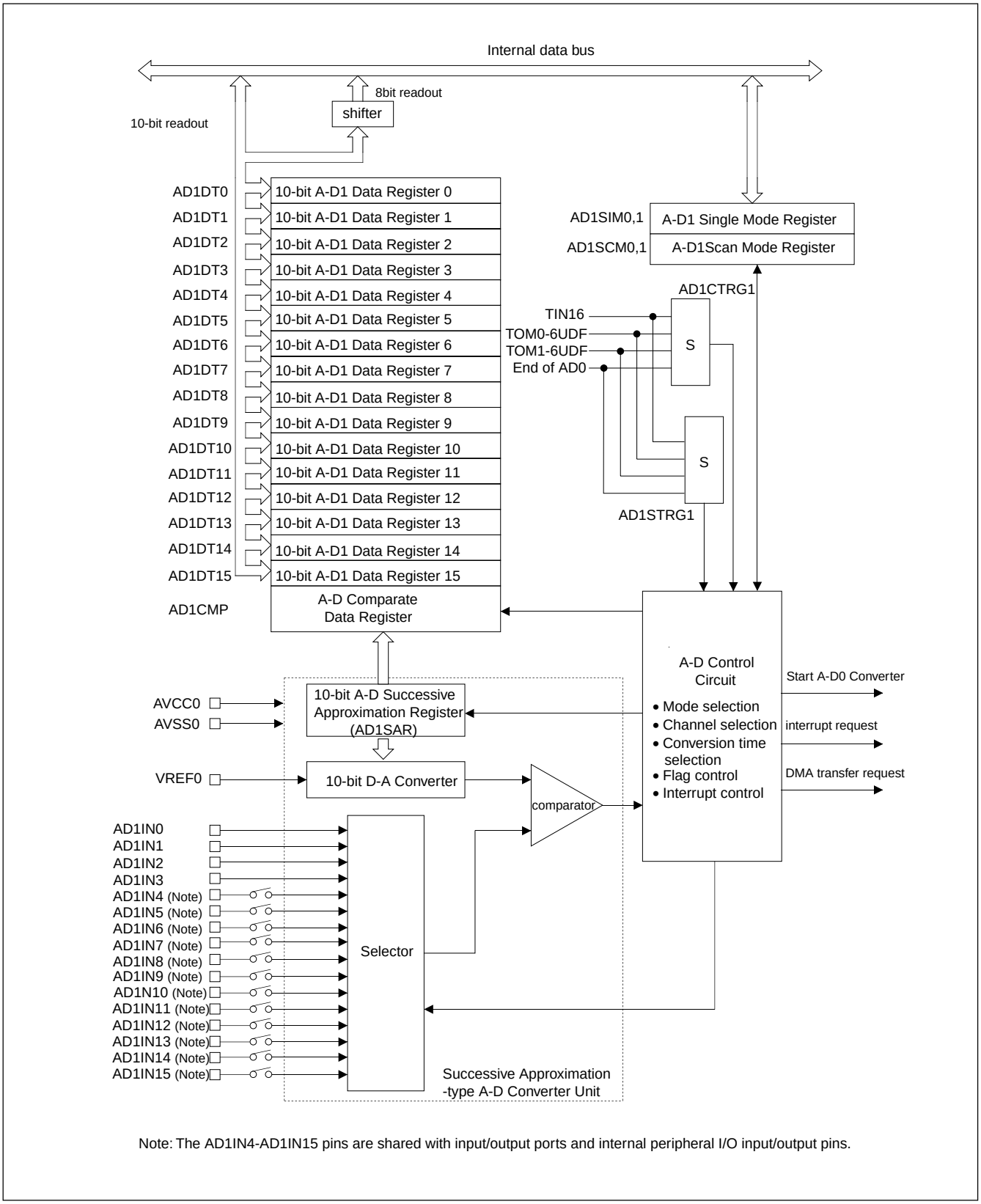
Item	Content			
Analog input	A-D0 converter: Analog input-only pin × 8 channels A-D0 converter: Analog input-only pin × 8 channels			
A-D conversion method	Successive approximation method			
Resolution	10 bits (Conversion results can be read out in either 10 or 8 bits)			
Nonlinearity error (Note 1) (Conditions: Ta = 25°, AVCC0,1 = VREF0,1 = 5.12 V)	Low speed mode	Normal	±2 LSB (Note 2)	
		Double speed	±2 LSB (Note 2)	
	High-speed mode	× 2 speed	±3LSB (Note 2)	
		× 4 speed	±3LSB (Note 2)	
Conversion mode	A-D conversion mode,comparator mode			
Operation mode	Single mode, scan mode			
Scan mode	Single -shot scan mode, continuous scan mode			
Conversion start trigger	Software start Started by setting A-D conversion start bit to 1			
	Hardware start A-D0 converter: Input to external pin TIN16, underflow of TOM0_6, enable event to TOM0_0–7 (Note 3), end of A-D1 conversion A-D1 converter: Input to external pin TIN16, underflow of TOM0_6, underflow to TOM1_6, end of A-D0 conversion			
Conversion rate f(BCLK) : Internal peripheral clock operating frequency (Note 4)	During single mode	Low speed mode	Normal	299 × 1/ f (BCLK)
			Double speed	173 × 1/ f (BCLK)
		High-speed mode	× 2 speed	131 × 1/ f (BCLK)
	(Shortest time)		× 4 speed	89 × 1/ f (BCLK)
	During comparator mode	Low speed mode	Normal	47 × 1/ f (BCLK)
			Double speed	29 × 1/ f (BCLK)
		High-speed mode	× 2 speed	23 × 1/ f (BCLK)
	(Shortest time)		× 4 speed	7 × 1/ f (BCLK)
Interrupt request generation	When A-D conversion is finished, when comparate operation is finished, when single-shot scan is finished, or when one cycle of continuous scan is finished			
DMA transfer request generation	When A-D conversion is finished, when comparate operation is finished, when single-shot scan is finished, or when one cycle of continuous scan is finished			

Note 1: The nonlinearity error is a deviation from the ideal conversion characteristic after offset and full-scale errors have been adjusted to 0.
Note 2: This indicates the accuracy of A-D conversion with respect to the input signal from the analog input-only pin.
Note 3: There are following sources of trigger.
TID0 overflow/underflow, TOM0_7 underflow, and input to external pin TIN18
Note 4: When input clock (XIN) = 10 MHz, f(BCLK) = 20 MHz.



Note: The AD0IN8-AD0IN15 pins are shared with input/output ports and internal peripheral I/O input/output pins.

Figure 13. Block Diagram of the A-D0 Converter



Note: The AD1IN4-AD1IN15 pins are shared with input/output ports and internal peripheral I/O input/output pins.

Figure 14. Block Diagram of the A-D1 Converter

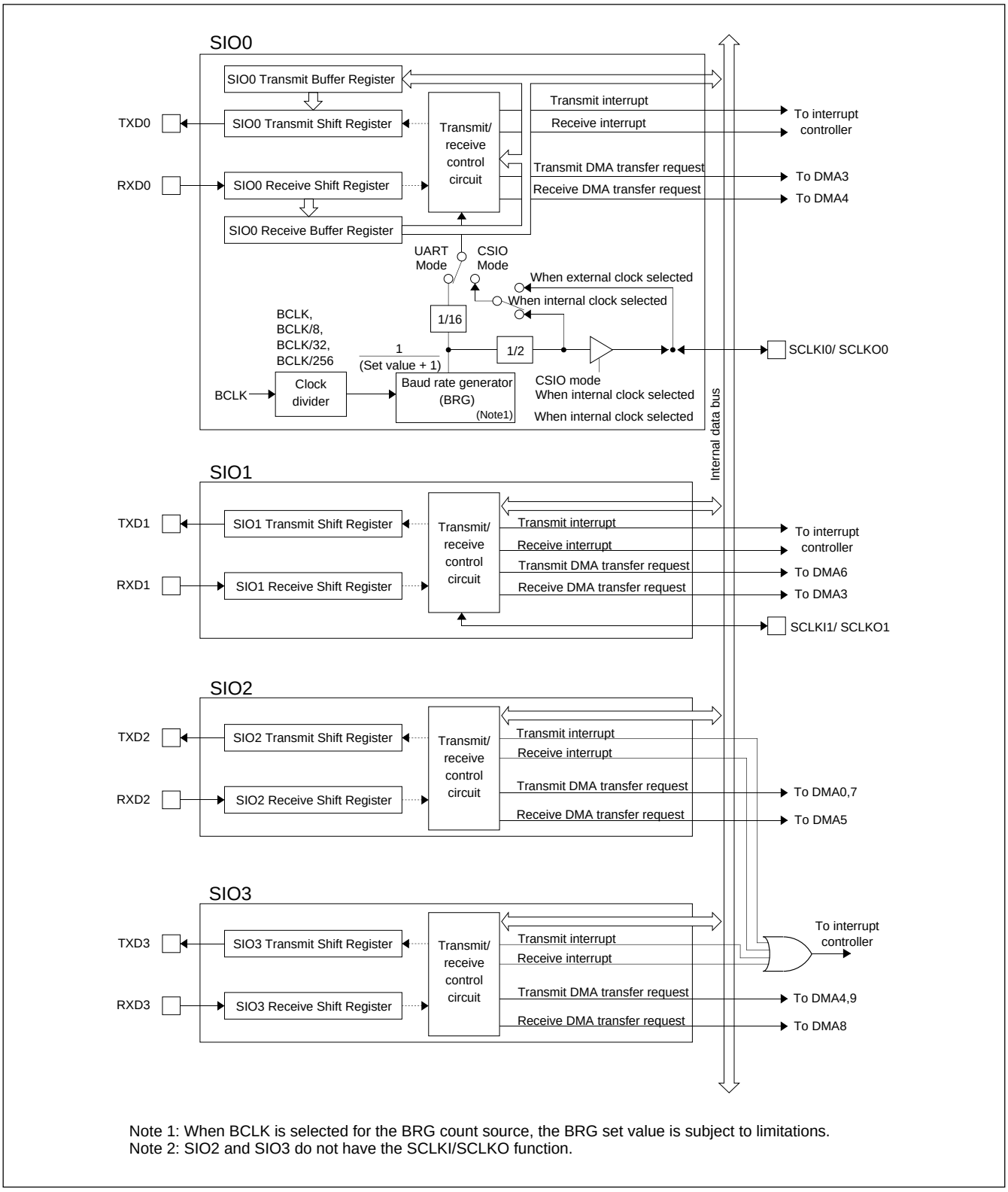
8-channel High-speed Serial I/Os

The microcomputer contains eight channels of serial I/Os consisting of four channels that can be set for CSIO mode (clock-synchronized serial I/O) or UART mode (asynchronous serial I/O) and four other channels that can only be set for UART mode.
The SIO has the function to generate a DMA transfer request when data reception is completed or the transmit register becomes empty, and is capable of high-speed serial communication without causing any additional CPU load.

Table 8. Outline of the Serial I/O

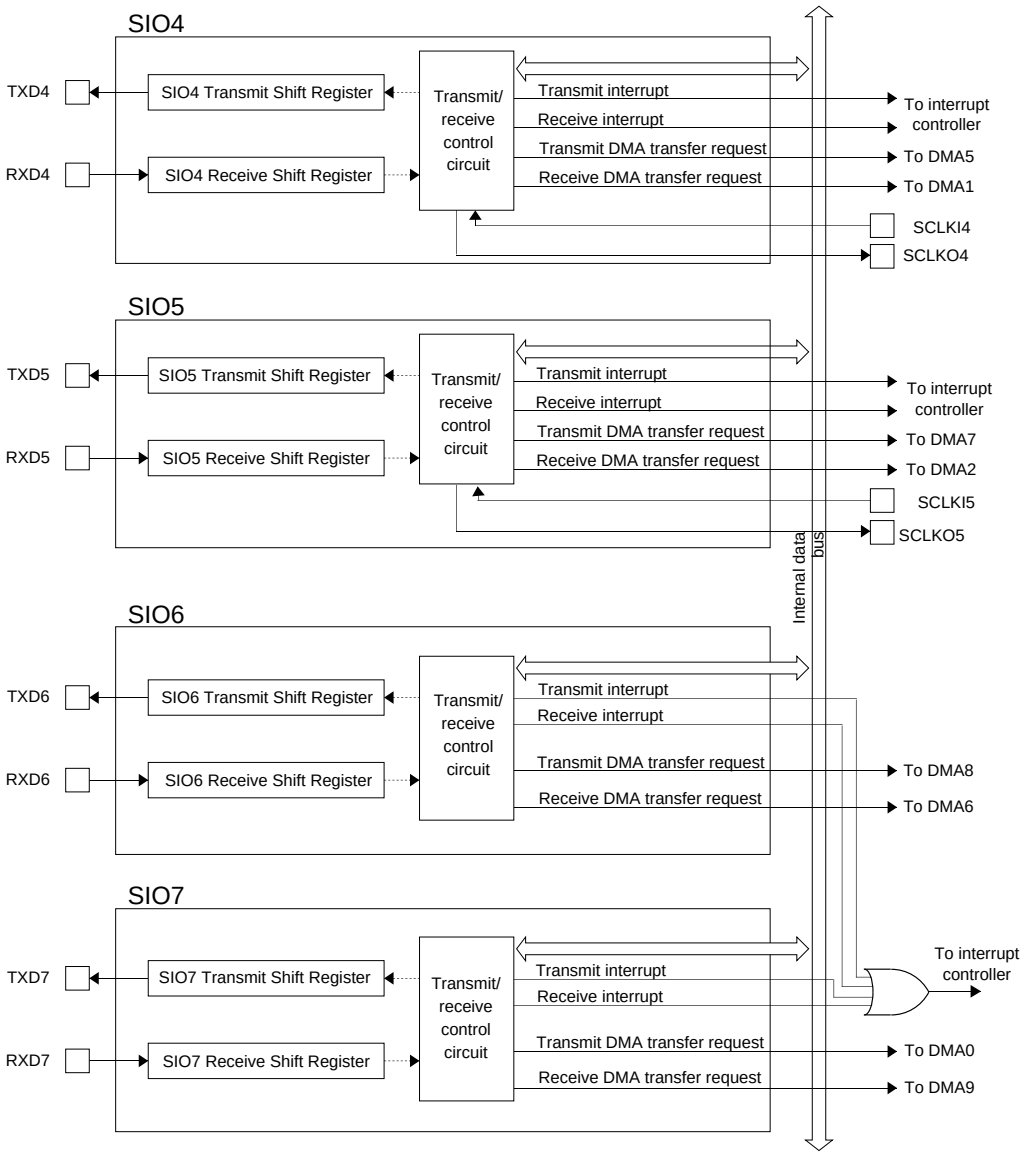
Item	Content		
Number of channels	CSIO/UART: 4 channels (SIO0,SIO1,SIO4,SIO5)		
	UART only : 4 channels (SIO2,SIO3,SIO6,SIO7)		
Clock	During CSIO mode : Internal clock / external clock, selectable (Note1)		
	During UART mode: Internal clock only		
Transfer mode	Transmit half-duplex, receive half-duplex, transmit/receive full-duplex		
BRG count sourcef	(BCLK), f(BCLK)/8, f(BCLK)/32, f(BCLK)/256 (When internal clock is selected) (Note2)		
Data format	CSIO mode:	Data length = Fixed to 8 bits	
		Order of transfer = Fixed to LSB first	
	UARTmode:	Start bit = 1 bit	
		Character length = 7, 8, or 9 bits	
		Parity bit = With or without (even/odd selectable)	
		Stop bit = 1 or 2 bits	
		Order of transfer = Fixed to LSB first	
Baud rate	CSIO mode: 190 bits per second to 2 Mbits per second (when operating with f(BCLK) = 20 MHz)		
	UARTmode: 23 bits per second to 196 Kbits per second (when operating with f(BCLK) = 20 MHz)		
Error detection	CSIO mode:	Overrun error only	
	UARTmode:	Overrun, parity, and framing errors	
		(The error-sum bit indicates which error has occurred)	
Fixed cycle clock output function	When SIO0, SIO1, SIO4, or SIO5 is in UART mode, this function outputs a 1/2 BRG clock from the SCLK pin.		

Note 1: During CSIO mode, the maximum input frequency of an external clock is f(BCLK) divided by 16.
Note 2: When f(BCLK) is selected for the BRG count source, the BRG set value is subject to limitations.



Note 1: When BCLK is selected for the BRG count source, the BRG set value is subject to limitations.
Note 2: SIO2 and SIO3 do not have the SCLKI/SCLKO function.

Figure 15. Block Diagram of the Serial I/O (1/2)



Note : SIO6 and SIO7 do not have the SCLKI/SCLKO function.

Figure 16. Block Diagram of the Serial I/O (2/2)

CAN Module

The microcomputer contains two Full CAN modules compliant with CAN Specification V2.0B (CAN0 and CAN1), each of which has 16-channel message slots and three mask registers.

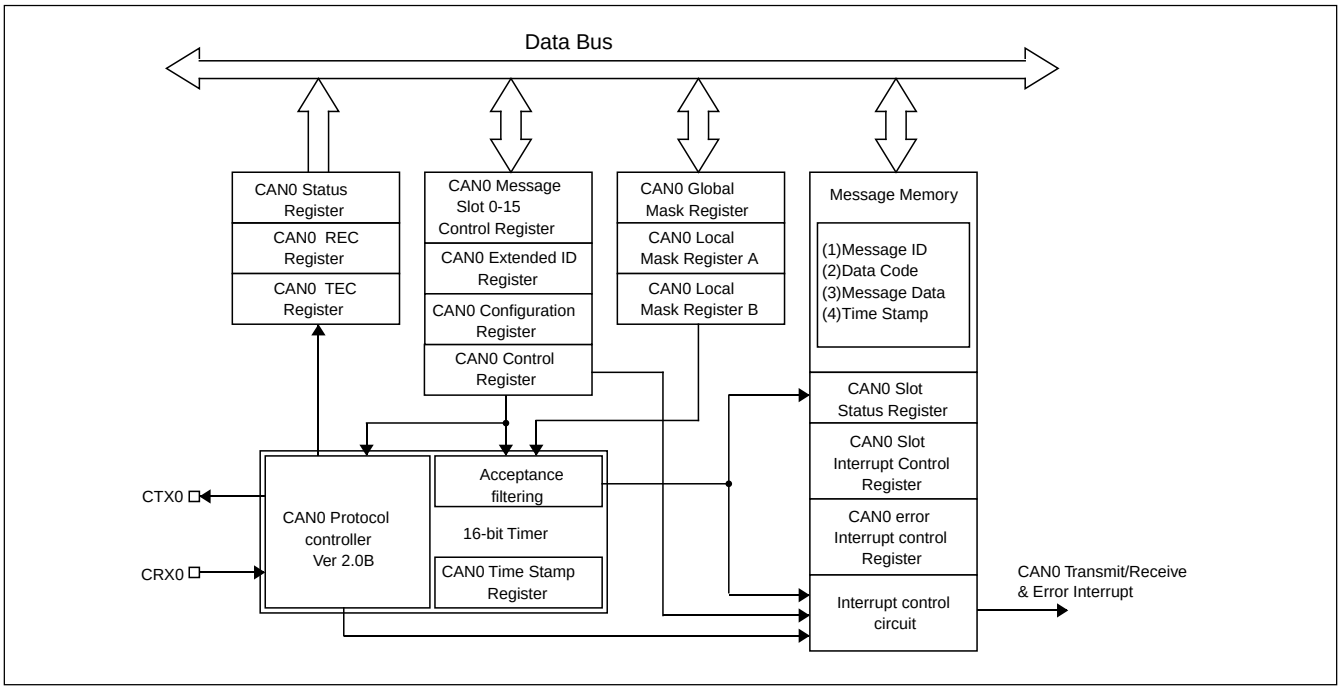


Figure 17. Block Diagram of the CAN0 Module

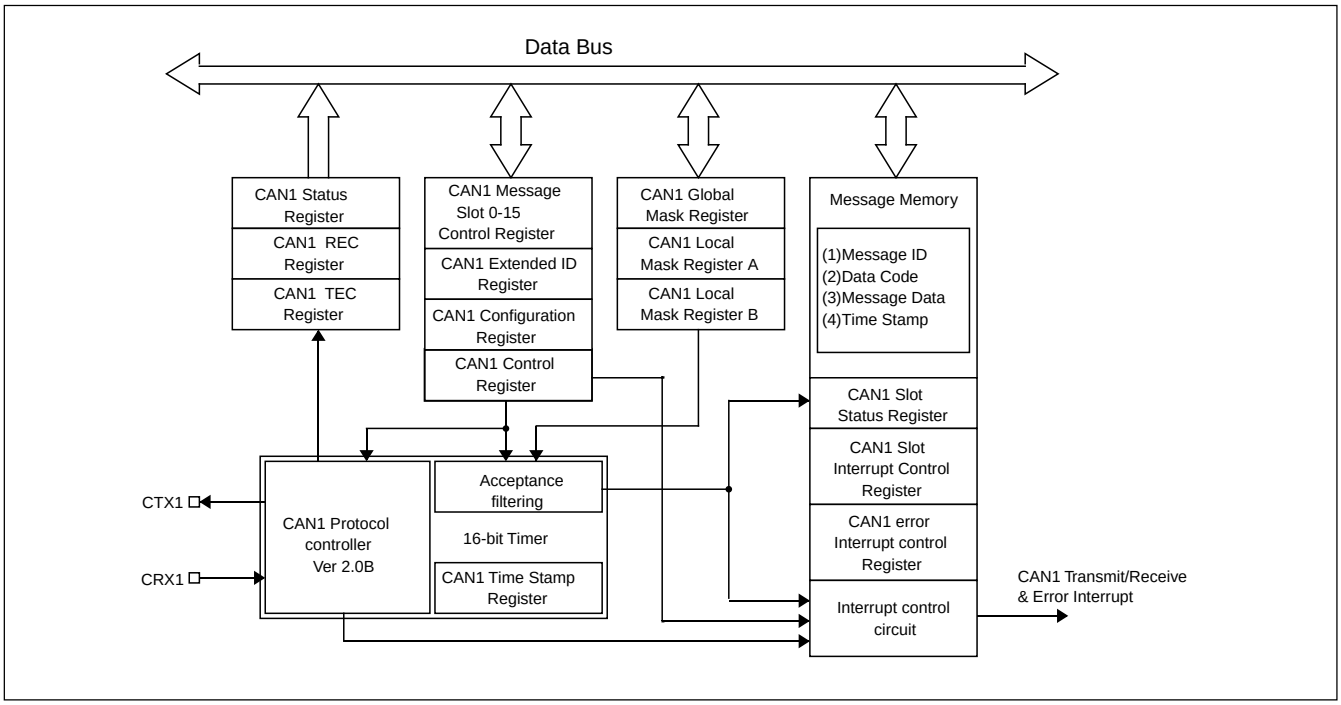


Figure 18. Block Diagram of the CAN1 Module

PD Interface Module

The microcomputer contains eight-channel event counters which can be used as a dedicated interface circuit for PD (Phase Digital) sensors. When used in combination with PD sensors, this interface module can perform the necessary predictive arithmetic operation during position detection at high speed.

Note: A separate external circuit is required before this interface module can be used in combination with PD sensors.

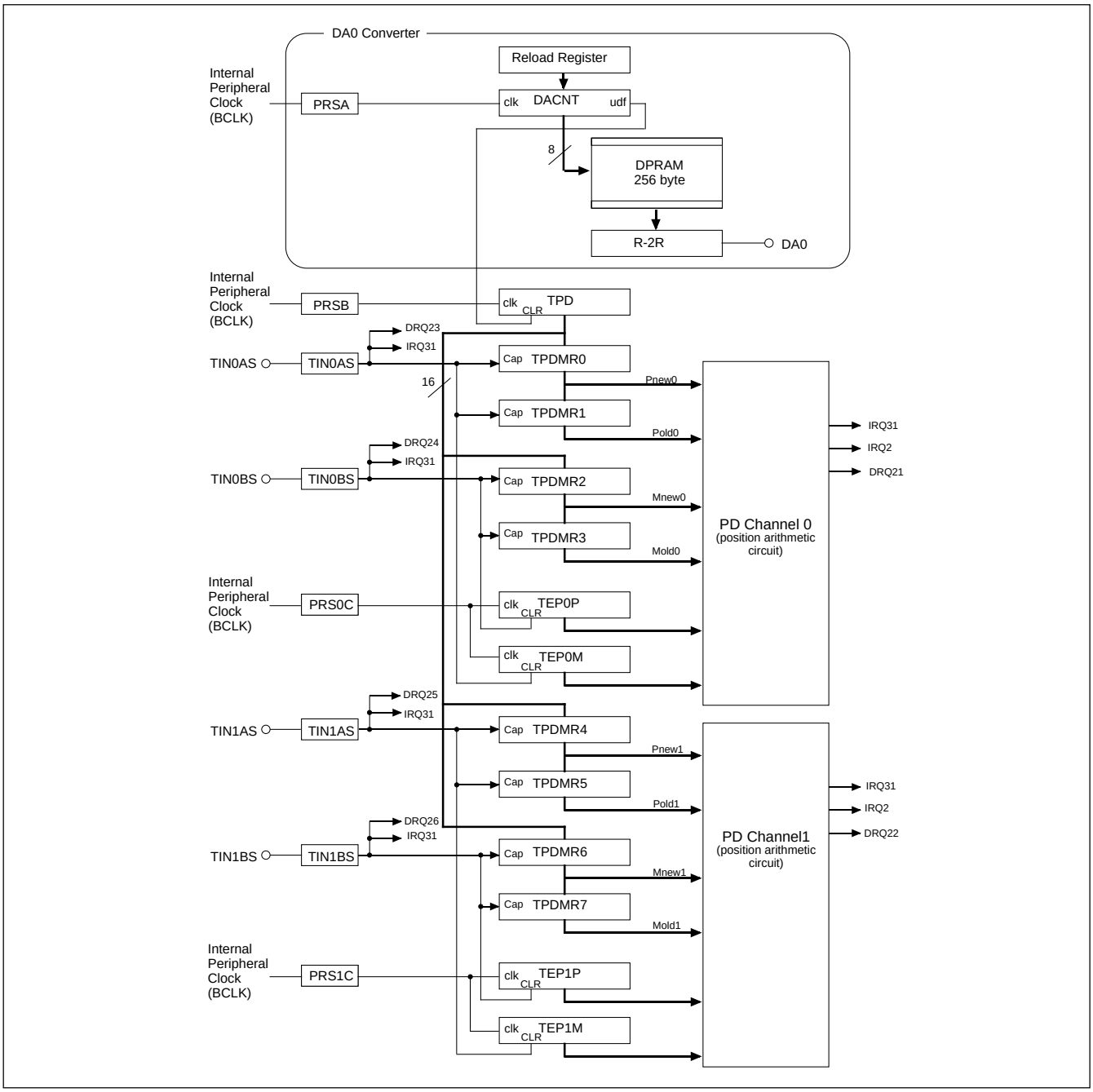


Figure 19. Block Diagram of the PD Interface Module

D-A Converters

The microcomputer contains two 8-bit D-A converters (D-A0 and D-A1 converters). There are two D-A conversion modes: single mode and continuous mode (D-A1 converter only).

Single mode: In this mode, the D-A converter outputs an analog value corresponding to the value set in the D-A conversion register.

Continuous mode: In this mode, the D-A converter outputs the values set in D-A data registers n (n = 0–255) after successively converting them into analog quantities.

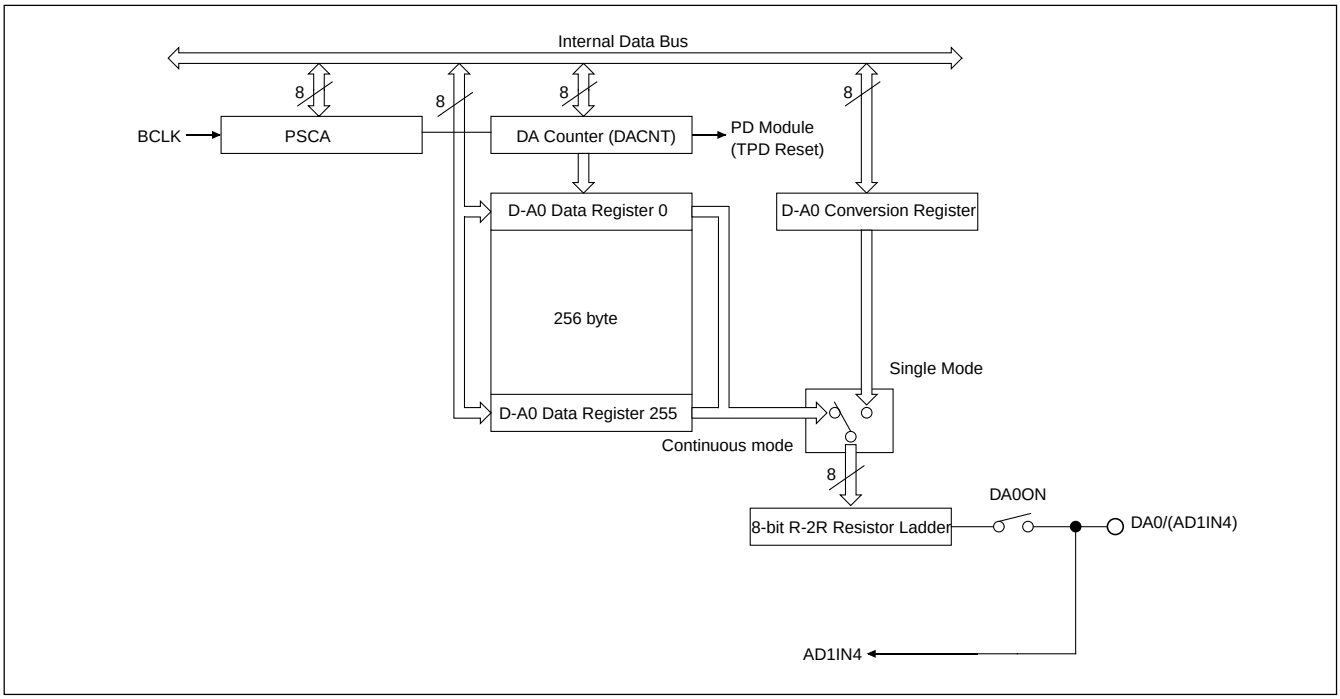


Figure 20. Block Diagram of the D-A0 Converter

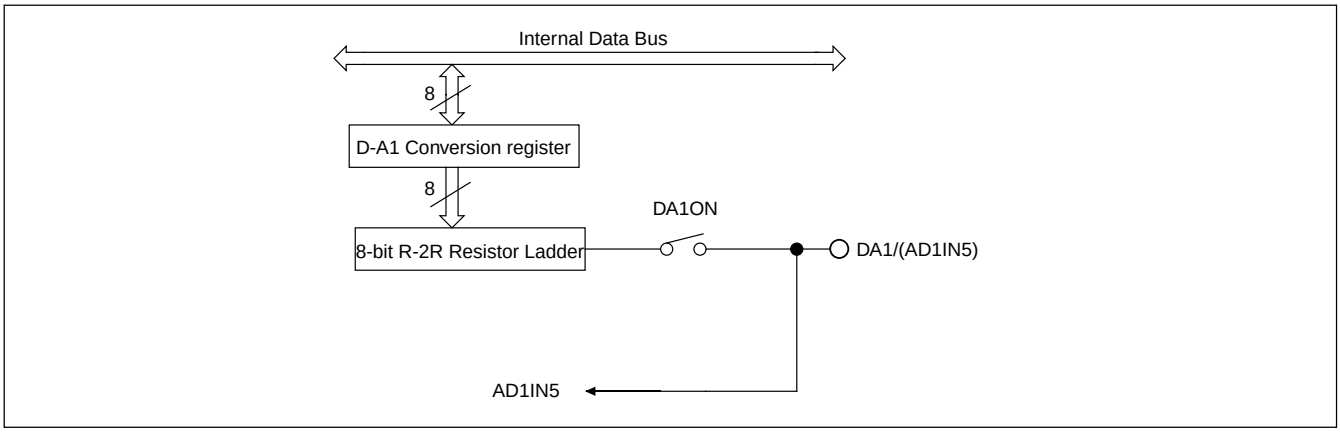


Figure 21. Block Diagram of the D-A1 Converter

8-level Interrupt Controller

The Interrupt Controller controls interrupt requests from each internal peripheral I/O (31 sources) by using eight priority levels assigned to each interrupt source, including interrupts disabled. In addition to these interrupts, it handles System Break Interrupt (SBI), Reserved Instruction Exception (RIE), and Address Exception (AE) as nonmaskable interrupts.

Wait Controller

The Wait Controller supports access to external devices.
For access to an external extended area of up to 1 Mbytes (during external extended or processor mode), the Wait Controller controls bus cycle extension by inserting one to four wait cycles or using external $\overline{\text{WAIT}}$ signal input.

Realtime Debugger (RTD)

The Realtime Debugger (RTD) provides a function for accessing directly from the outside to the internal RAM. It uses a dedicated clock-synchronized serial I/O to communicate with the outside.
Use of the RTD communicating via dedicated serial lines allows the internal RAM to be read out and rewritten without having to halt the CPU.

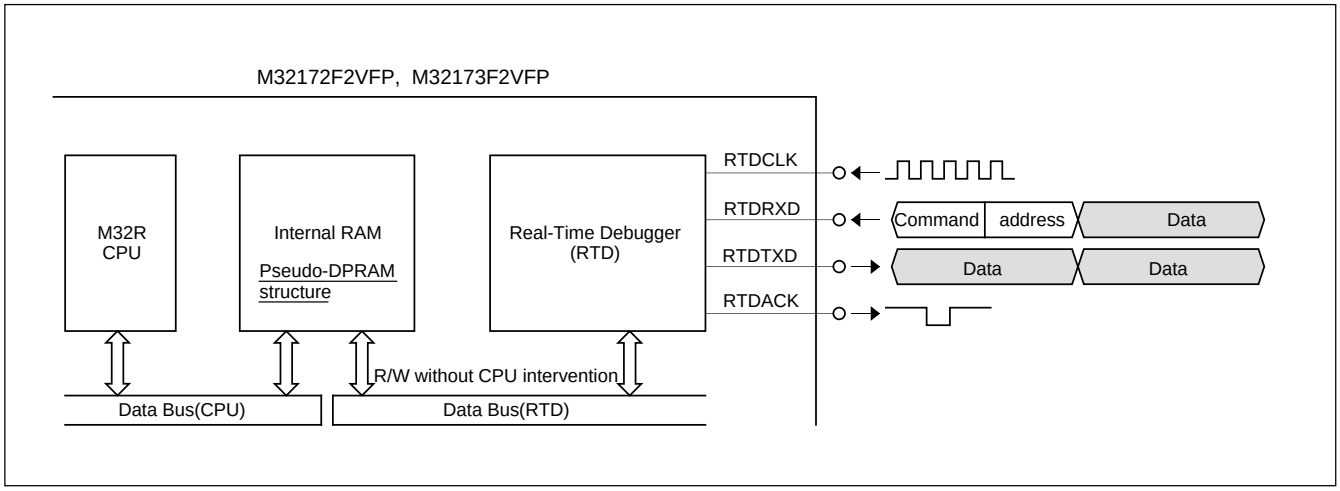


Figure 22. Conceptual Diagram of the Realtime Debugger (RTD)

CPU Instruction Set

The M32R employs a RISC architecture, supporting a total of 83 discrete instructions.

(1) Load/store instructions

Perform data transfer between memory and registers.

LD	Load
LDB	Load byte
LDUB	Load unsigned byte
LDH	Load halfword
LDUH	Load unsigned halfword
LOCK	Load locked
ST	Store
STB	Store byte
STH	Store halfword
UNLOCK	Store unlocked

(2) Transfer instructions

Perform register to register transfer or register to immediate transfer.

LD24	Load 24-bit immediate
LDI	Load immediate
MV	Move register
MVFC	Move from control register
MVTC	Move to control register
SETH	Set high-order 16-bit

(3) Branch instructions

Used to change the program flow.

BC	Branch on C-bit
BEQ	Branch on equal
BEQZ	Branch on equal zero
BGEZ	Branch on greater than or equal zero
BGTZ	Branch on greater than zero
BL	Branch and link
BLEZ	Branch on less than or equal zero
BLTZ	Branch on less than zero
BNC	Branch on not C-bit
BNE	Branch on not equal
BNEZ	Branch on not equal zero
BRA	Branch
JL	Jump and link
JMP	Jump
NOP	No operation

(4) Arithmetic/logic instructions

Perform comparison, arithmetic/logic operation, multiplication/division, or shift between registers.

• Comparison

CMP	Compare
CMPI	Compare immediate
CMPU	Compare unsigned
CMPUI	Compare unsigned immediate

• Logical operation

AND	AND
AND3	AND 3-operand
NOT	Logical NOT
OR	OR
OR3	OR 3-operand
XOR	Exclusive OR
XOR3	Exclusive OR 3-operand

• Arithmetic operation

ADD	Add
ADD3	Add 3-operand
ADDI	Add immediate
ADDV	Add (with overflow checking)
ADDV3	Add 3-operand
ADDX	Add with carry
NEG	Negate
SUB	Subtract
SUBV	Subtract (with overflow checking)
SUBX	Subtract with borrow

• Multiplication/division

DIV	Divide
DIVU	Divide unsigned
MUL	Multiply
REM	Remainder
REMU	Remainder unsigned

• Shift

SLL	Shift left logical
SLL3	Shift left logical 3-operand
SLLI	Shift left logical immediate
SRA	Shift right arithmetic
SRA3	Shift right arithmetic 3-operand
SRAI	Shift right arithmetic immediate
SRL	Shift right logical
SRL3	Shift right logical 3-operand
SRLI	Shift right logical immediate

(5) Instructions for the DSP function

Perform 32 bit × 16 bit or 16 bit × 16 bit multiplication or sum-of-products calculation. These instructions also perform rounding of the accumulator data or transfer between accumulator and general-purpose register.

MACHI	Multiply-accumulate high-order halfwords
MACLO	Multiply-accumulate low-order halfwords
MACWHI	Multiply-accumulate word and high-order halfword
MACWLO	Multiply-accumulate word and low-order halfword
MULHI	Multiply high-order halfwords
MULLO	Multiply low-order halfwords
MULWHI	Multiply word and high-order halfword
MULWLO	Multiply word and low-order halfword
MVFACHI	Move from accumulator high-order word
MVFACLO	Move from accumulator low-order word
MVFACMI	Move from accumulator middle-order word
MVTACHI	Move to accumulator high-order word
MVTACLO	Move to accumulator low-order word
RAC	Round accumulator
RACH	Round accumulator halfword

(6) EIT related instructions

Start trap or return from EIT processing.

RTE	Return from EIT
TRAP	Trap

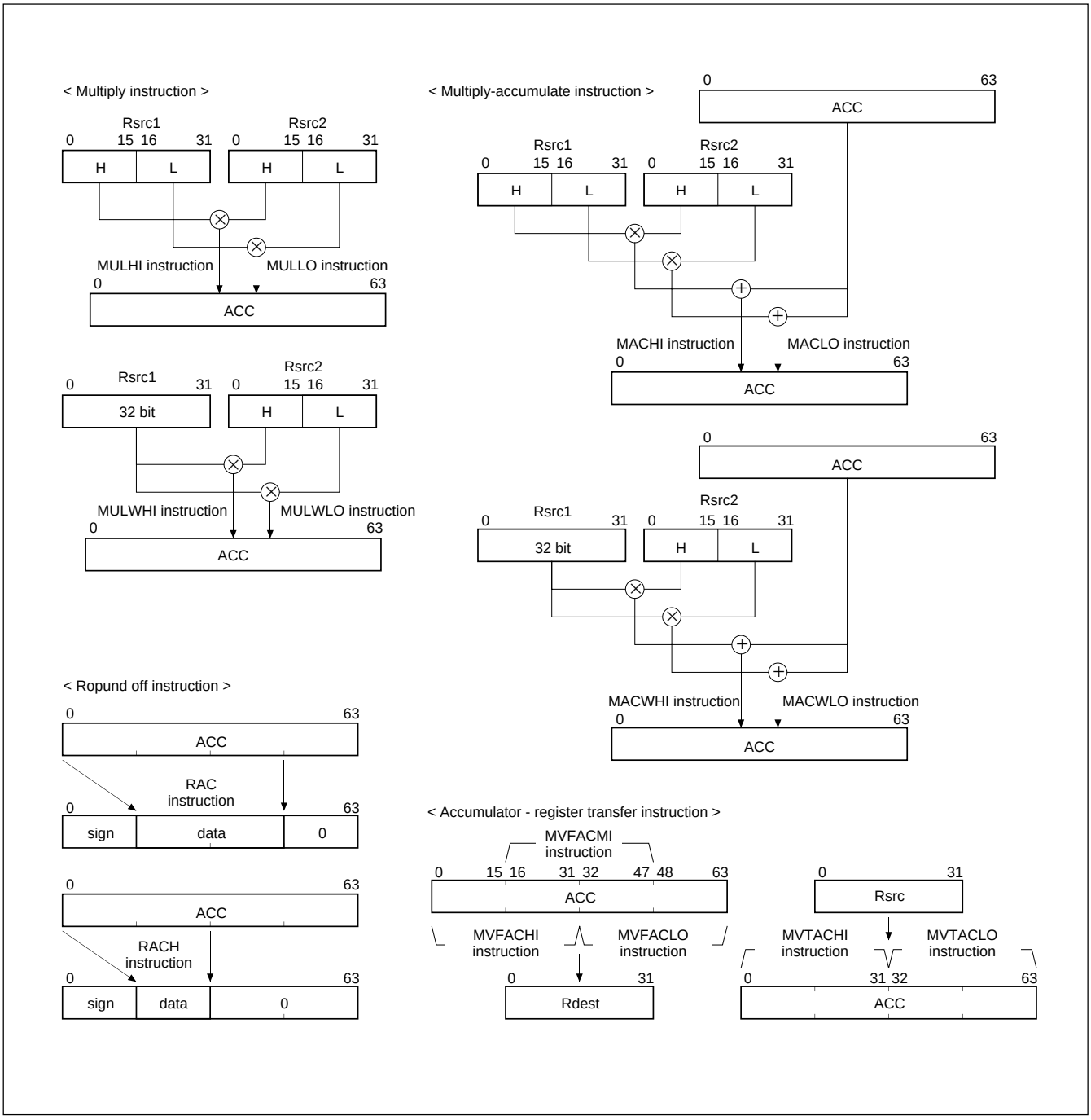


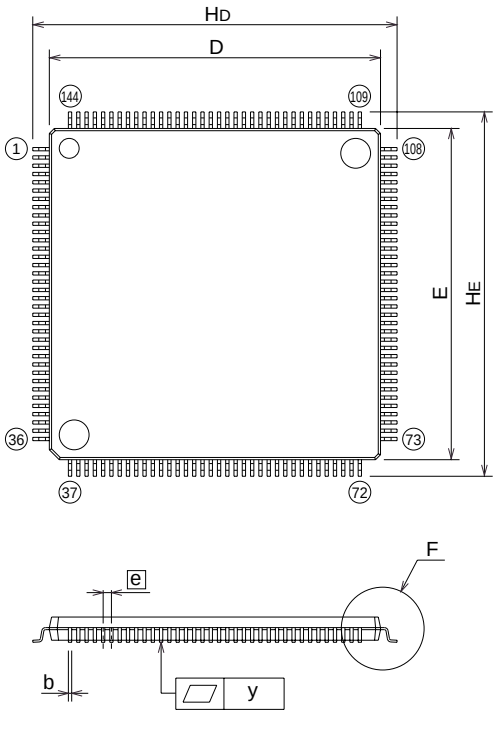
Figure 23. Instructions for the DSP Function

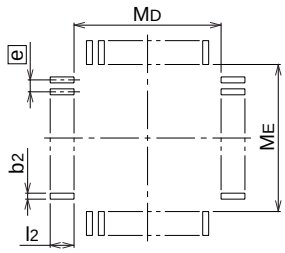
Package Dimensions Diagram

144P6Q-A

Plastic 144pin 20×20mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP144-P-2020-0.50	–		Cu Alloy





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A1	0.05	0.125	0.2
A2	–	1.4	–
b	0.17	0.22	0.27
c	0.105	0.125	0.175
D	19.9	20.0	20.1
E	19.9	20.0	20.1
e	–	0.5	–
HD	21.8	22.0	22.2
HE	21.8	22.0	22.2
L	0.35	0.5	0.65
L1	–	1.0	–
y	–	–	0.1
θ	0°	–	8°
b2	–	0.225	–
l2	1.0	–	–
MD	–	20.4	–
ME	–	20.4	–

MEMO

Mitsubishi Microcomputers

M32172F2VFP
M32173F2VFP

SINGLE-CHIP 32-BIT CMOS MICROCOMPUTER

Renesas Technology Corp.
Nippon Bldg.,6-2,Otemachi 2-chome,Chiyoda-ku,Tokyo,100-0004 Japan

New publication, effective Nov. 2000.
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