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HA16117F Series

CMOS Watchdog Timer

ADE-204-018B (Z)
Rev. 2
Dec. 2000

Description

The HA16117F Series of ICs make a micro-processor (MPU) system fail-safe by monitoring its power supply to detect voltage drops, and monitoring a P-RUN (program running) pulse to detect system crashes. Also referred to as watchdog timers, these devices are essential in systems that aim for high levels of crash protection. Fabricated by a CMOS process, they consume little power and are ideally suited for battery-operated systems.

These ICs are available in versions for industrial and communications equipment and automotive applications, as well as for consumer products.

Functions

- Power-on reset
  - Sends a $\overline{\text{RES}}$ signal to the MPU for a fixed time at power-on
- Watchdog timer (WDT)
  - Monitors a P-RUN signal from the MPU and sends the MPU a $\overline{\text{RES}}$ signal if P-RUN departs from a set frequency range
- Auto-reset
  - Outputs $\overline{\text{RES}}$ signals to the MPU at clocked intervals while P-RUN remains abnormal
- Supply voltage supervision
  - Outputs a low $\overline{\text{RES}}$ signal if the supply voltage (same as the MPU's V_{CC}) falls below a low threshold level (V_{TL}). The threshold differs for different ICs in the series, allowing designers to choose an IC matching system requirements (see ordering information)

Features

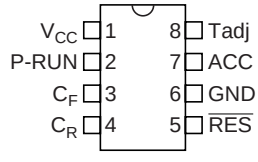
- Low power consumption : Operating (ACC pin low) = 0.5 mW (Typ)
  : Standby (ACC pin high) = 0.2 mW (Typ)
- Watchdog timer on/off control by ACC input signal
- Independent auto-reset high and low times (t_{RH} and t_{RL})
- Watchdog monitoring by frequency filtering (independent of duty cycle)
- High-precision low voltage detection (±2%)
- Space- and weight-saving 8-pin SOP package

Ordering Information

The HA16117F Series includes three ICs with different low threshold levels (V_{TL}).

Type No.	Low Threshold Voltage (V_{TL})
HA16117FPA/FPAJ	4.4 V Typ
HA16117FPB/FPBJ	4.2 V Typ
HA16117FPC/FPCJ	4.0 V Typ

Pin Arrangement



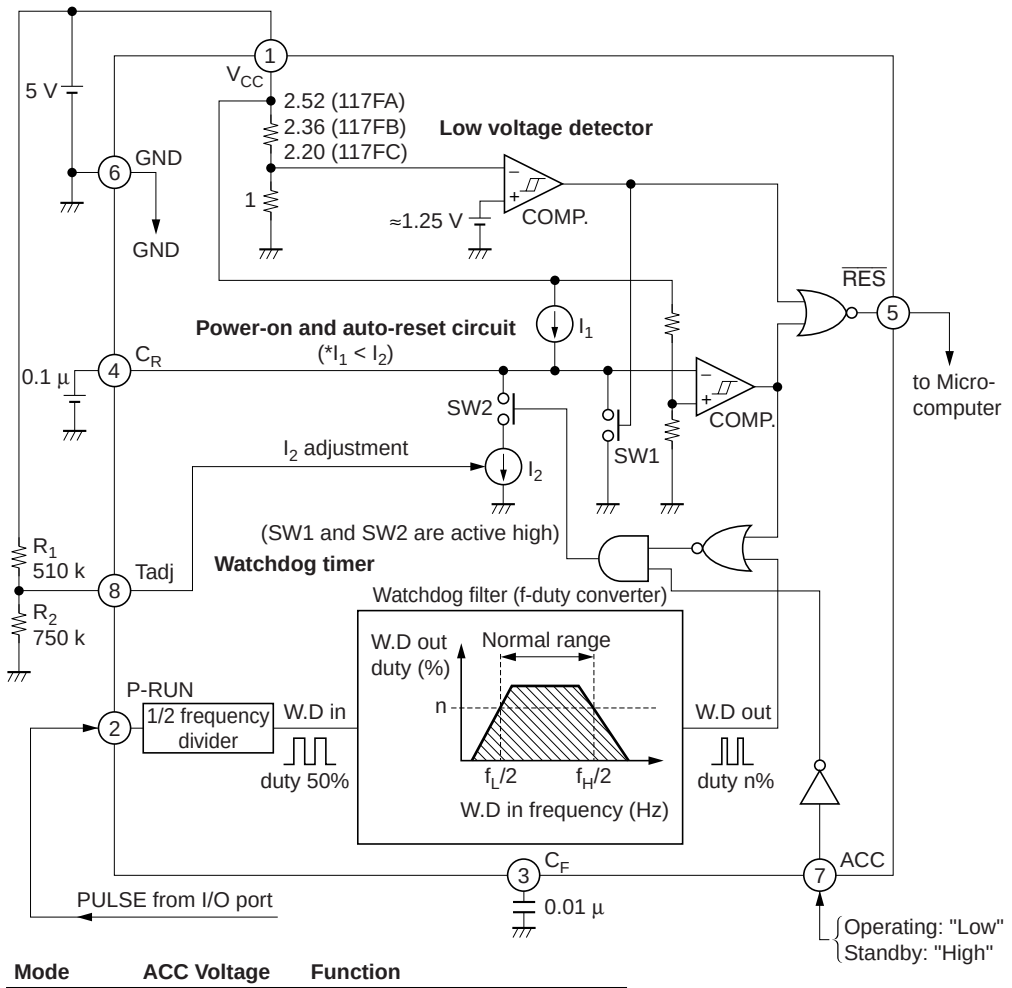
(Top view)

Pin Description

Pin No.	Symbol	Function
1	V_{CC}	Power supply voltage input
2	P-RUN	Watchdog timer (WDT) input
3	C_F	Connected capacitor C_F determines WDT filter characteristic (normal frequency range)
4	C_R	Connected capacitor C_R determines t_{ON} for power-on reset and t_{OFF}, t_{RH}, and t_{RL} for auto-reset
5	$\overline{RES}$	Reset signal output from WDT and voltage supervision circuits
6	GND	Ground
7	ACC	WDT on/off control input (on when ACC is low)
8	Tadj *	For adjusting t_{RH} and t_{OFF} (divide V_{CC} to get the adjustment voltage)

Note: The low-voltage threshold cannot be modified by changing the external resistors connected to the Tadj pin.

Block Diagram



Mode	ACC Voltage	Function
Operating	Low	Low voltage detection and WDT
Standby	High	Low voltage detection

Note: The power-on reset circuit operates in both operating and standby modes.

The HA16117F consists of a low voltage detector, power-on and auto-reset circuit, and watchdog timer.

Low Voltage Detector

Uses a reference voltage source (≈ 1.25 V) and high-precision comparator to detect drops in the supply voltage.

Power-On and Auto-Reset Circuit

Generates the $\overline{RES}$ waveform, using a multivibrator consisting of a current source I_1 that charges the external capacitor C_R, a current source I_2 that discharges C_R, and a comparator.

Watchdog Timer

Reshapes the P-RUN signal (programming-running pulse) from the MPU to obtain a 50% duty cycle, then converts frequency to duty cycle in the watchdog filter (WD filter).

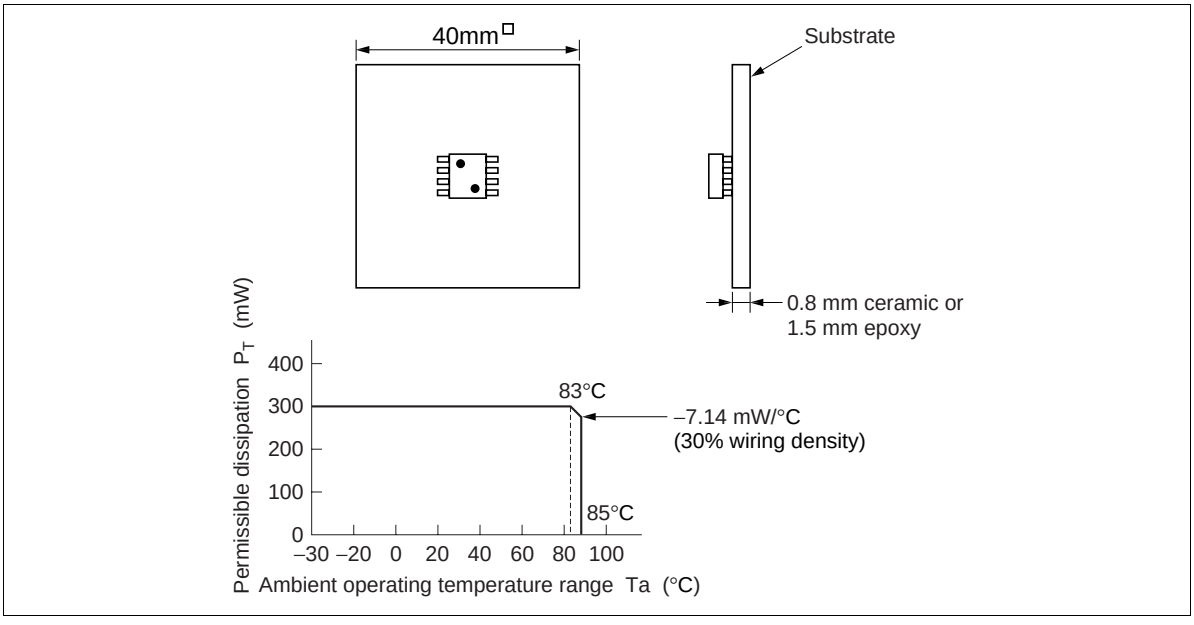
The watchdog filter is a bandpass filter. The duty cycle of the filter output is highest in the normal frequency range of P-RUN.

The watchdog filter output controls I_2 in the multivibrator, the higher the duty cycle of the watchdog filter output, the shorter the time during which I_2 discharges C_R. If the duty cycle is high enough then C_R is held at a high potential, preventing the multivibrator from firing, and the $\overline{RES}$ output remains high.

Absolute Maximum Ratings (Ta = 25°C)

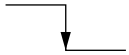
Item	Symbol	Ratings		Unit
		HA16117FPA/FPB/FPC	HA16117FPAJ/FPBJ/FPCJ	
Power supply voltage	V_{CC}	–0.3 to +14	–0.3 to +14	V
P-RUN input voltage	V_P	V_{CC}	V_{CC}	V
ACC input voltage	V_{ACC}	14	14	V
RES output current	I_{RES}	10	10	mA
Permissible dissipation *[1]	P_T	300	300	mW
Operating temperature range	Topr	–30 to +85	–40 to +85	°C
Storage temperature	Tstg	–55 to +125	–55 to +125	°C

Note: 1. This is the value when mounted on a glass epoxy substrate with 30% wiring density, up to an ambient temperature of 83°C. Above that temperature, derate by 7.14 mW/°C.

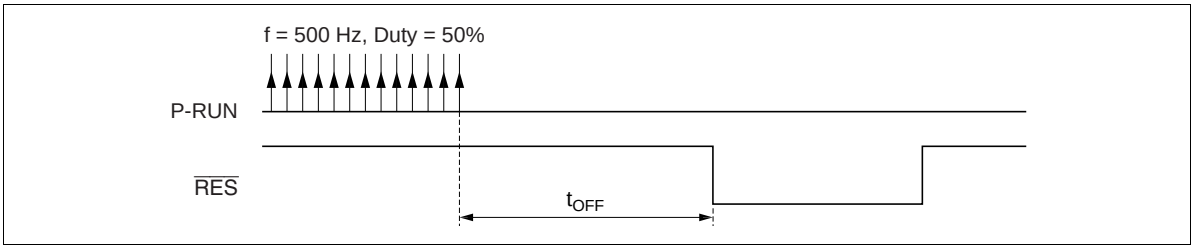


Electrical Characteristics

(V_{CC} = 5 V, Ta = 25°C, C_F = 0.01 µF, C_R = 0.1 µF, R_1 = 510 kΩ, R_2 = 750 kΩ)

Item			Symbol	Min	Typ	Max	Unit	Test Conditions
General	Operating supply current		I_{CC1}	—	100	—	µA	V_{ACC} = 0 V, $f_{P\text{-}RUN}$ = 100 Hz
			I_{CC2}	—	200	600	µA	V_{ACC} = 0 V, $f_{P\text{-}RUN}$ = 20 kHz
	Standby supply current		I_{STBY}	—	43	100	µA	V_{ACC} = 12 V
Low voltage detector	Low voltage threshold level	HA16117FPA/FPAJ	V_{TL}	4.3	4.4	4.5	V	When V_{CC} drops 
		HA16117FPB/FPBJ		4.1	4.2	4.3	V	
		HA16117FPC/FPCJ		3.9	4.0	4.1	V	
	Hysteresis width		V_{HYS}	50	100	150	mV	
ACC	Low input voltage		V_{IL1}	—	—	0.8	V	
	High input voltage		V_{IH1}	2.0	—	—	V	
P-RUN input	Low input voltage		V_{IL2}	—	—	0.8	V	
	High input voltage		V_{IH2}	2.0	—	—	V	
WDT	Power-on reset time		t_{ON}	24	40	56	ms	
	Reset-clock off time		t_{OFF} *1	78	130	182	ms	
	Reset low time		t_{RL}	12	20	28	ms	
	Reset high time		t_{RH}	36	60	84	ms	P-RUN pin = 0 V
	Low setup time		t_{SL}	1	—	—	ms	
	High setup time		t_{SH}	—	—	1	ms	
$\overline{RES}$ output	$\overline{RES}$ low voltage		V_{OL}	—	—	0.4	V	I_{OL} = 1 mA
	$\overline{RES}$ high voltage		V_{OH}	—	V_{CC}	—	V	Open
	Reset function starting voltage		V_{RES}	—	0.8	1.4	V	
Constant range	Constant range of R_1 and R_2		K	0.55	0.6	0.8	—	K = R_2 / (R_1 + R_2)
Operating supply voltage range			V_{CCRNG}	V_{TL}	—	6.0	V	

Note: 1. Reset-clock off time t_{OFF} is provided a shown in the under figure.



Timing Waveforms and Functional Description

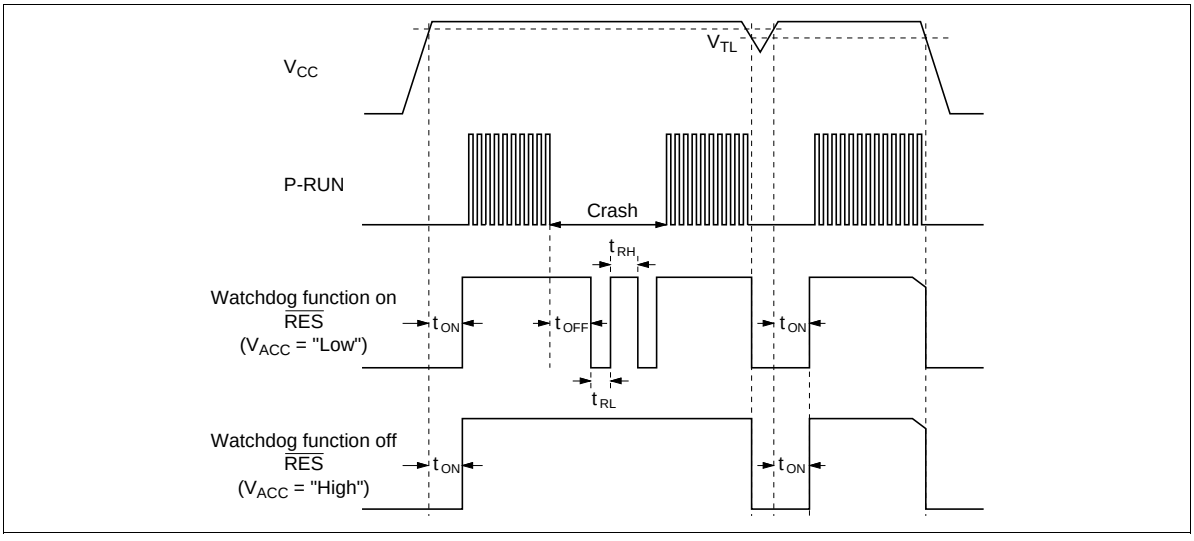


Figure 1 Timing Waveforms

Watchdog On/Off Function

A feature of the HA16117F is that watchdog supervision can be switched on and off. When the watchdog function is switched on, both the supply voltage and

P-RUN input are monitored to detect abnormal conditions. When the watchdog function is switched off (standby mode), only the supply voltage is monitored. Watchdog supervision is switched on and off by the input at the ACC pin (pin 7): Supervision is on when ACC is low, and off when ACC is high.

Many MPUs have a standby mode in which the CPU stops running but memory contents are retained. In standby mode, program execution halts and I/O ports go to the high-impedance state, so there is no need for the watchdog timer to supervise pulse output from an I/O port to detect abnormal conditions. Power can be saved by placing both the MPU and HA16117F in standby mode at the same time. The HA16117F is designed to draw a typical standby current I_{STBY} of only 43 µA Typ when the watchdog function is switched off.

ACC Pin (pin 7) and $\overline{RES}$ Output

When the MPU returns from standby mode to normal operation it generally takes 10 to 200 ms for the clock oscillator in the MPU to stabilize. The $\overline{RES}$ signal is not output during this setup time. After the setup time (t_{SL}) has elapsed, $\overline{RES}$ is output if the P-RUN signal from the MPU is still abnormal.

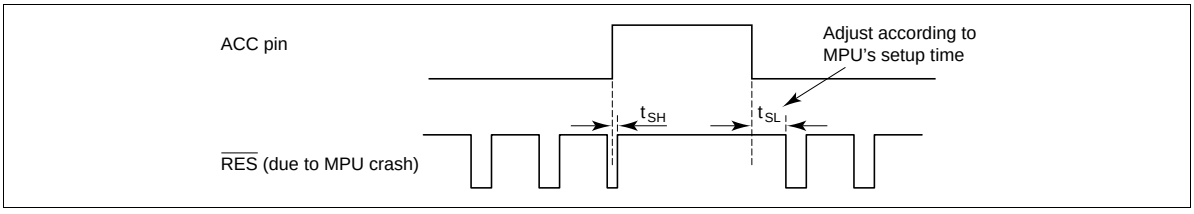


Figure 2 ACC Pin and $\overline{RES}$ Output

Internal Operation and Usage Notes

Figure 3 shows an equivalent circuit of the watchdog timer block with a V_{CC} pin level of 5 V and ACC pin level of 0 V, and the following pages show internal operation timing charts for different P-RUN frequencies. (Descriptions apply to conditions C_F = 0.01 µF, C_R = 0.1 µF, $R_2/(R_1 + R_2)$ = 0.6.)

Operation

The power-on and auto-reset circuit is a multivibrator with timing controlled by C_R charge current I_1 and discharge current I_2. As $I_1 : I_2 \approx 3 : 1$ (Typ design value), when the (WD) (watchdog filter circuit output) on-duty is 25% or above, the C_R pin potential does not fall below 1.6 V. Therefore, (C) in the figure below is fixed low, and $\overline{RES}$ is not output. The (WD) on-duty varies according to the P-RUN frequency. If the frequency is lower or higher than the design value, the (WD) on-duty decreases, and at 25% or below, $\overline{RES}$ is output. Refer to the timing charts on the following pages for an explanation of the operation of the watchdog filter.

Usage Notes

- When the P-RUN frequency reaches 20 kHz or above, t_{OFF} is short (see the timing charts on the following pages). This must be borne in mind in the design stage.
- If the P-RUN frequency fluctuates, $\overline{RES}$ may also be output within the normal detection set frequency (see the timing charts on the following pages).
- Detection frequencies f_H and f_L described in the Data Book are Typ values, and a certain amount of dispersion can be expected. A margin of ±30% or more should be allowed for in the design.

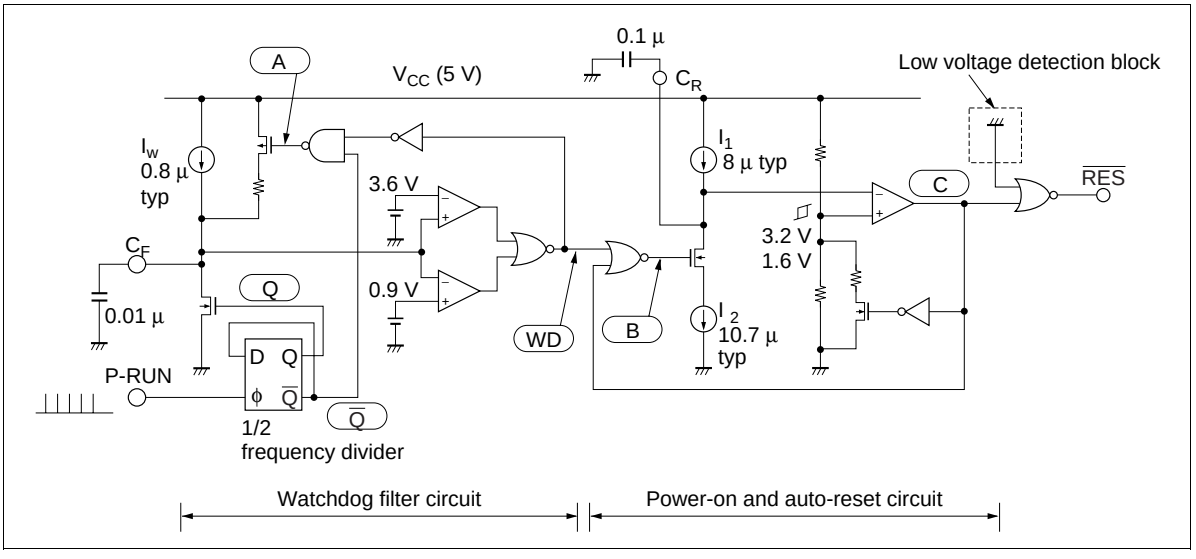
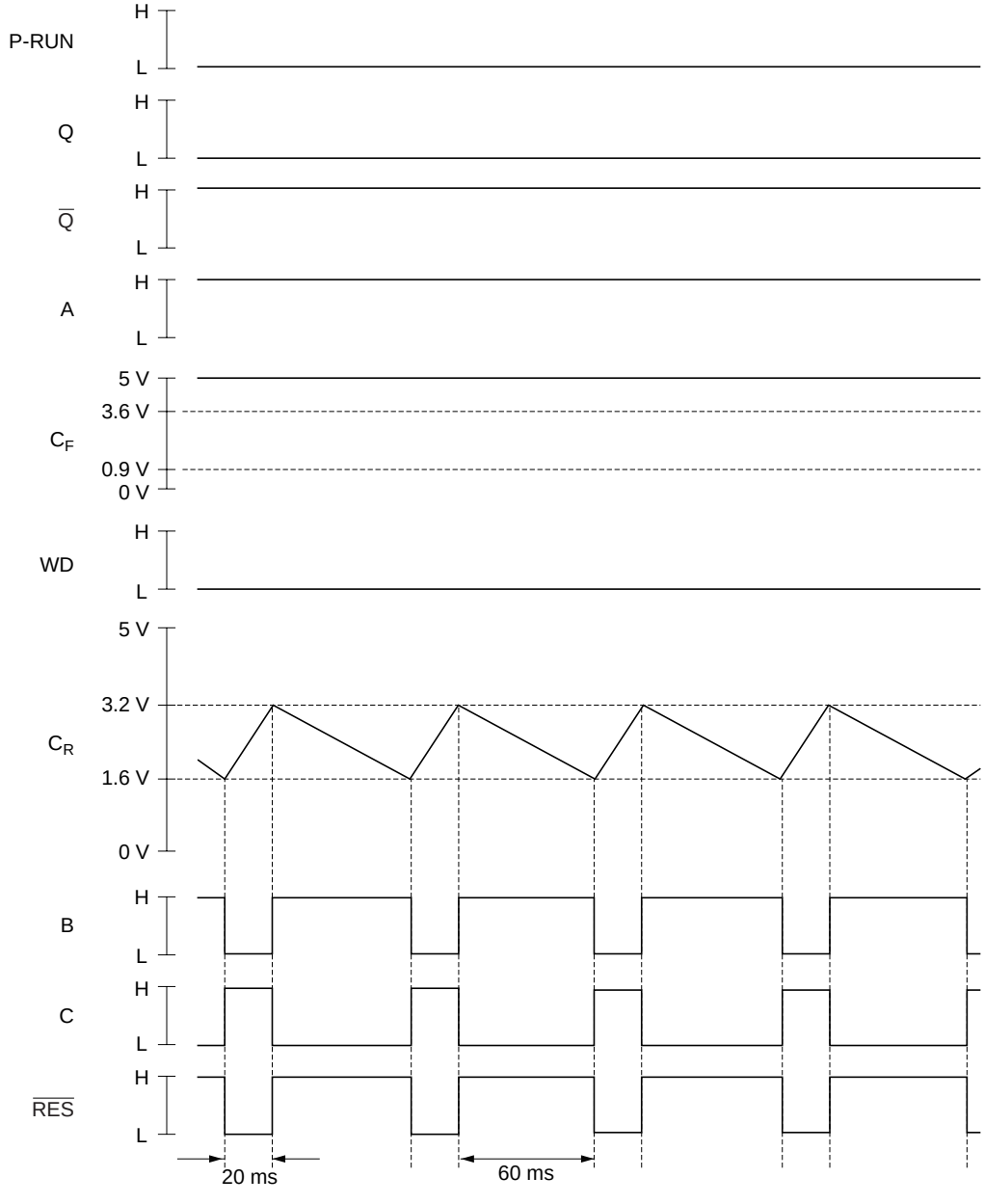


Figure 3 Watchdog Timer Evaliation Circuit

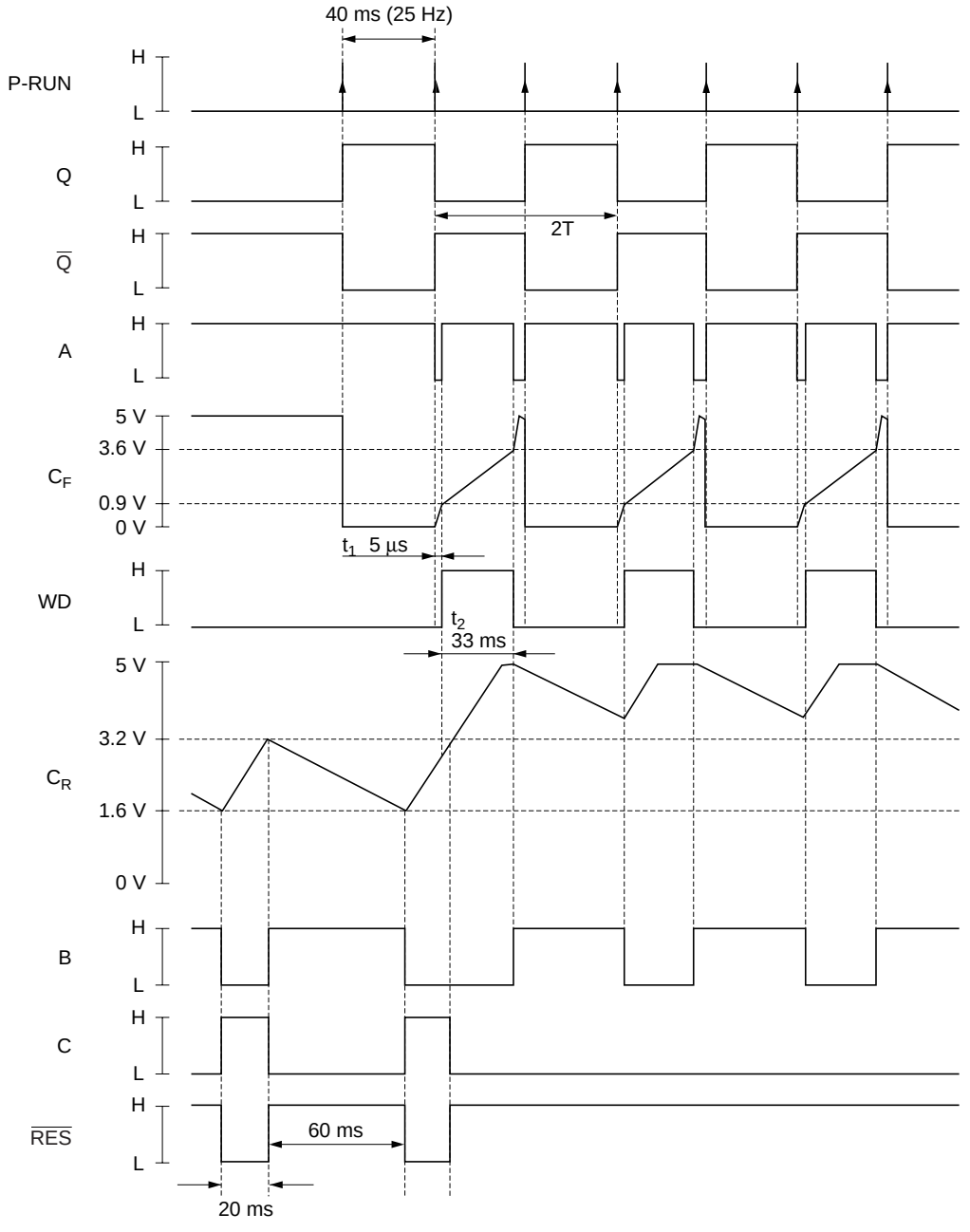
1. When P-RUN signal is not input

The watchdog filter circuit output (WD) is fixed low, so the $\overline{RES}$ signal is output as shown in the figure below in accordance with power-on and auto-reset circuit C_R charge/discharge.



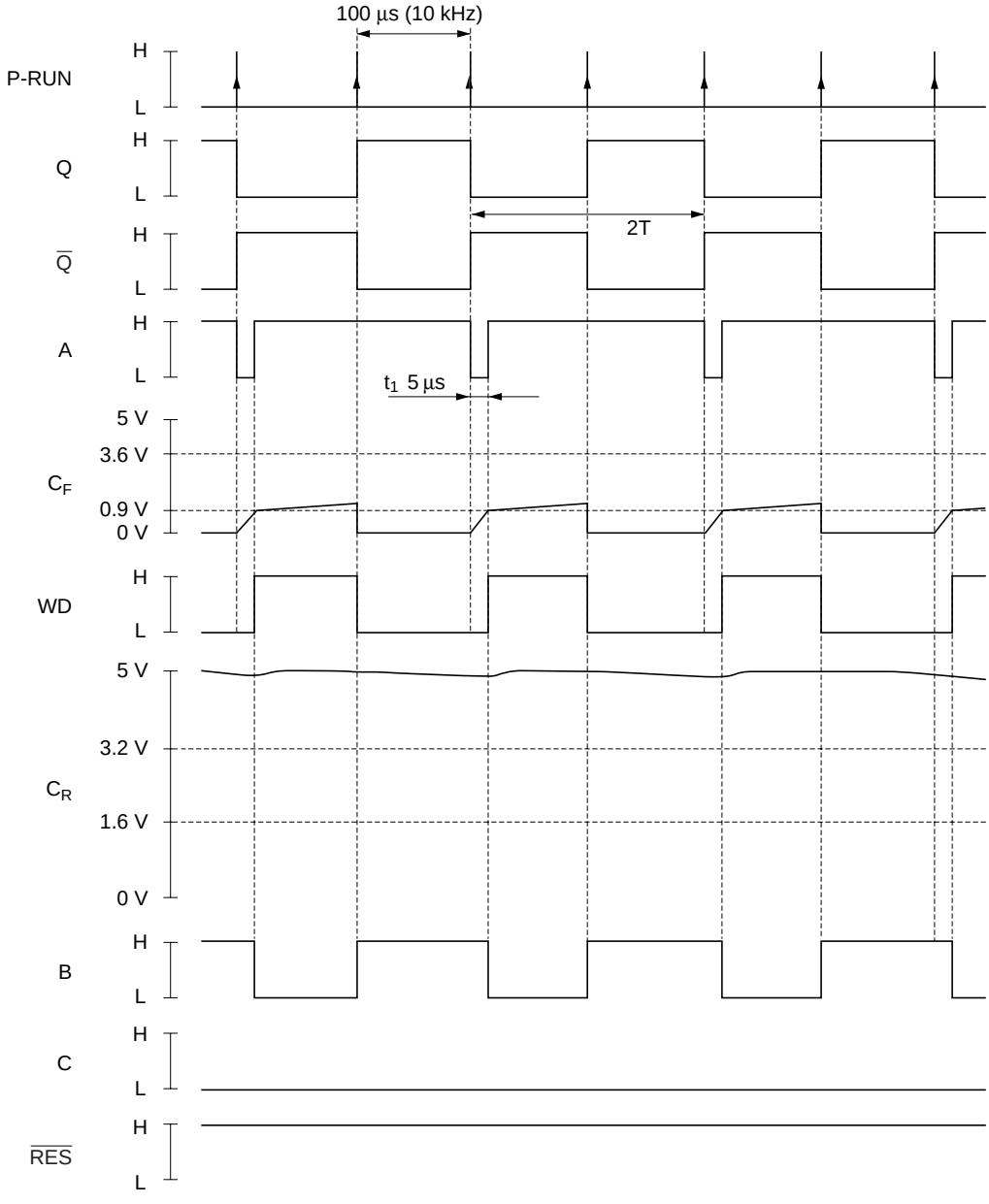
2. With a low-frequency P-RUN signal (≈ 13 Hz to 26 Hz)

When $f_{P\text{-}RUN}$ is 13 Hz to 26 Hz, the WD duty (D = 100 × t_2/2T) is 25% to 50%. When the WD duty is 25% or above, multivibrator (power-on and auto-reset circuit) oscillation stops. As a result, the $\overline{RES}$ signal is fixed high.



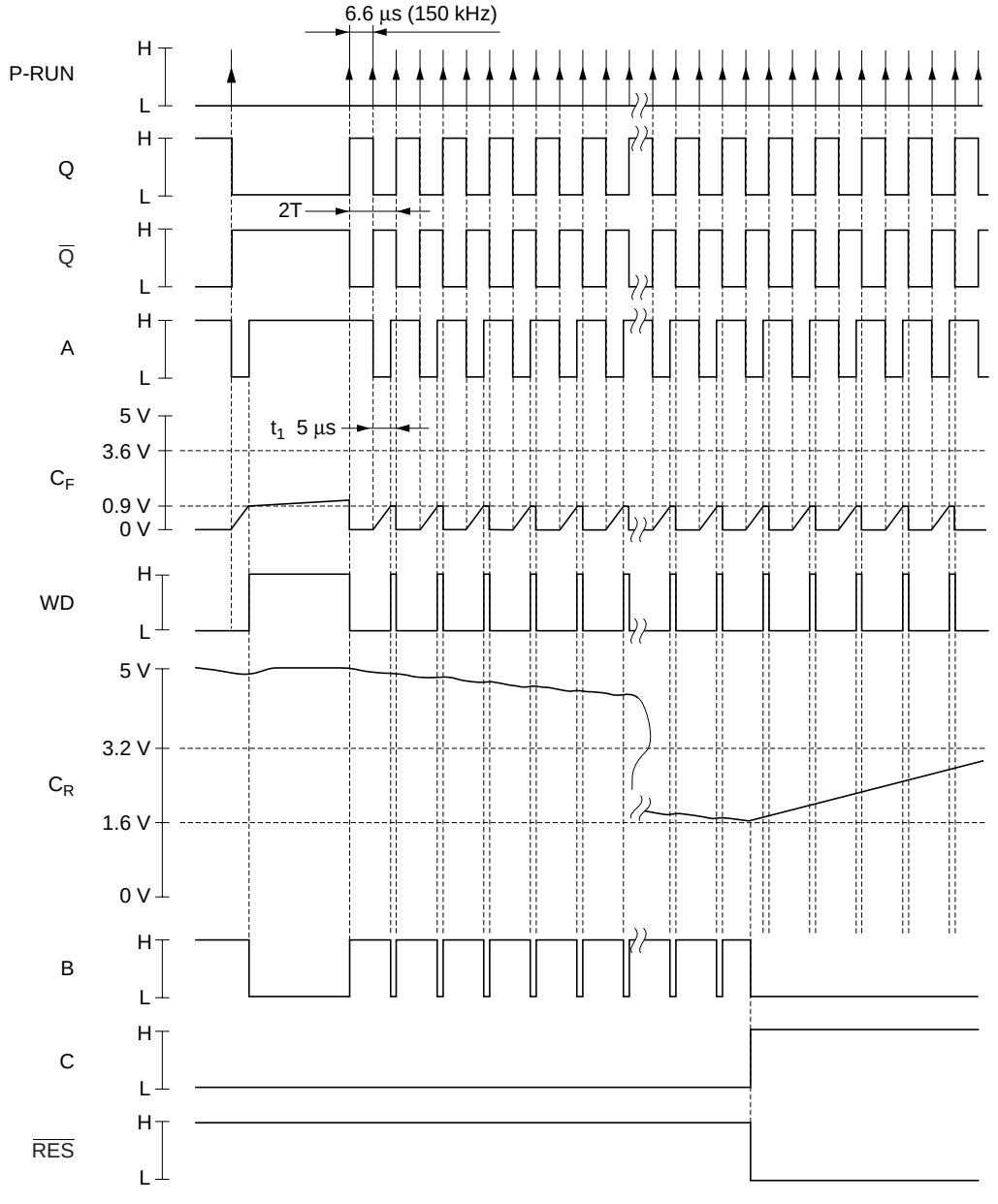
3. With a 10 kHz P-RUN signal

When $f_{P\text{-}RUN}$ is 10 kHz, the WD duty ($D = 100 \times (T - t_2)/2T$) is 48%. As the duty is above 25%, the multivibrator (power-on and auto-reset circuit) does not oscillate. The $\overline{RES}$ signal remains high.



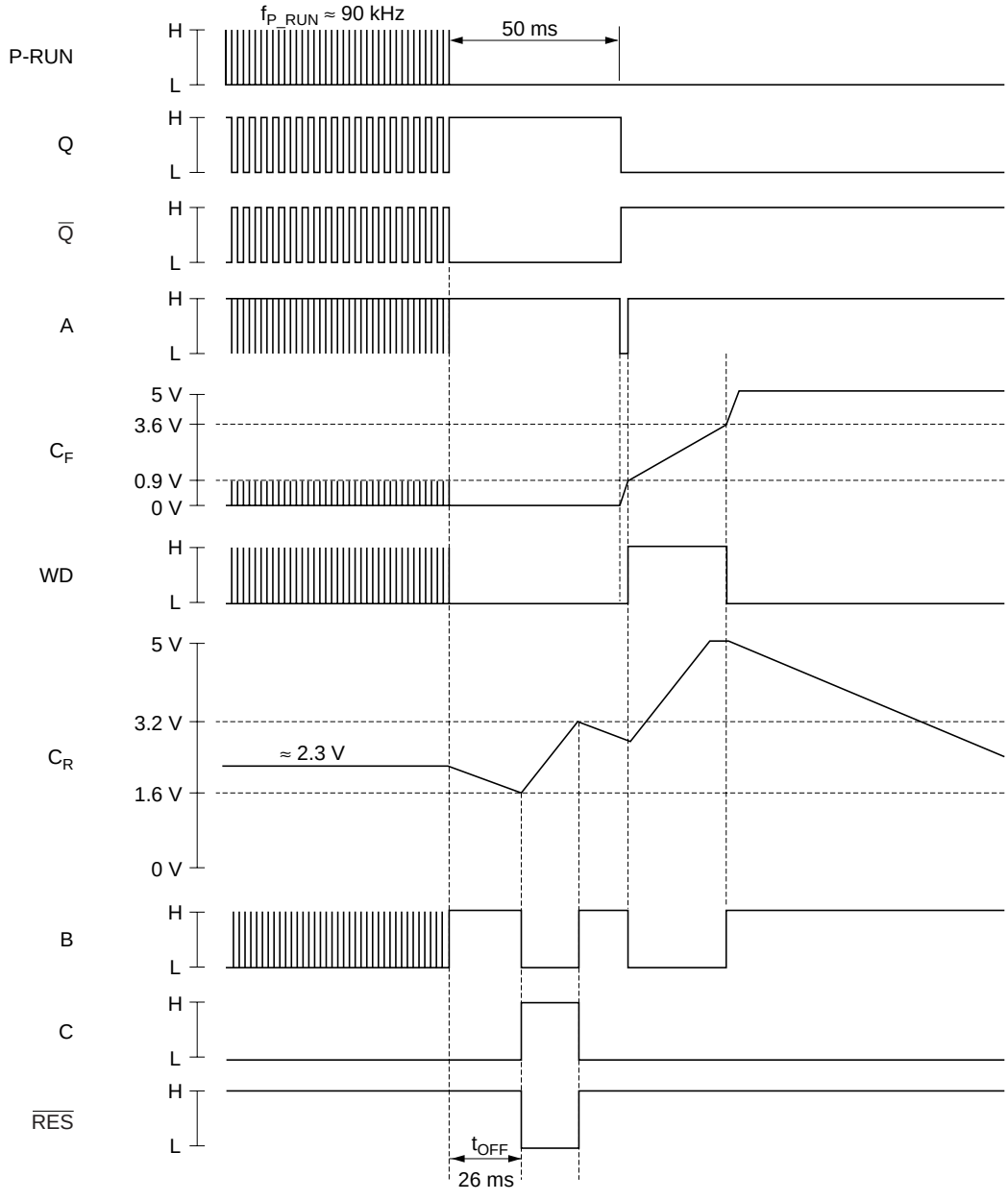
4. With a 150 kHz P-RUN signal

When $f_{P\text{-}RUN}$ is 100 kHz or above, the WD duty (D = 100 × (T – t_2)/2T) is 25% or below. Therefore, C_R is discharged, and the $\overline{RES}$ signal is output at the instant that the pin potential falls to the comparator circuit threshold value (V_{TL} = 1.6 V).



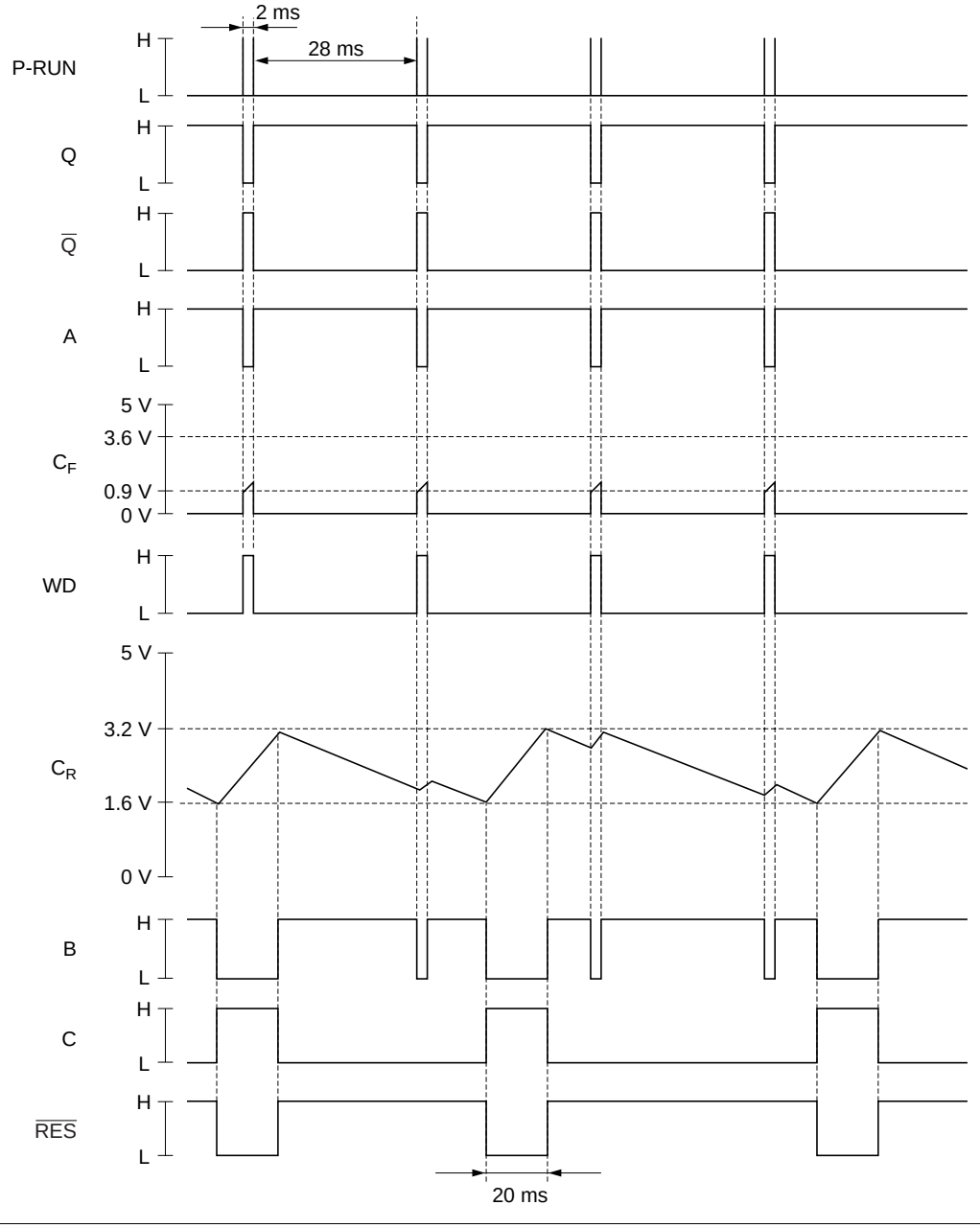
5. t_{OFF} when P-RUN signal ≈ 90 kHz

When the P-RUN frequency is high, even though within specification, the C_R pin potential falls. If the P-RUN frequency falls sharply at this time, t_{OFF} may be short.
With values of C_F = 0.01 µF and C_R = 0.1 µF, the C_R pin potential will not fall as long as the P-RUN frequency is 20 kHz or below.



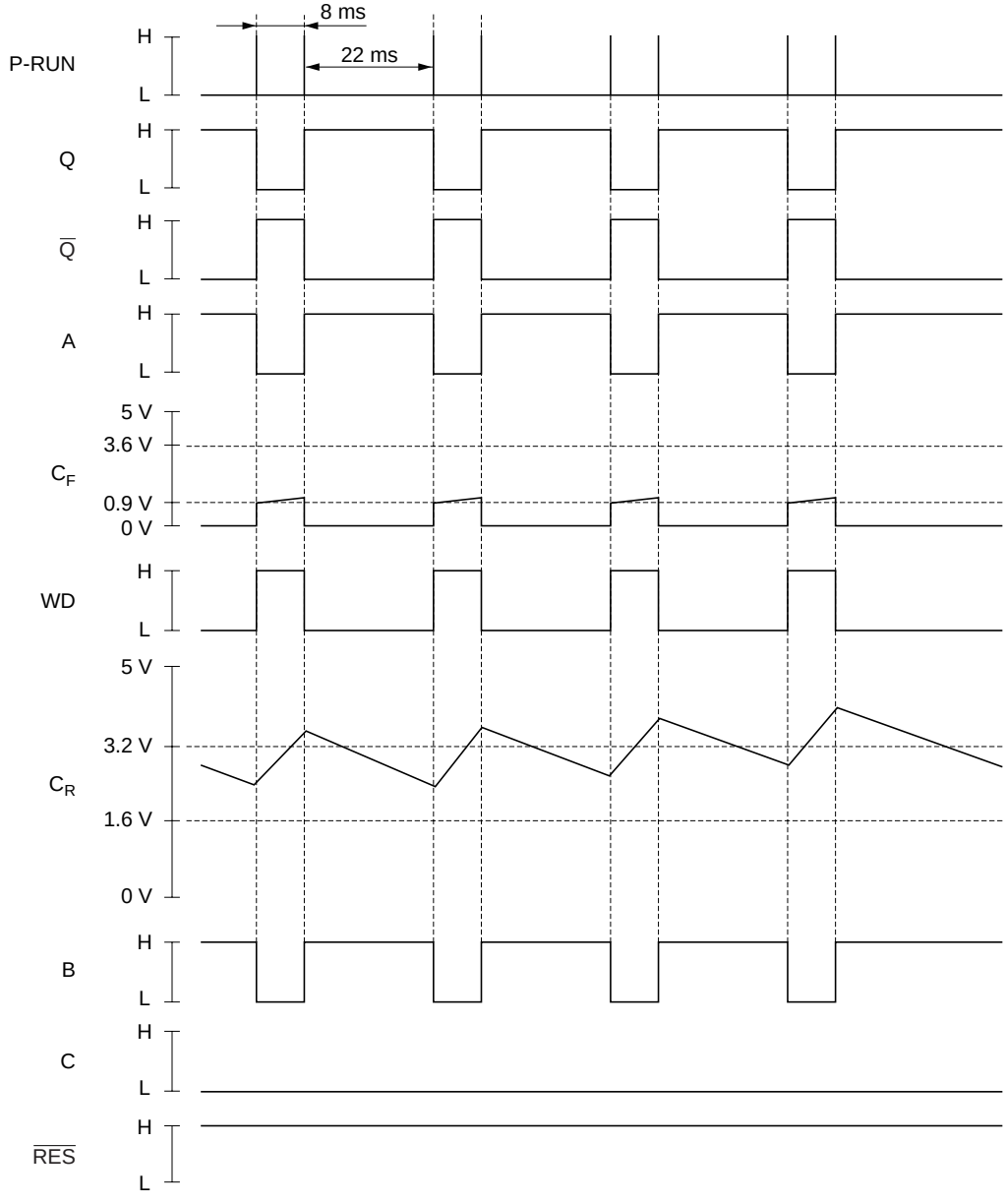
6. When P-RUN frequency fluctuates (1)

If there is a double-pulse in P-RUN, the WD filter duty will be decreased and $\overline{RES}$ will be output, as shown in the figure below, for example. In this case, the condition for non-output of the $\overline{RES}$ signal is a value of 3 or less for the ratio of P-RUN pulse interval minimum value to maximum value (when $f_{P\text{-}RUN} \leq 20$ kHz). This is because the C_R pin charge/discharge current ratio is 3.



7. When P-RUN frequency fluctuates (2)

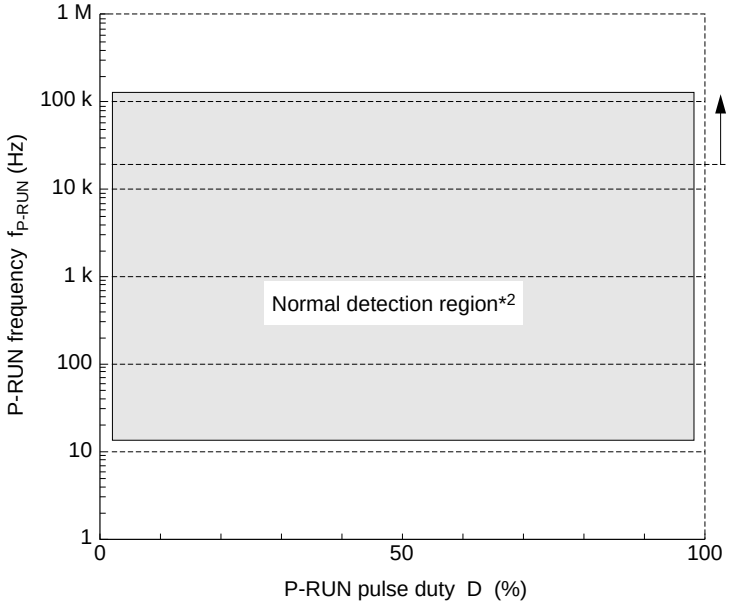
If there is a double-pulse in P-RUN, $\overline{RES}$ will not be output as long as the ratio of P-RUN pulse interval minimum value to maximum value is 3 or less. The timing chart for a P-RUN minimum interval of 8 ms and maximum interval of 22 ms is shown below.



8. Summary of cases where P-RUN frequency fluctuates

If there is a double-pulse in P-RUN, $\overline{RES}$ may be output if the double-pulse has multiple frequency components. If the P-RUN frequency fluctuates, refer to the following when making the P-RUN setting.

- P-RUN normal detection region, duty dependency

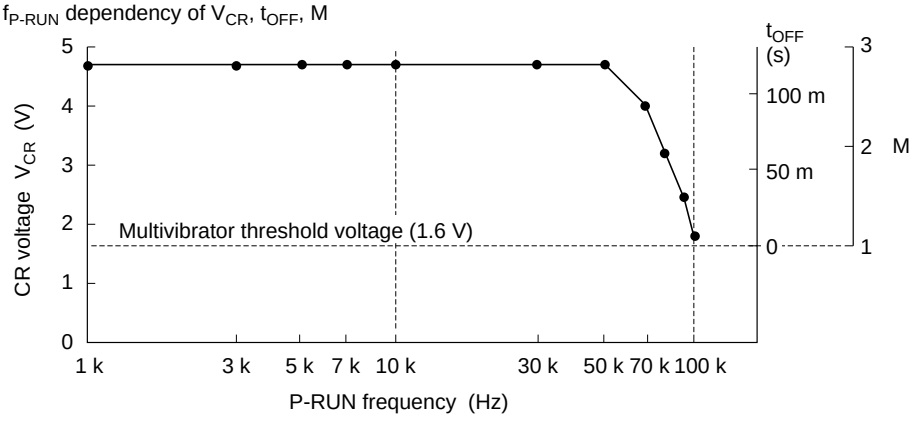


Note: 1
When $f_{P-RUN} \geq 20$ kHz, t_{OFF} is frequency-dependent, so care is required when making the P-RUN setting (see figure below).

Note: 2. This is the region when f_{P-RUN} is constant.
If f_{P-RUN} fluctuates within the normal detection region, the following applies:

Normal detection is performed when the condition $f_{P-RUN\ H}/f_{P-RUN\ L} < M$ is satisfied.

- f_{P-RUN} dependency of V_{CR}, t_{OFF}, M



Setting of $\overline{RES}$ Timing and Watchdog Frequency Range

Different MPUs have different $\overline{RES}$ timing requirements. The minimum reset time (t_{ON}) required at power-on (rise of V_{CC}) is 20 ms for some MPUs and 100 ms for others.

$\overline{RES}$ timing waveform parameters must be selected according to the MPU. With the HA16117F the timing of the $\overline{RES}$ output and the watchdog frequency range can both be set by external constants (C_F, C_R, and K).

		Parameters		
Item	**Symbol**	**CR (pin 4)**	**CF (pin 3)**	**K (pin 8) *1**
Power-on reset time	t_{ON}	●		
Reset-clock off time	t_{OFF}	●	▲ *2	●
Reset low time	t_{RL}	●		
Reset high time	t_{RH}	●		●
Watchdog frequency high	f_H		●	●
Watchdog frequency low	f_L	●	●	●

Notes: 1. $K = R_2 / (R_1 + R_2)$
2. Variability of t_{OFF} increases with increasing C_F. The variability Δt_{OFF} is approximately 3.3 (MΩ) × C_F (μF), so $C_F \leq 0.01$ (μF) is recommended.
3. External constants should be selected with reference to the formulas in tables 1 and 2.

Table 1 Calculation of $\overline{RES}$ Output Timing

Item	**Formula**	**Notes**
t_{ON} (ms)	400 (Ω) × C_R (μF)	t_{ON} and t_{OFF} can be set independently
t_{OFF} (ms)	1.99 × t_{RH} (ms)	
t_{RL} (ms)	0.5 × t_{ON} (ms)	t_{RL} and t_{RH} can be set independently
t_{RH} (ms)	$\dfrac{1.6\ (V)}{K \times 31\ (\mu A) - 15.8\ (\mu A)} \times C_R\ (\mu F) \times 10^3$	
t_{SL} (ms)	≈ t_{OFF} (ms)	

Table 2 Calculation of Watchdog Frequency Range

Item	**Formula**
f_H (MHz)	$\dfrac{1}{500\ (\Omega) \times C_F\ (\mu F)} \times \dfrac{t_{RH}\ (ms) - t_{RL}\ (ms)}{t_{RH}\ (ms) + t_{RL}\ (ms)}$
f_L (Hz)	$\dfrac{1}{1.7\ (M\Omega) \times C_F\ (\mu F)} \times \dfrac{t_{RL}\ (ms)}{t_{RH}\ (ms) + t_{RL}\ (ms)}$ or $\dfrac{1}{t_{OFF}\ (ms)} \times 10^3$ Whichever is larger

Selection of External Constants

If the reset duration necessary for the MPU to operate reliably at power-on is known, there is a simple procedure for selecting external constants, starting from the power-on reset time (t_{ON}).

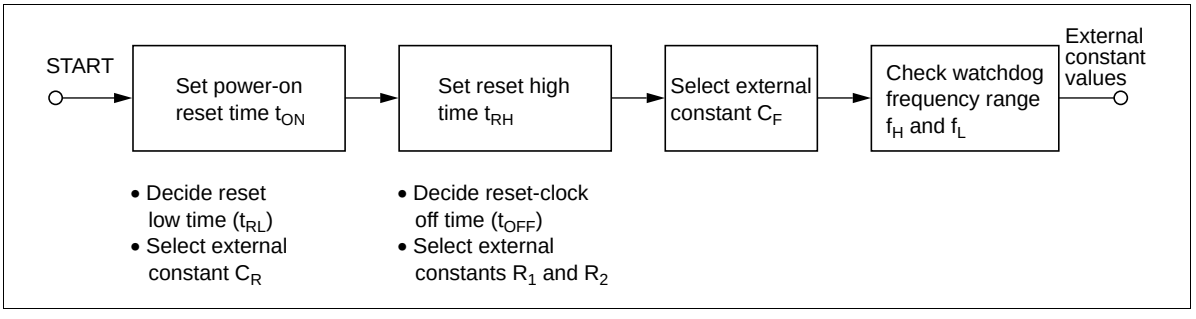
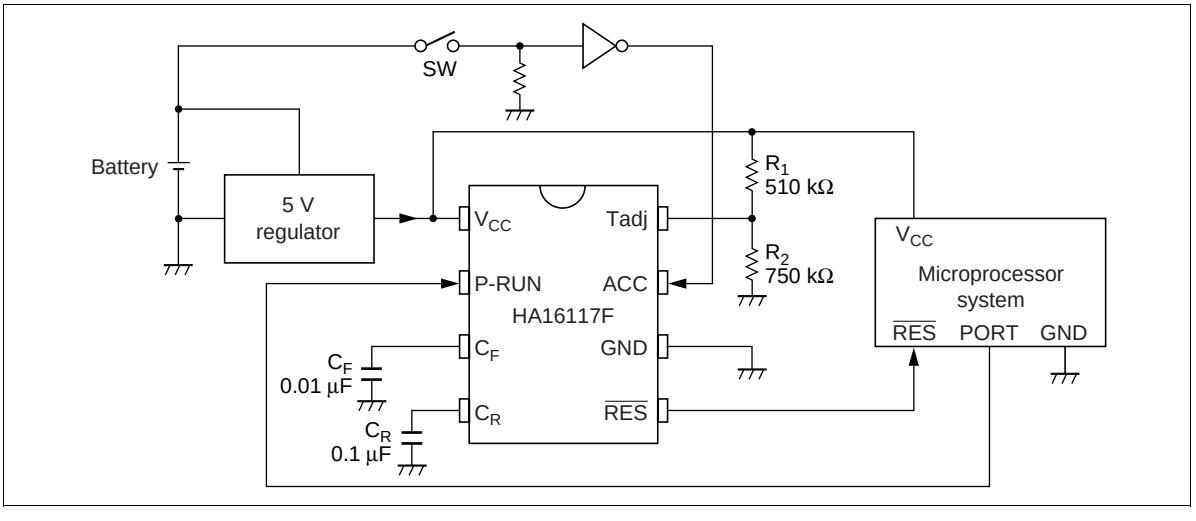
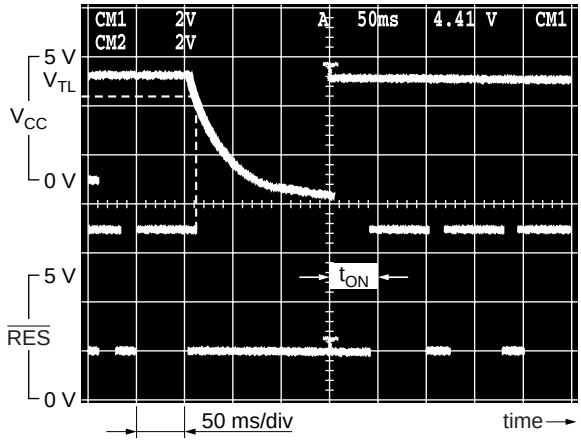


Figure 4 Procedure for Selecting External Constants

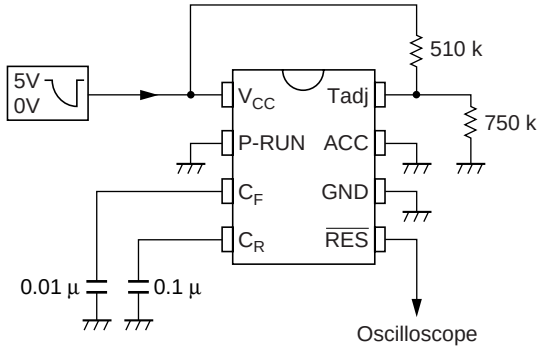
Application Example



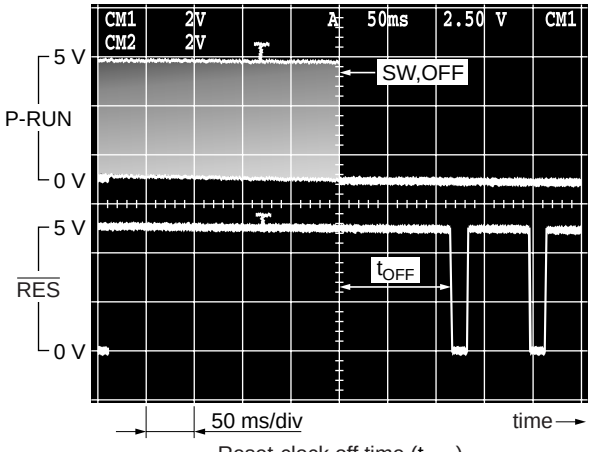
Operating Characteristics and Test Circuits



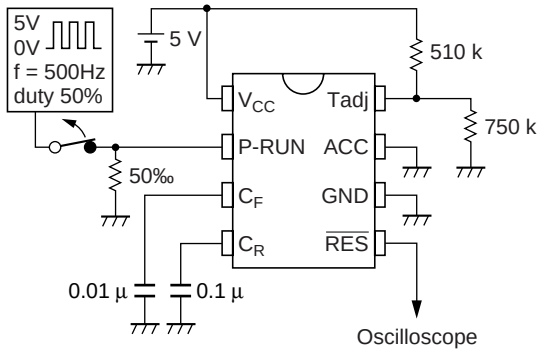
Power-on reset time (t_{ON})



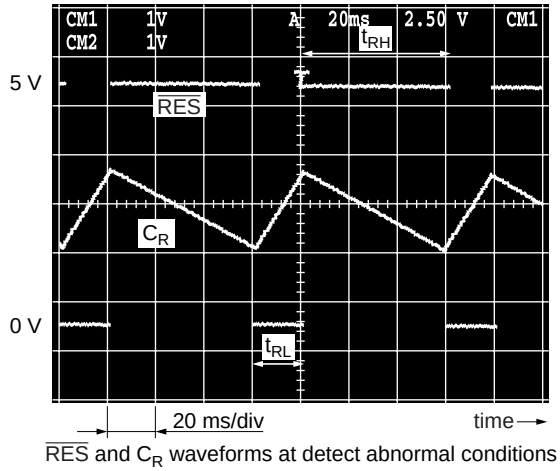
Circuit for measuring t_{ON}



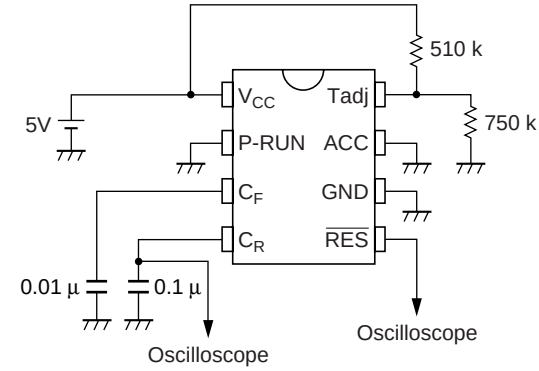
Reset-clock off time (t_{OFF})



Circuit for measuring t_{OFF}

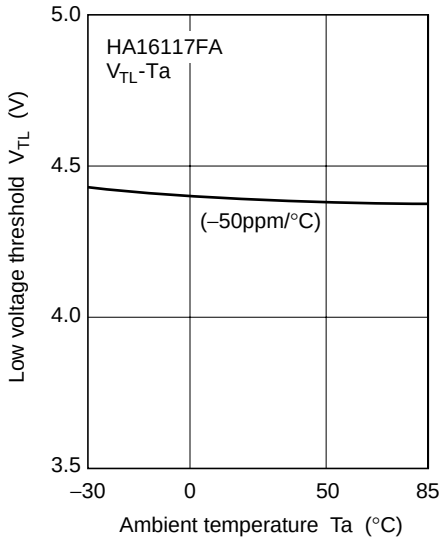


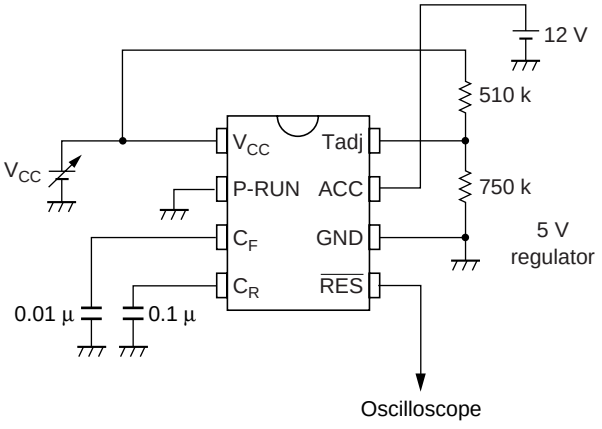
$\overline{RES}$ and C_R waveforms at detect abnormal conditions



Circuit for measuring $\overline{RES}$ and C_R waveforms

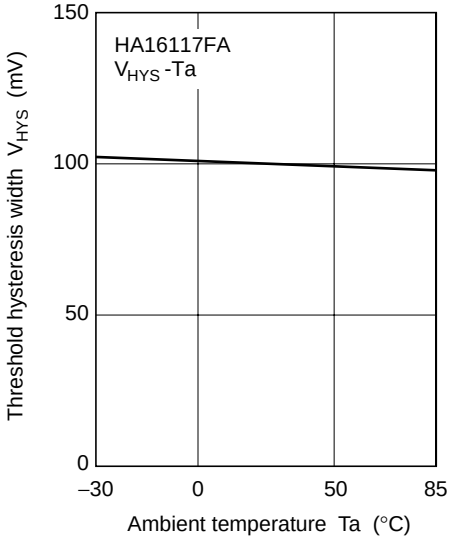
Low Voltage Threshold vs. Ambient Temperature

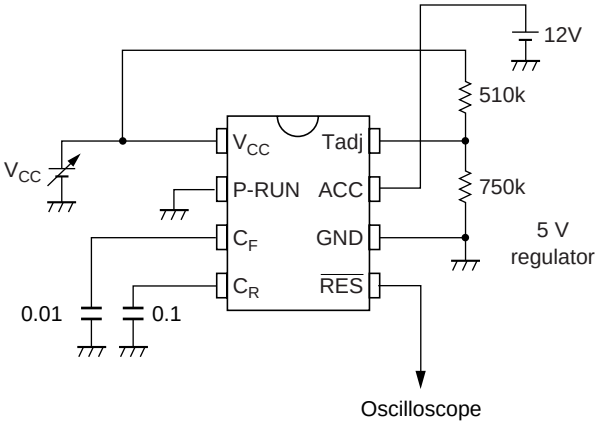




Test circuit

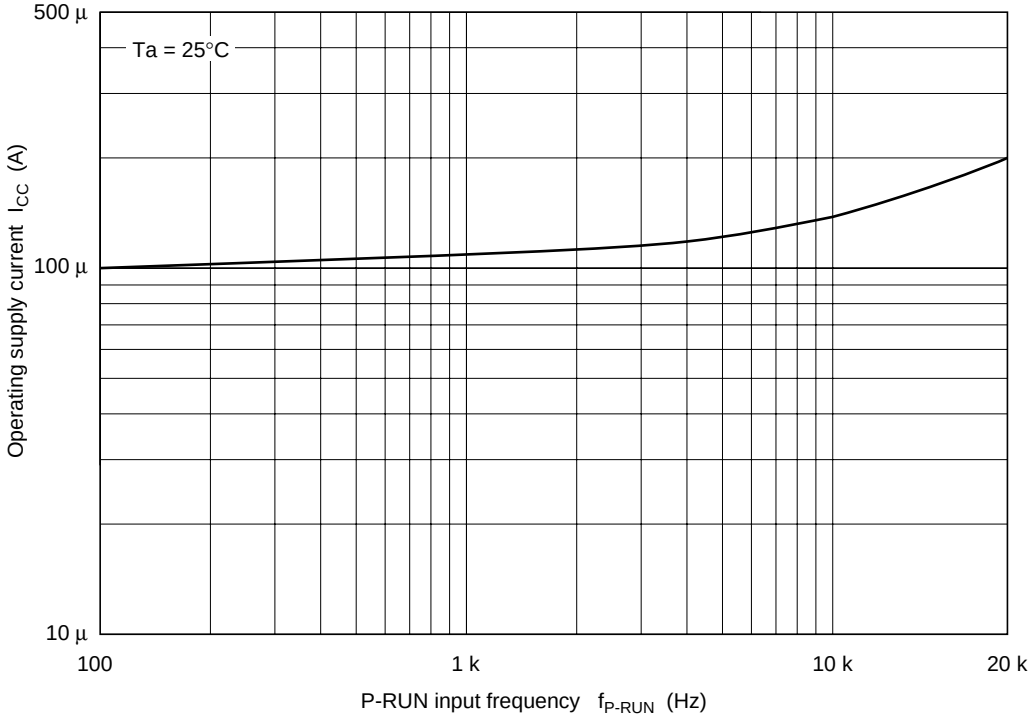
Threshold Hysteresis Width vs. Ambient Temperature

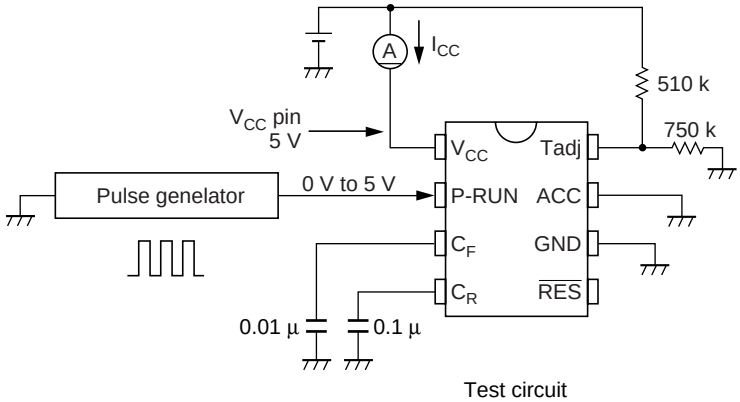




Test circuit

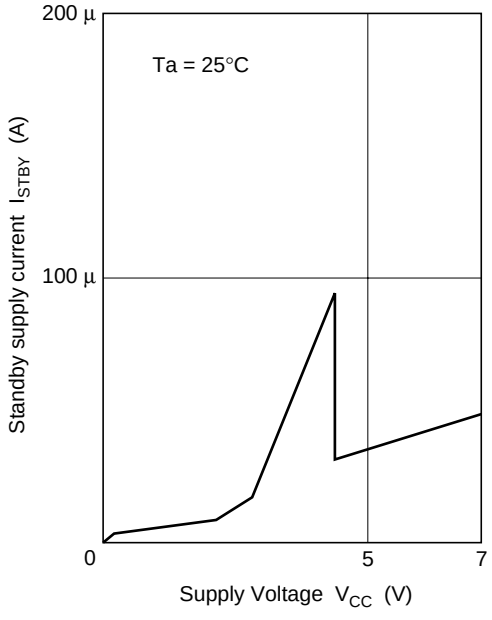
Operating Supply Current vs. P-RUN Input Frequency

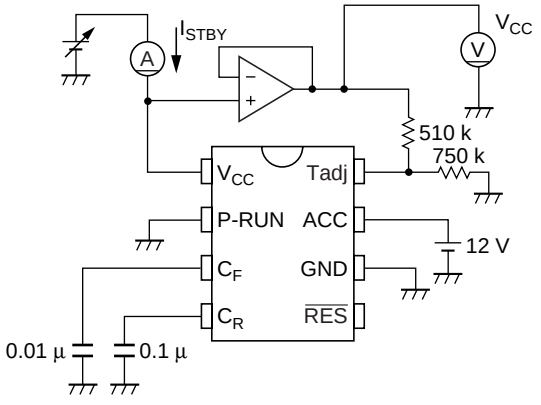




Test circuit

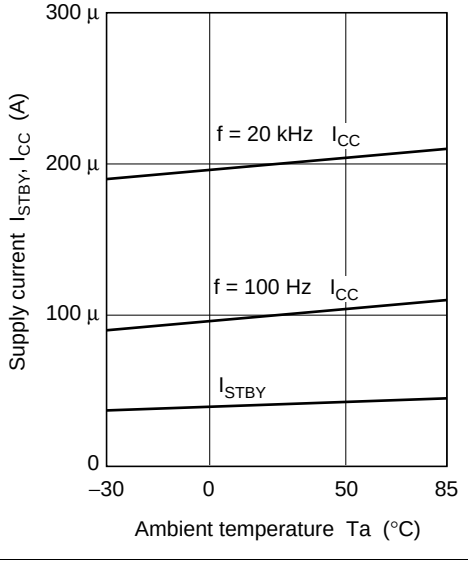
Standby Supply Current vs. Supply Voltage



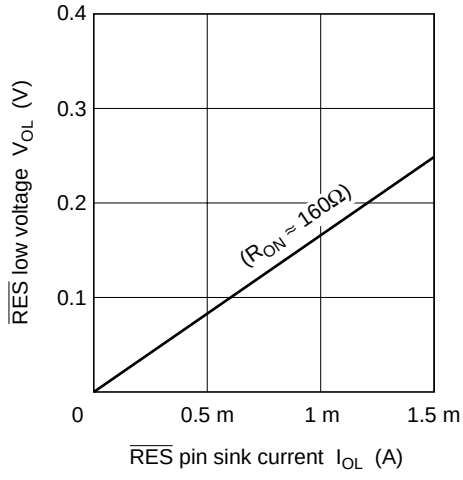


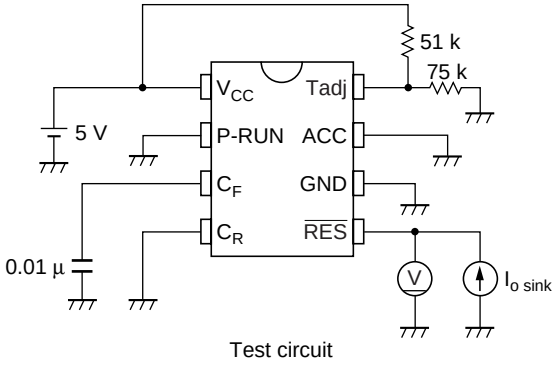
Test circuit

Supply Current vs. Ambient Temperature



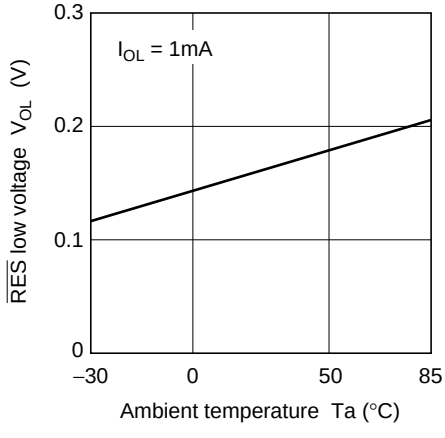
$\overline{RES}$ Low Voltage vs. $\overline{RES}$ pin Sink Current



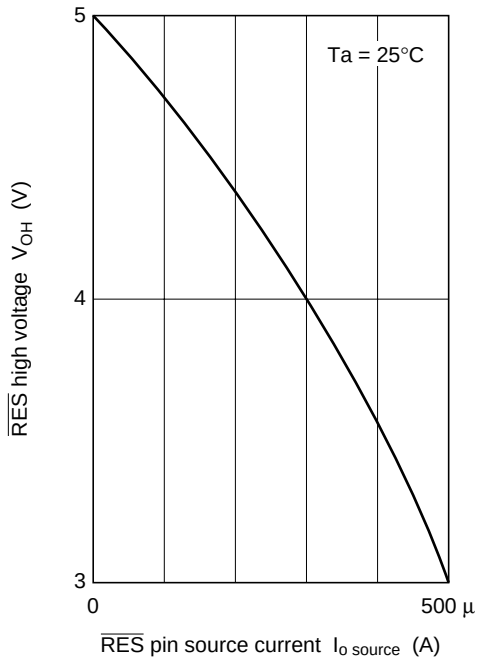


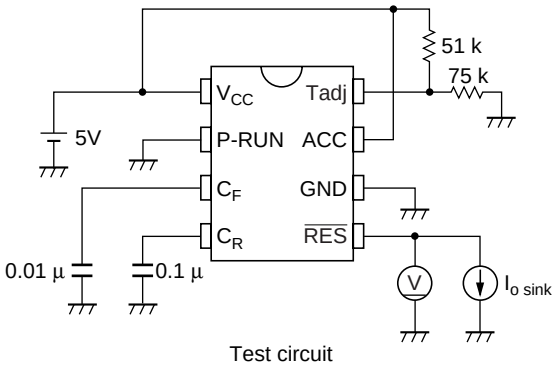
Test circuit

$\overline{RES}$ Low Voltage vs. Ambient Temperature



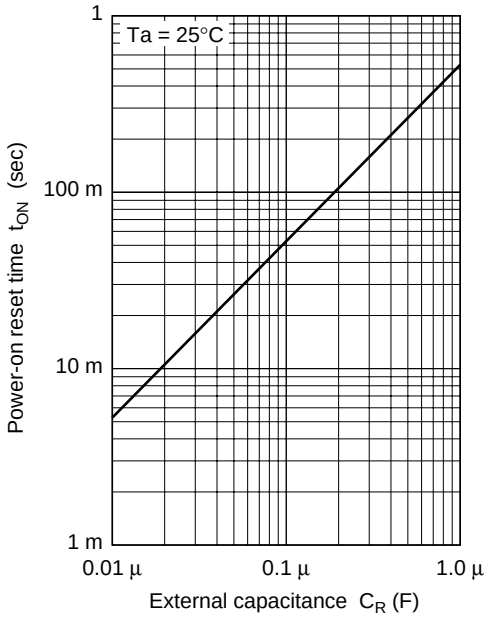
$\overline{RES}$ High Voltage vs. $\overline{RES}$ pin Source Current

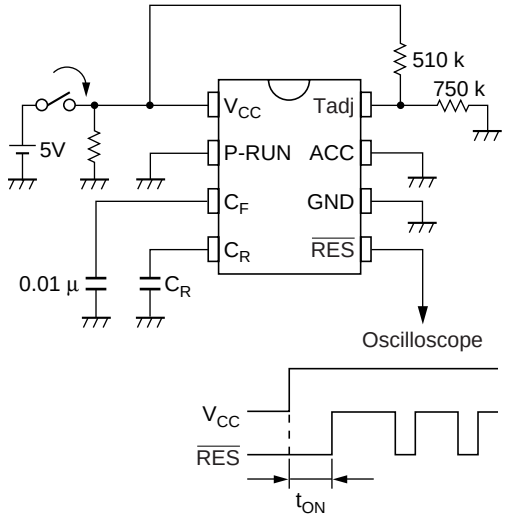




Test circuit

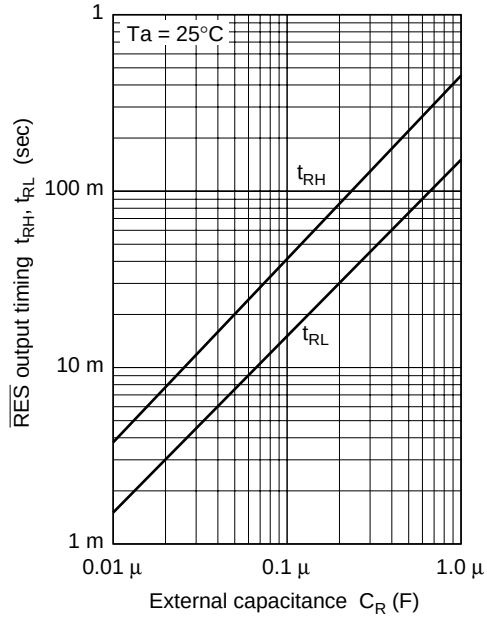
Power-on Reset Time vs. C_R Capacitance

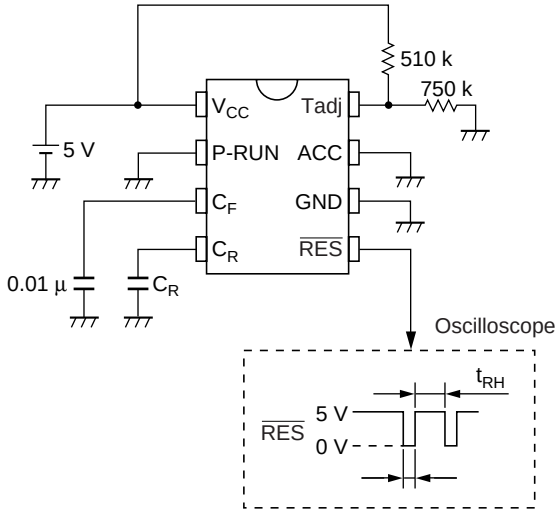




Test circuit

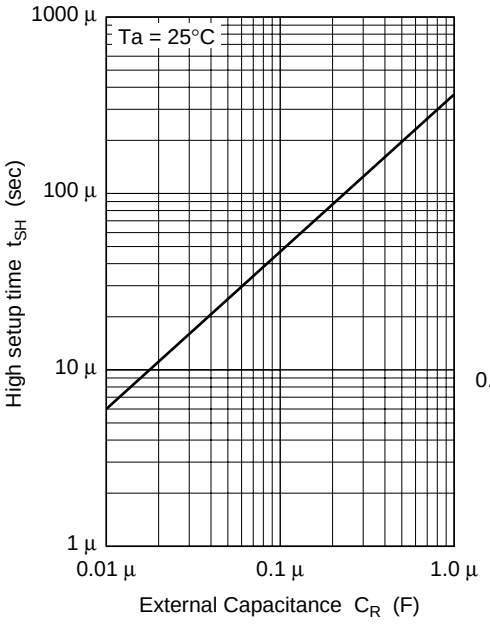
$\overline{RES}$ Output Timing vs. C_R Capacitance

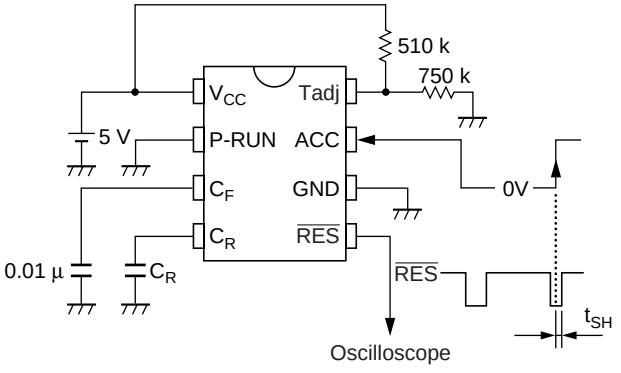




Test circuit

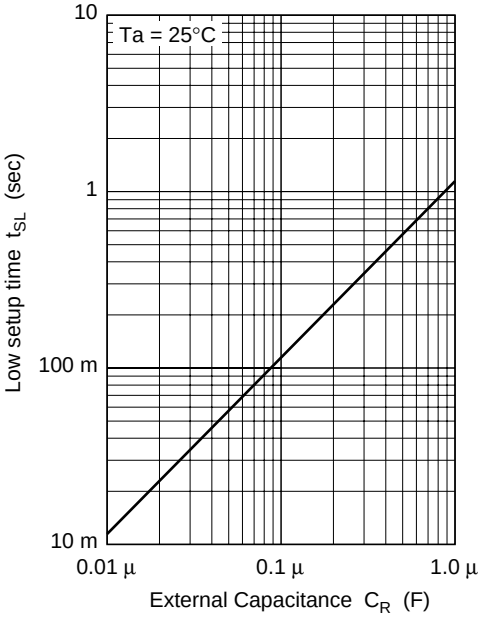
High Setup Time vs. C_R Capacitance

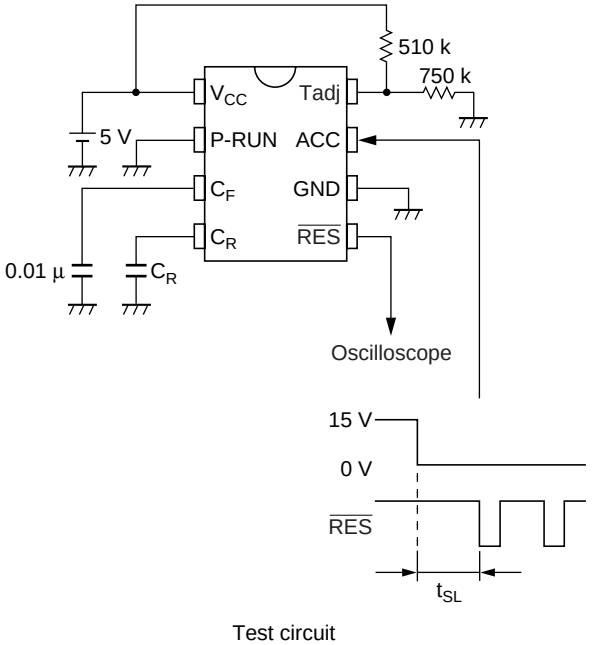




Test circuit

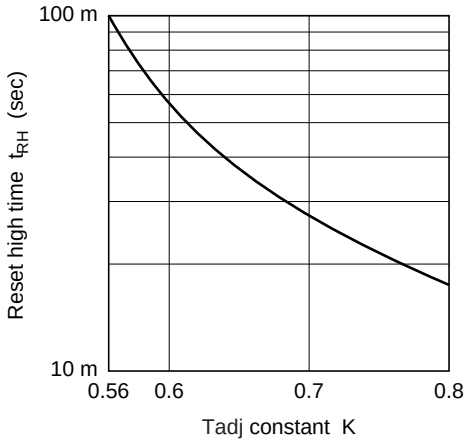
Low Setup Time vs. C_R Capacitance

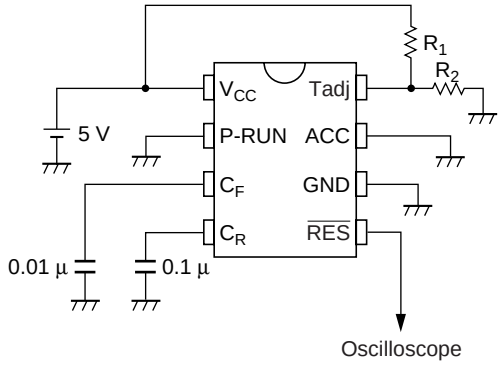




Test circuit

Reset High Time vs. K (Tadj Constant)

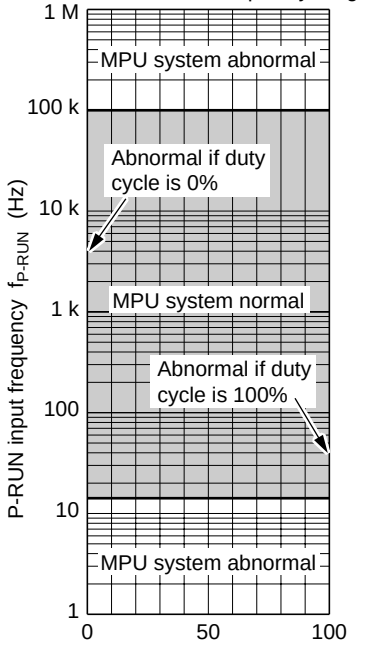


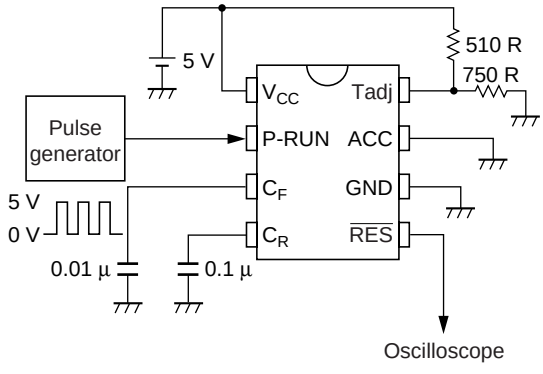


Test circuit

$$K = \frac{R_2}{R_1 + R_2}$$

Duty-cycle dependence of P-RUN normal frequency range



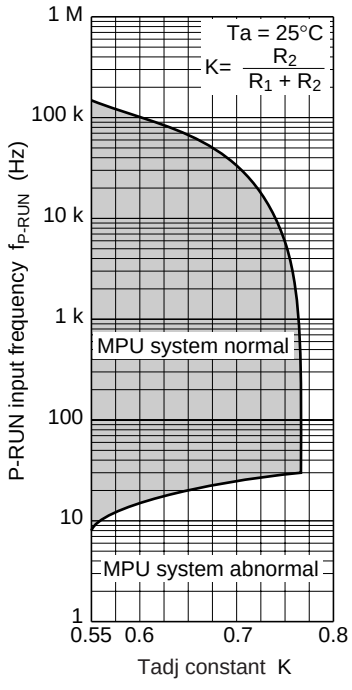


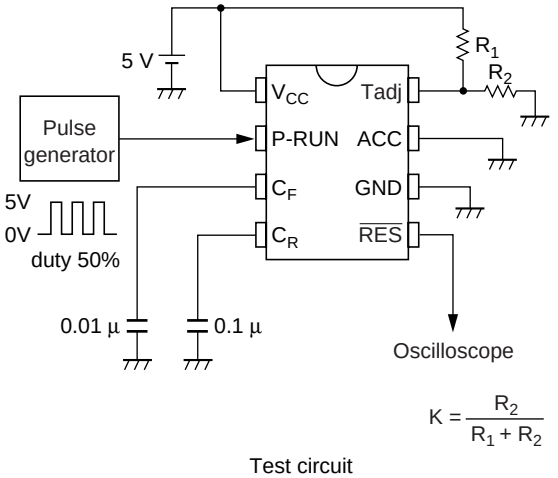
Test circuit

Notes: 1. Normal detection is assumed when $\overline{RES}$ is not output.

2. The figure at left is for a constant P-RUN frequency. See "8. Summary of cases where P-RUN frequency fluctuates" for cases where the frequency fluctuates.

P-RUN Input Frequency vs. K (Tadj constant)

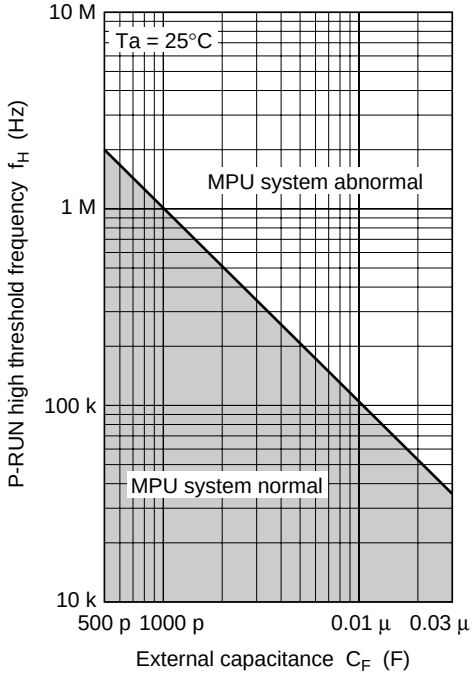


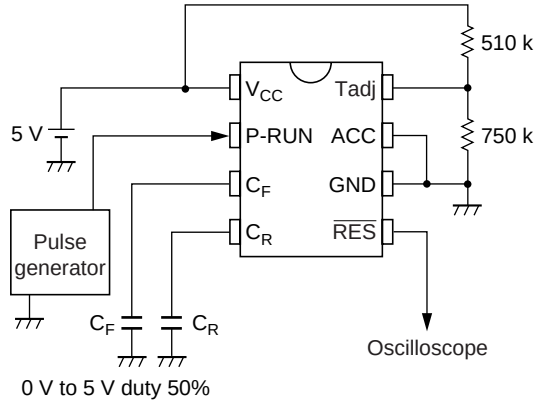


Test circuit

Notes: 1. Normal detection is assumed when $\overline{RES}$ is not output.
2. The figure at left is for a constant P-RUN frequency.

P-RUN High Threshold Frequency vs. C_F Capacitance

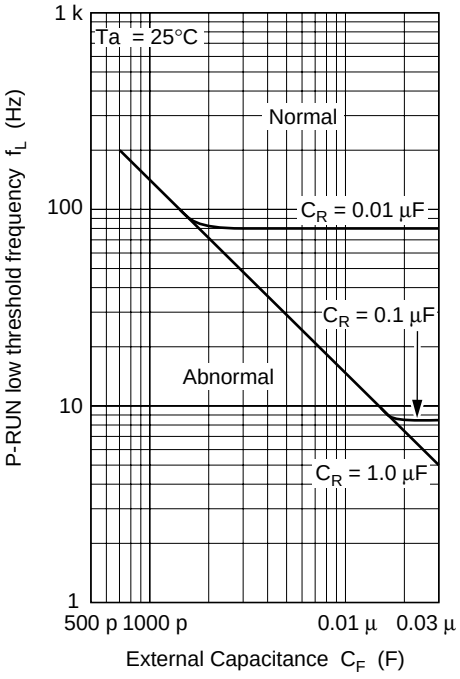


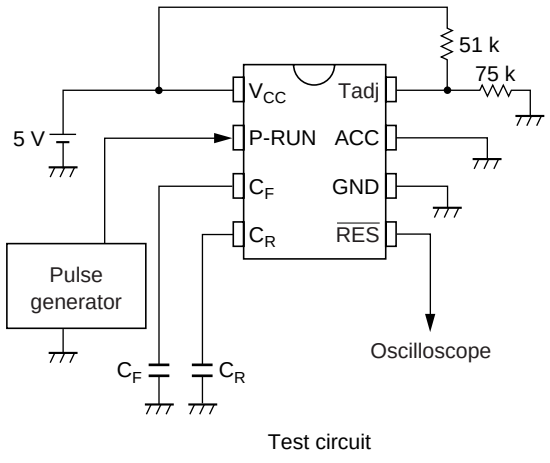


Test circuit

Notes: 1. Normal detection is assumed when $\overline{RES}$ is not output.
2. The figure at left is for a constant P-RUN frequency.

P-RUN Low Threshold Frequency vs. C_F Capacitance

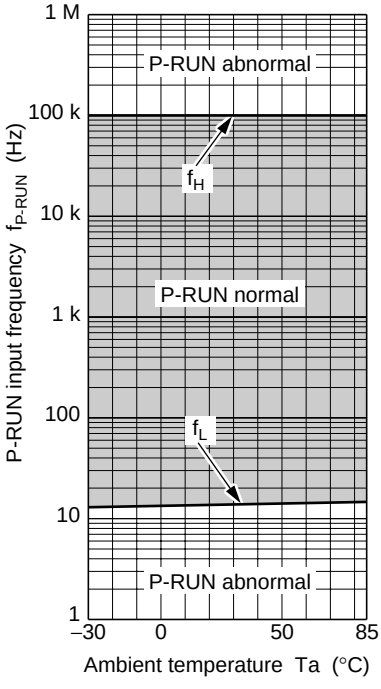


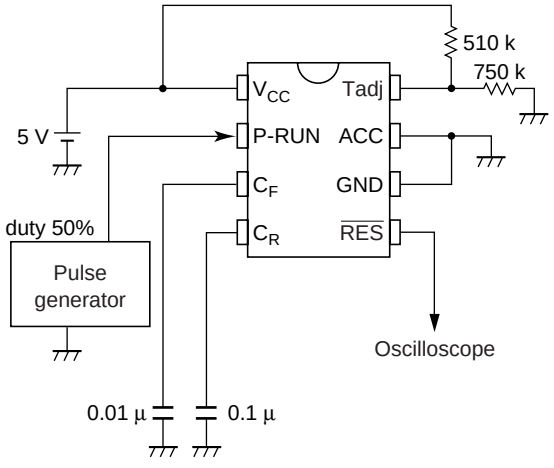


Test circuit

Notes: 1. Normal detection is assumed when $\overline{RES}$ is not output.
2. The figure at left is for a constant P-RUN frequency.

P-RUN Input Frequency vs. Ambient Temperature

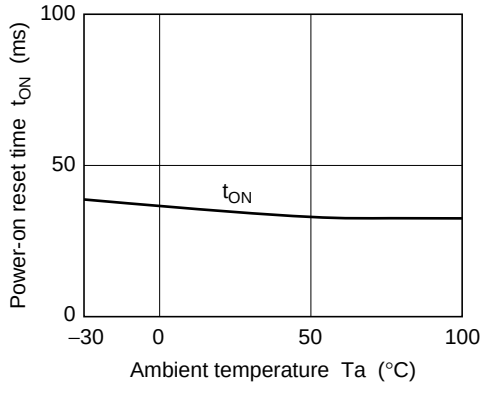




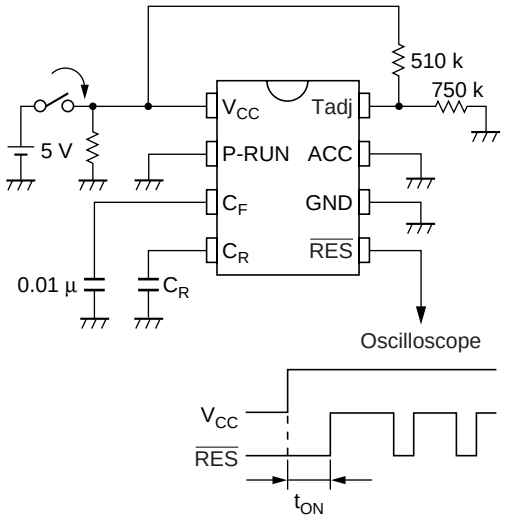
Test circuit

Notes: 1. Normal detection is assumed when $\overline{RES}$ is not output.
2. The figure at left is for a constant P-RUN frequency.

Power-on Reset Time vs. Ambient Temperature

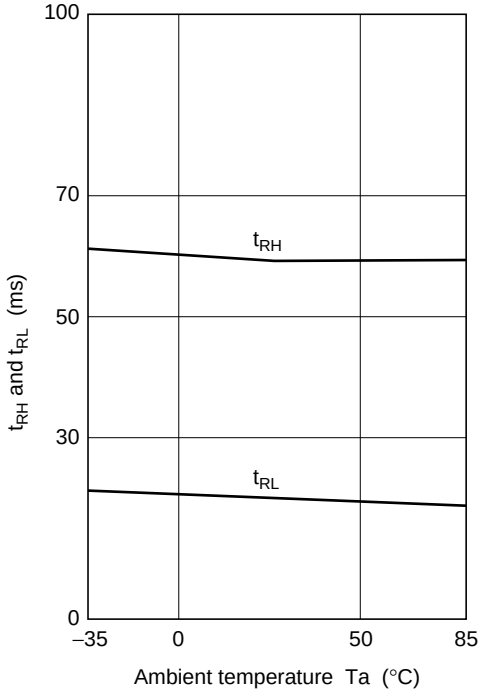


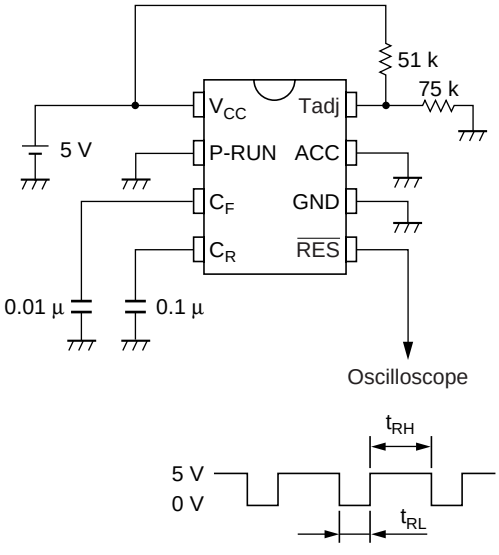
Power-on Reset Time vs. Ambient Temperature



Test circuit

t_{RH} and t_{RL} vs. Ambient Temperature

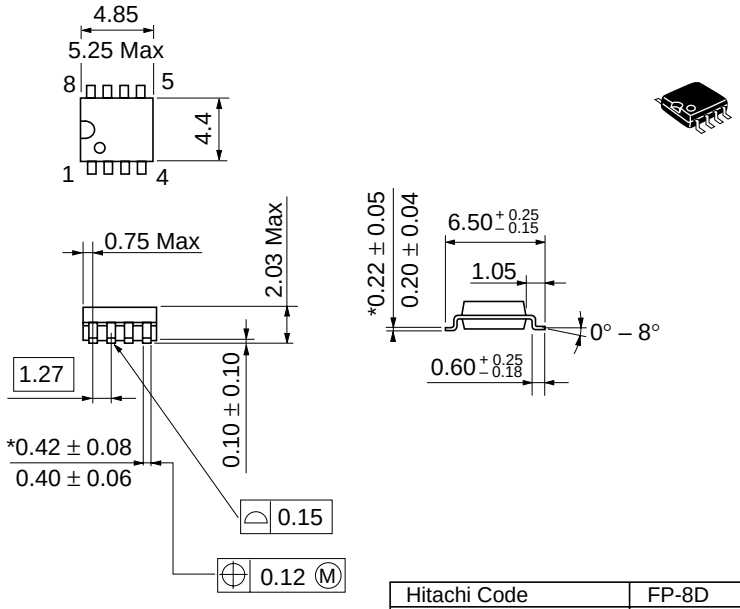




Test circuit

Package Dimensions

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-8D
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.10 g

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