

To all our customers

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Renesas Technology Corp.  
Customer Support Dept.  
April 1, 2003

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Keep safety first in your circuit designs!

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# 4AK17

## Silicon N-Channel Power MOS FET Array



ADE-208-1202 (Z)  
1st. Edition  
Mar. 2001

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### Application

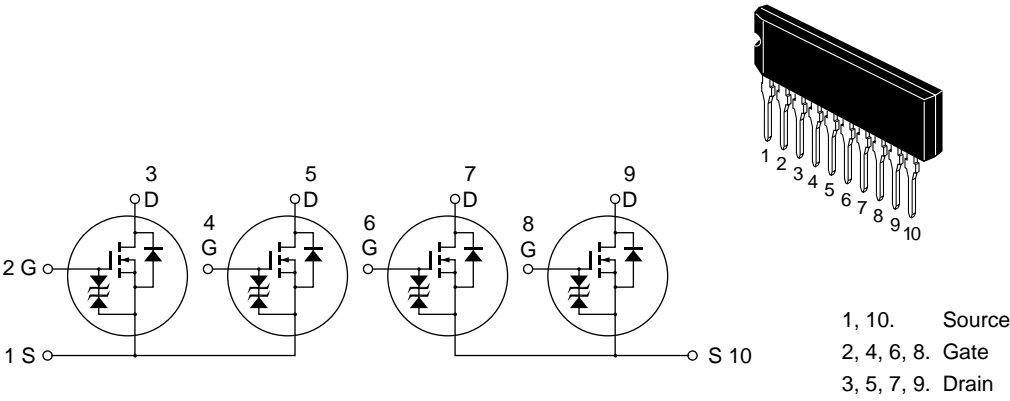
High speed power switching

### Features

- Low on-resistance  
 $R_{DS(on)} \leq 0.045$  ,  $V_{GS} = 10$  V,  $I_D = 10$  A  
 $R_{DS(on)} \leq 0.065$  ,  $V_{GS} = 4$  V,  $I_D = 10$  A
- Capable of 4 V gate drive
- Low drive current
- High speed switching
- High density mounting
- Suitable for motor driver, solenoid driver and lamp driver

Outline

SP-10



Absolute Maximum Ratings (Ta = 25°C) (1 Unit)

Item	Symbol	Rating	Unit
Drain to source voltage	$V_{DSS}$	60	V
Gate to source voltage	$V_{GSS}$	±20	V
Drain current	$I_D$	10	A
Drain peak current	$I_{D(pulse)}^{*1}$	40	A
Body to drain diode reverse drain current	$I_{DR}$	10	A
Channel dissipation	$P_{ch} (T_c = 25^{\circ}C)^{*2}$	28	W
Channel dissipation	$P_{ch}^{*2}$	4	W
Channel temperature	$T_{ch}$	150	°C
Storage temperature	$T_{stg}$	-55 to +150	°C

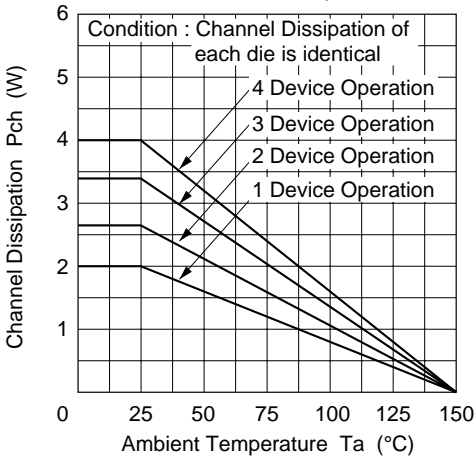
Notes: 1.  $PW \leq 10 \mu s$ , duty cycle  $\leq 1\%$   
2. 4 devices operation

**Electrical Characteristics** (Ta = 25°C) (1 Unit)

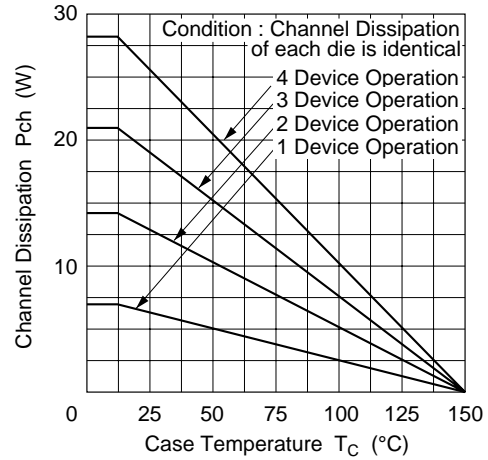
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	$I_D = 10 \text{ mA}$ , $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	$I_G = \pm 100 \text{ } \mu\text{A}$ , $V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	±10	μA	$V_{GS} = \pm 16 \text{ V}$ , $V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	250	μA	$V_{DS} = 50 \text{ V}$ , $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	$I_D = 1 \text{ mA}$ , $V_{DS} = 10 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.033	0.045	Ω	$I_D = 10 \text{ A}$ $V_{GS} = 10 \text{ V}^{*1}$
			0.04	0.065	Ω	$I_D = 10 \text{ A}$ $V_{GS} = 4 \text{ V}^{*1}$
Forward transfer admittance	$ y_{fs} $	10	17	—	S	$I_D = 10 \text{ A}$ $V_{DS} = 10 \text{ V}^{*1}$
Input capacitance	$C_{iss}$	—	1400	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	$C_{oss}$	—	720	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	220	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	15	—	ns	$I_D = 10 \text{ A}$
Rise time	$t_r$	—	95	—	ns	$V_{GS} = 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	300	—	ns	$R_L = 3 \text{ } \Omega$
Fall time	$t_f$	—	170	—	ns	
Body to drain diode forward voltage	$V_{DF}$	—	1.05	—	V	$I_F = 10 \text{ A}$ , $V_{GS} = 0$
Body to drain diode reverse recovery time	$t_{rr}$	—	110	—	ns	$I_F = 10 \text{ A}$ , $V_{GS} = 0$ $dI_F/dt = 50 \text{ A}/\mu\text{s}$

Note: 1. Pulse test

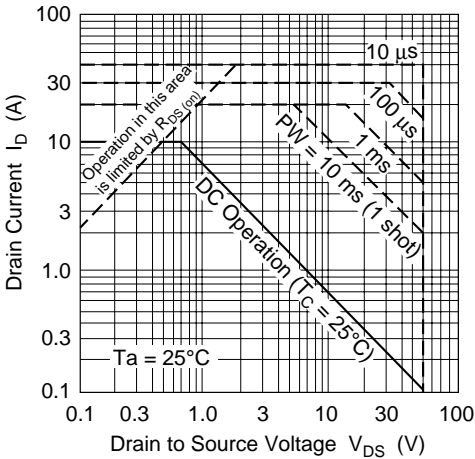
Maximum Channel Dissipation Curve



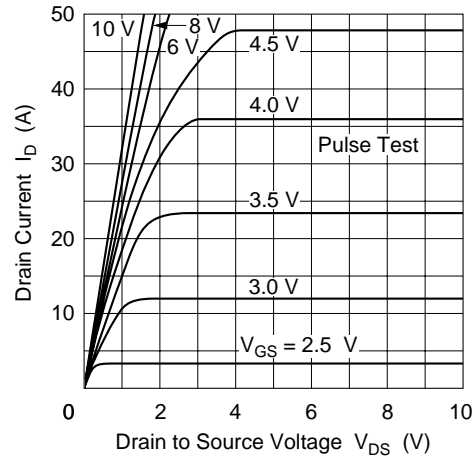
Maximum Channel Dissipation Curve



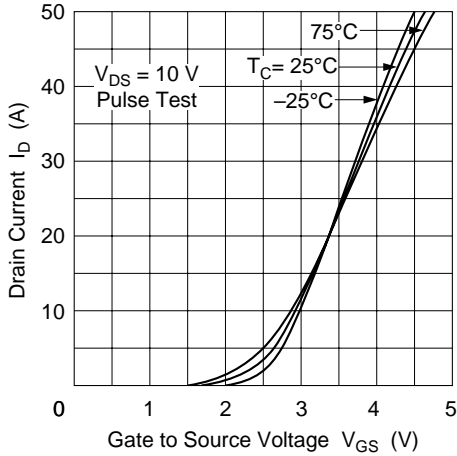
Maximum Safe Operation Area



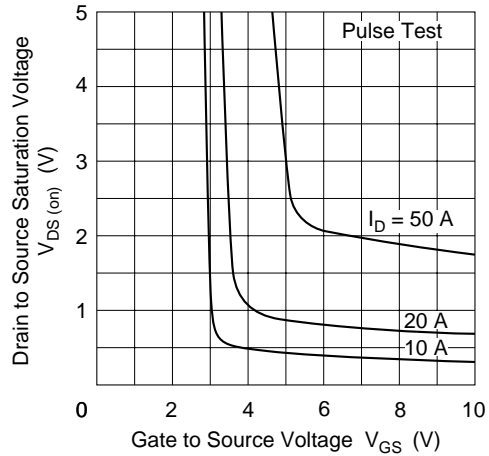
Typical Output Characteristics



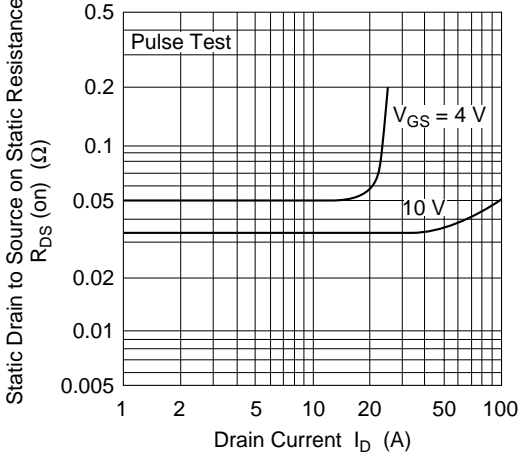
Typical Transfer Characteristics



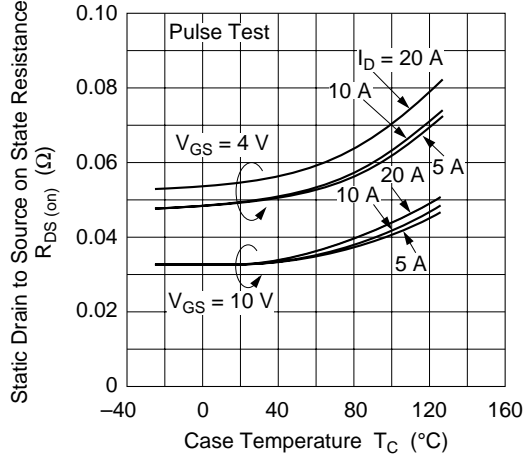
Drain to Source Saturation Voltage vs. Gate to Source Voltage



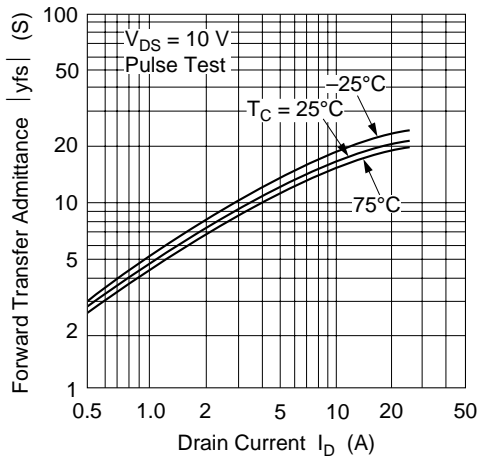
Static Drain to Source on State Resistance vs. Drain Current



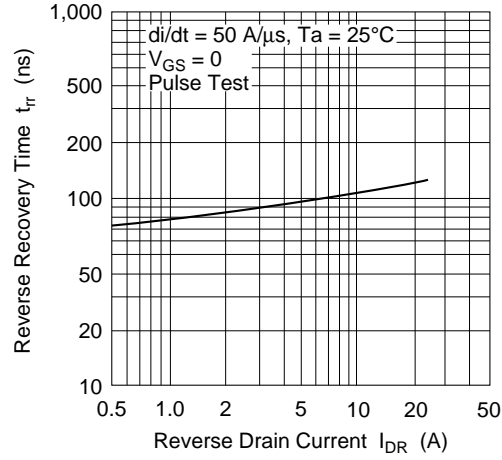
Static Drain to Source on State Resistance vs. Temperature



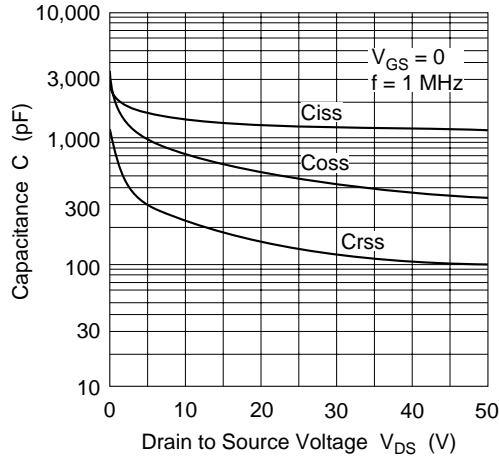
Forward Transfer Admittance  
vs. Drain Current



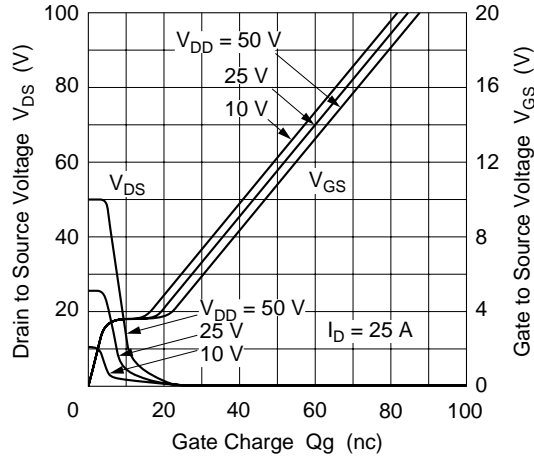
Body to Diode Reverse  
Recovery Time



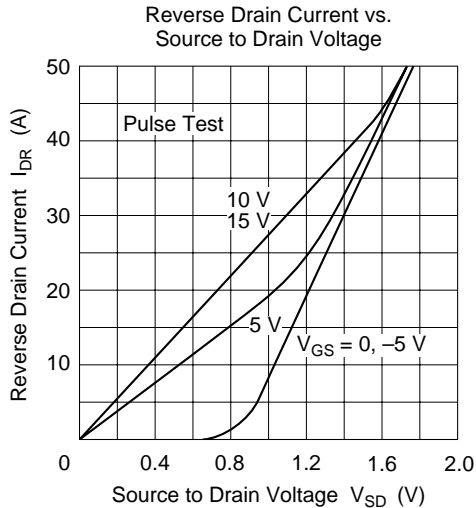
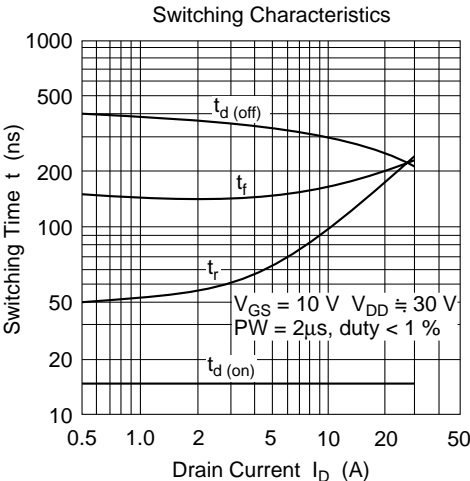
Typical Capacitance vs.  
Drain to Source Voltage



Dynamic Input Characteristics

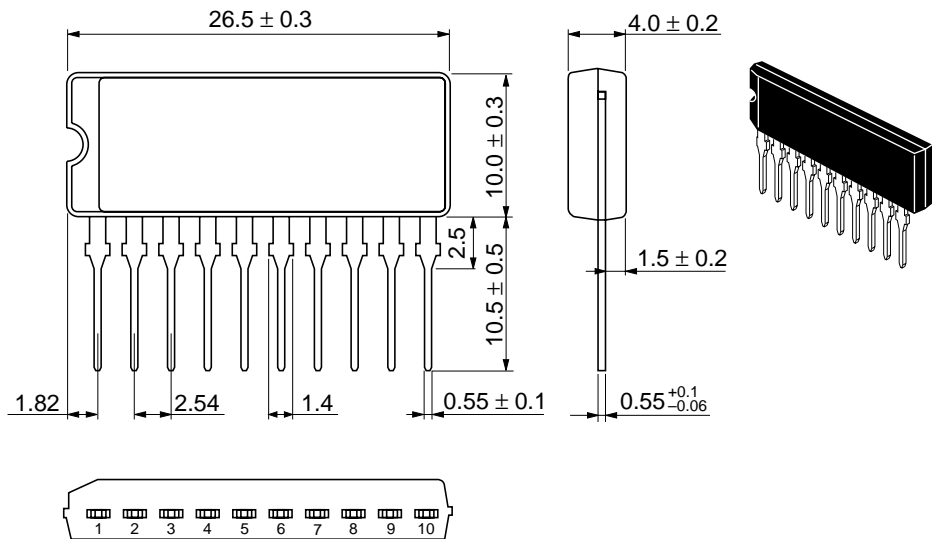






Package Dimensions

As of January, 2001  
Unit: mm



Hitachi Code	SP-10
JEDEC	—
EIAJ	—
Mass (reference value)	2.9 g

## Cautions

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