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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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4AK19

Silicon N Channel MOS FET High Speed Power Switching

RENESAS

ADE-208-727 (Z)

1st. Edition

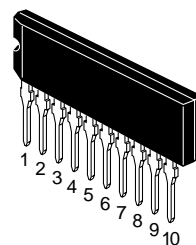
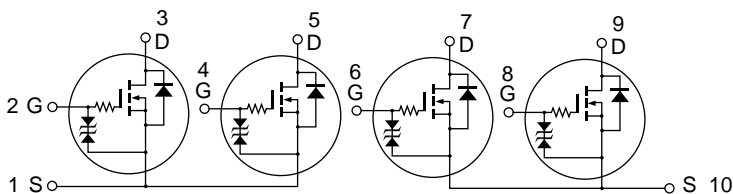
Feb. 1999

Features

- Low on-resistance
N Channel : $R_{DS(on)}$ $0.5\ \Omega$, $V_{GS} = 10V$, $I_D = 2.5A$
 $R_{DS(on)}$ $0.6\ \Omega$, $V_{GS} = 4V$, $I_D = 2.5A$
- 4V gate drive devices.
- High density mounting

Outline

SP-10



1, 10. Source
2, 4, 6, 8. Gate
3, 5, 7, 9. Drain

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	120	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_D	5	A
Drain peak current	$I_{D(pulse)}^{Note1}$	10	A
Body-drain diode reverse drain current	I_{DR}	5	A
Channel dissipation	$P_{ch}(T_c=25^{\circ}C)^{Note2}$	28	W
Channel dissipation	P_{ch}^{Note2}	3.5	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

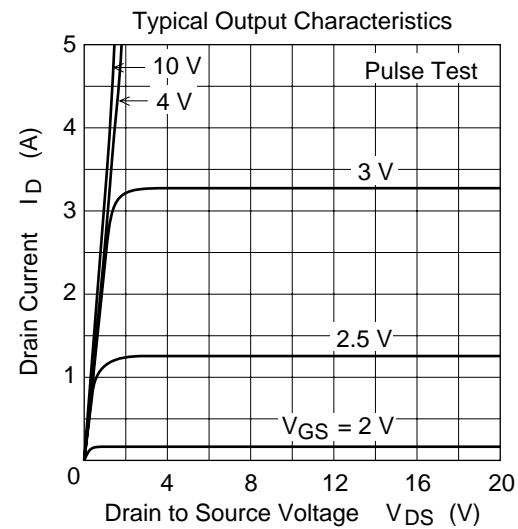
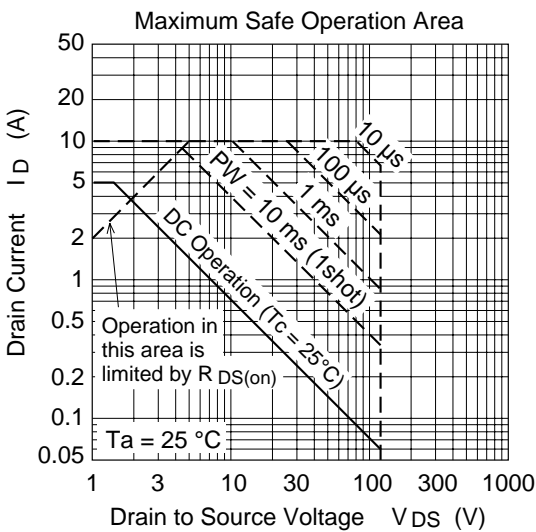
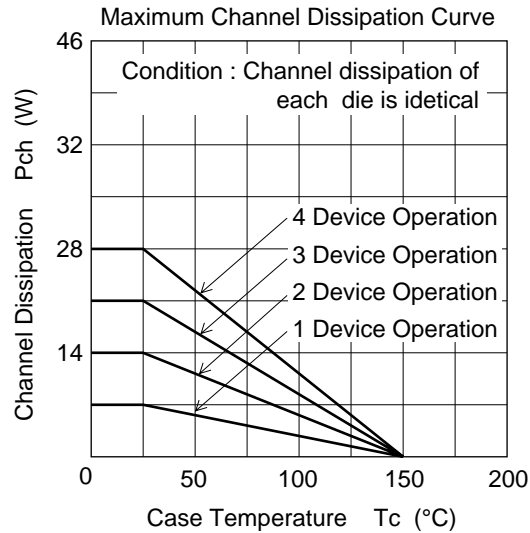
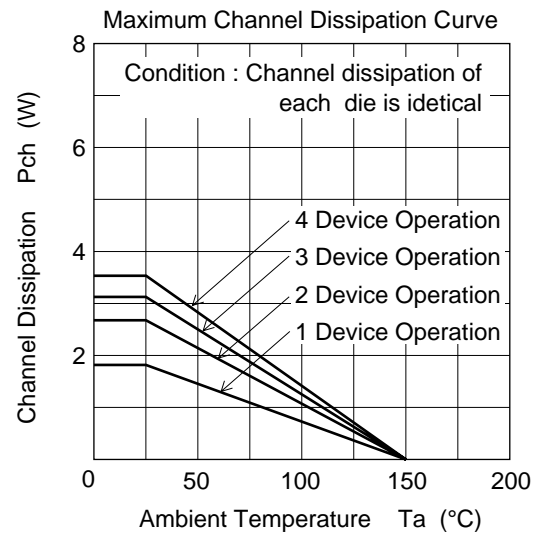
Note: 1. $PW \leq 10\mu s$, duty cycle $\leq 1\%$
2. 4 devices poeration

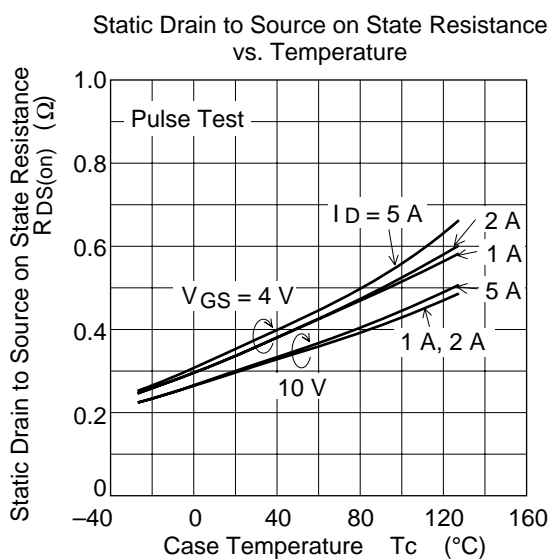
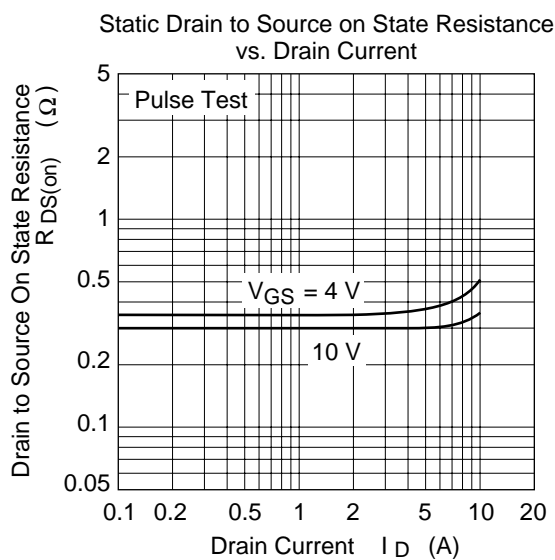
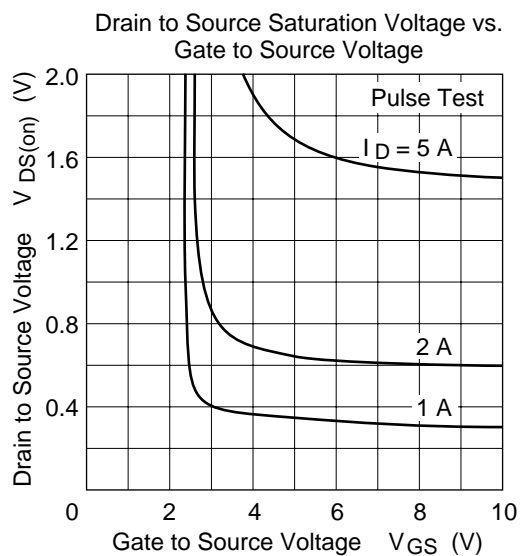
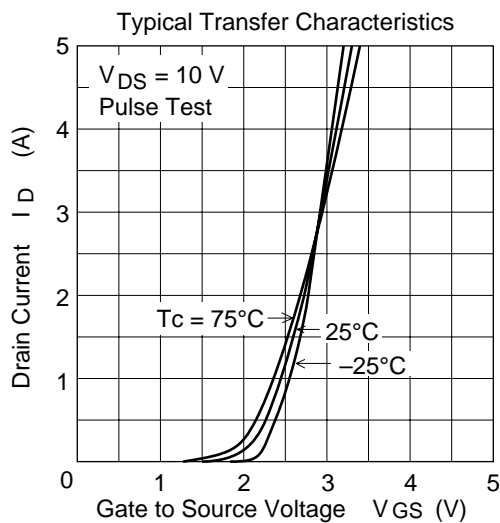
Electrical Characteristics (Ta = 25°C)

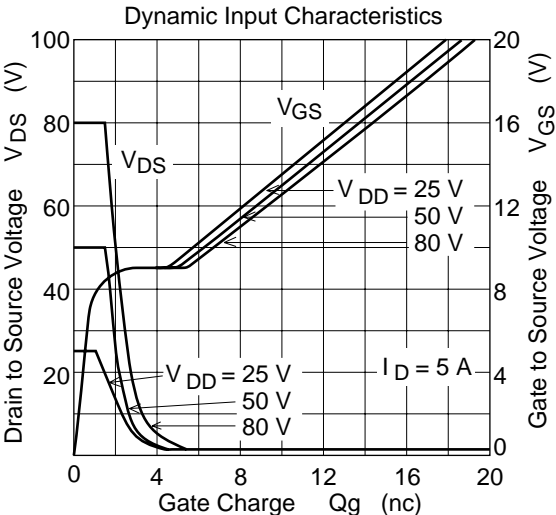
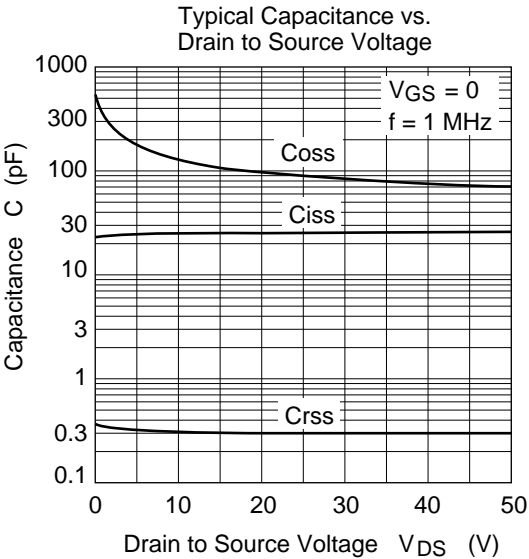
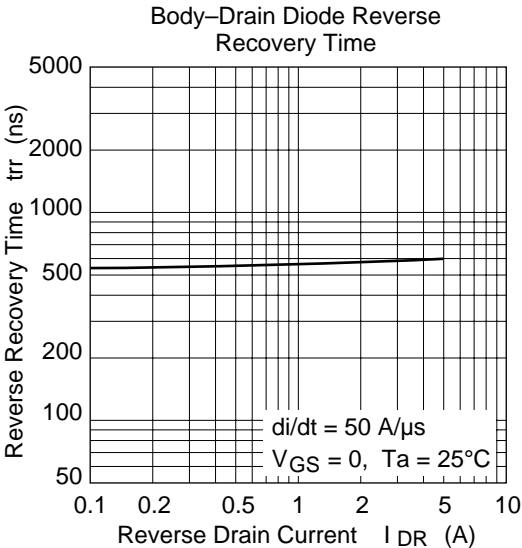
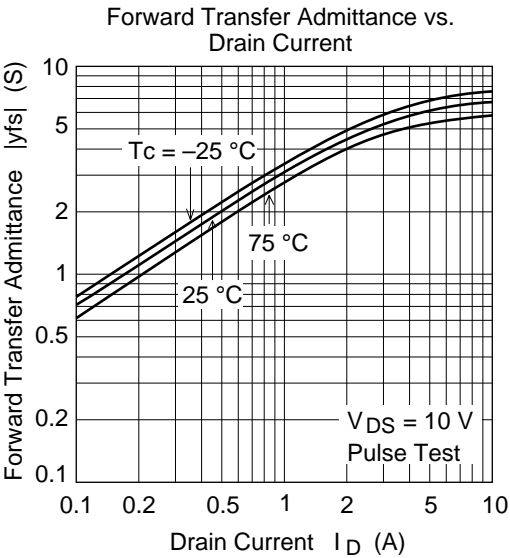
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	120	—	—	V	$I_D = 10\text{mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	$I_G = \pm 100\mu\text{A}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	100	μA	$V_{DS} = 100\text{V}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	±10	μA	$V_{GS} = \pm 16\text{V}$, $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	$I_D = 1\text{mA}$, $V_{DS} = 10\text{V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.3	0.5	Ω	$I_D = 2.5\text{A}$, $V_{GS} = 10\text{V}$ ^{Note3}
Static drain to source on state resistance	$R_{DS(on)}$	—	0.35	0.6	Ω	$I_D = 2.5\text{A}$, $V_{GS} = 4\text{V}$ ^{Note3}
Forward transfer admittance	$ y_{fs} $	3	5	—	S	$I_D = 2.5\text{A}$, $V_{DS} = 10\text{V}$ ^{Note3}
Input capacitance	C_{iss}	—	25	—	pF	$V_{DS} = 10\text{V}$
Output capacitance	C_{oss}	—	140	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	3	—	pF	$f = 1\text{MHz}$
Gate series resistance	R_g	—	2.5	—	kΩ	$V_{DS} = 0$, $V_{GS} = 0$, $f = 1\text{MHz}$
Turn-on delay time	$t_{d(on)}$	—	0.3	—	μs	$V_{GS} = 10\text{V}$, $I_D = 2.5\text{A}$
Rise time	t_r	—	0.45	—	μs	$R_L = 12\Omega$
Turn-off delay time	$t_{d(off)}$	—	6.6	—	μs	
Fall time	t_f	—	1.4	—	μs	
Body-drain diode forward voltage	V_{DF}	—	1.1	—	V	$I_F = 5\text{A}$, $V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	600	—	ns	$I_F = 5\text{A}$, $V_{GS} = 0$ $di_F/dt = 50\text{A}/\mu\text{s}$

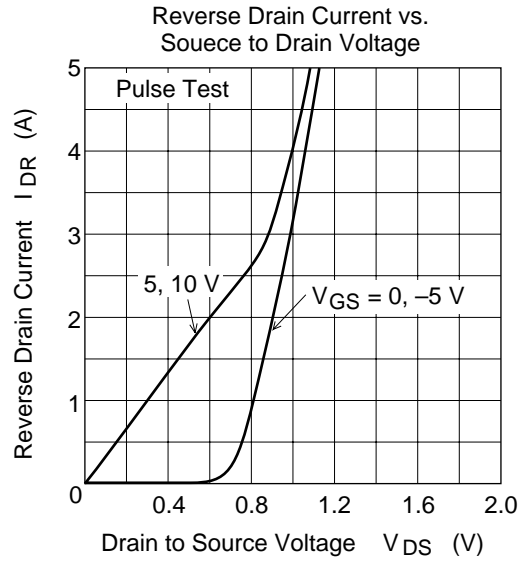
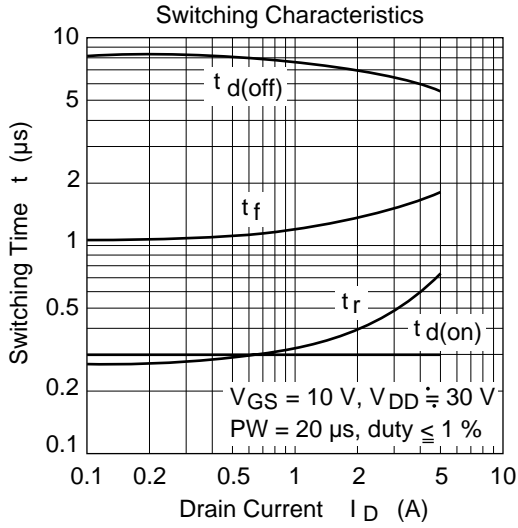
Note: 3. Pulse test

Main Characteristics

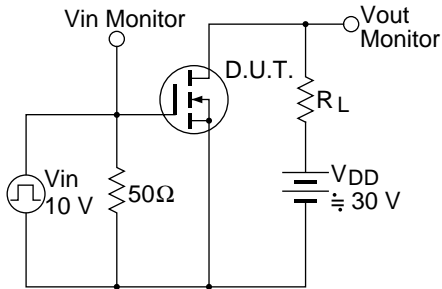




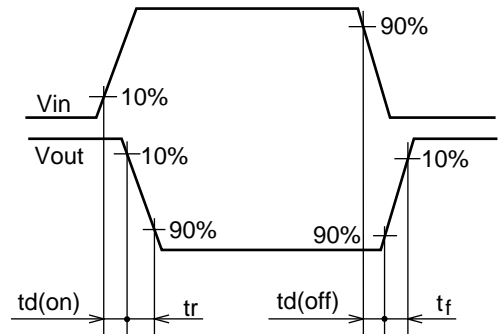




Switching Time Test Circuit

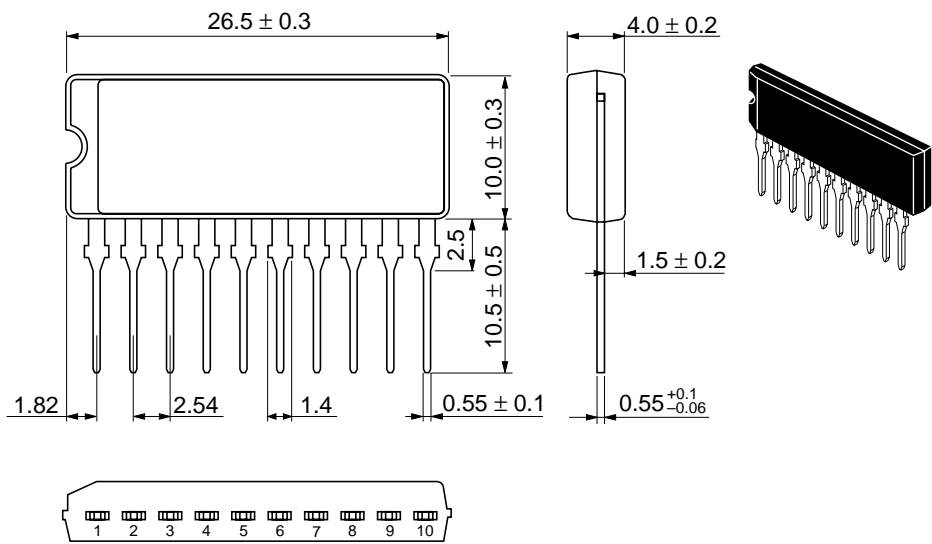


Waveform



Package Dimensions

As of January, 2001
Unit: mm



Hitachi Code	SP-10
JEDEC	—
EIAJ	—
Mass (reference value)	2.9 g

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