To all our customers

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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Keep safety first in your circuit designs!

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   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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2SJ186

Silicon P-Channel MOS FET

ADE-208-1184 (Z)
1st. Edition
Mar. 2001

Application

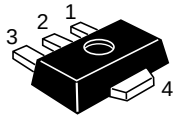
High speed power switching

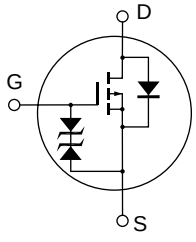
Features

- Low on-resistance
- High speed switching
- Low drive current
- Suitable for motor drive, DC-DC converter, power switch and solenoid drive

Outline

UPAK





1. Gate
2. Drain
3. Source
4. Drain

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–200	V
Gate to source voltage	V_{GSS}	±15	V
Drain current	I_D	–0.5	A
Drain peak current	$I_{D(pulse)}$*[1]	–1.0	A
Body to drain diode reverse drain current	I_{DR}	–0.5	A
Channel dissipation	Pch*[2]	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%
2. When using the alumina ceramic board (12.5×20×0.7 mm)

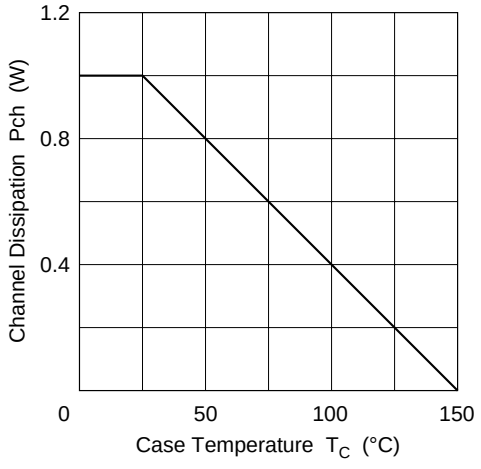
Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–200	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±15	—	—	V	I_G = ±100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±12 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	–50	µA	V_{DS} = –160 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–2.0	—	–4.0	V	I_D = –1 mA, V_{DS} = –10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	8.0	12.0	Ω	I_D = –0.25 A, V_{GS} = –10 V*[1]
		—	10.0	15.0		I_D = –1 A, V_{GS} = –10 V*[1]
Forward transfer admittance	$\|y_{fs}\|$	0.18	0.3	—	S	I_D = –0.25 A, V_{DS} = –10 V*[1]
Input capacitance	Ciss	—	75	—	pF	V_{DS} = –10 V, V_{GS} = 0, f = 1 MHz
Output capacitance	Coss	—	32	—	pF	
Reverse transfer capacitance	Crss	—	5	—	pF	
Turn-on delay time	$t_{d(on)}$	—	6	—	ns	I_D = –0.25 A, V_{GS} = –10 V, R_L = 120 Ω
Rise time	t_r	—	6	—	ns	
Turn-off delay time	$t_{d(off)}$	—	17	—	ns	
Fall time	t_f	—	15	—	ns	
Body to drain diode forward voltage	V_{DF}	—	0.95	—	V	I_F = –0.5 A, V_{GS} = 0
Body to drain diode reverse recovery time	t_{rr}	—	100	—	ns	I_F = –0.5 A, V_{GS} = 0, di_F/dt = 50 A/µs

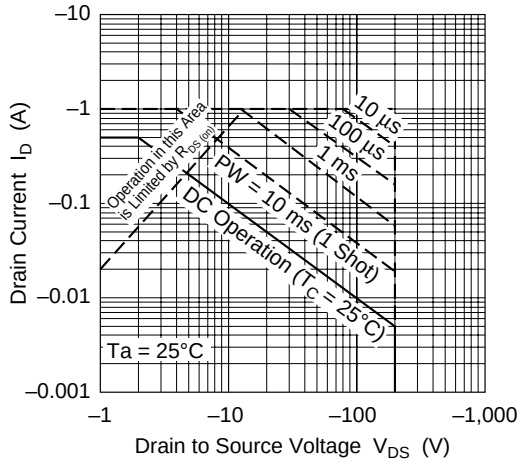
Note: 1. Pulse test

Marking for 2SJ186 is “CY”.

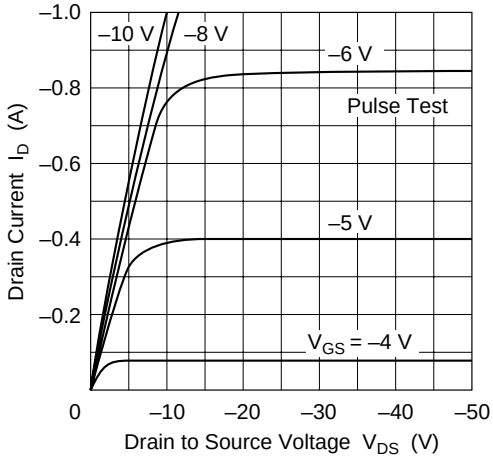
Power vs. Temperature Derating



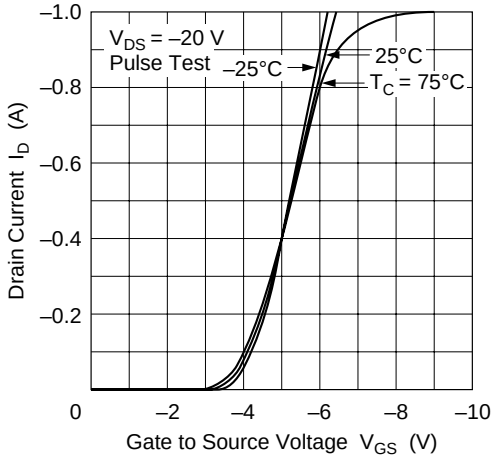
Maximum Safe Operation Area



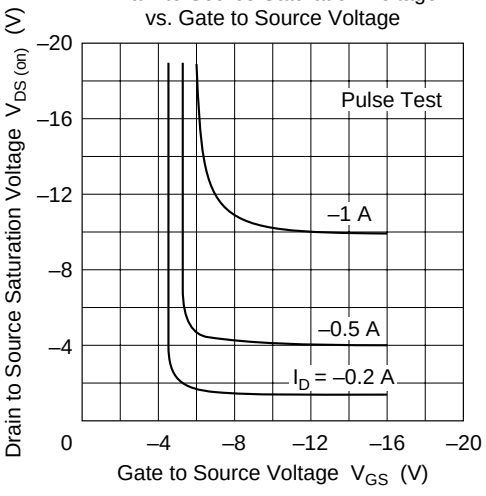
Typical Output Characteristics



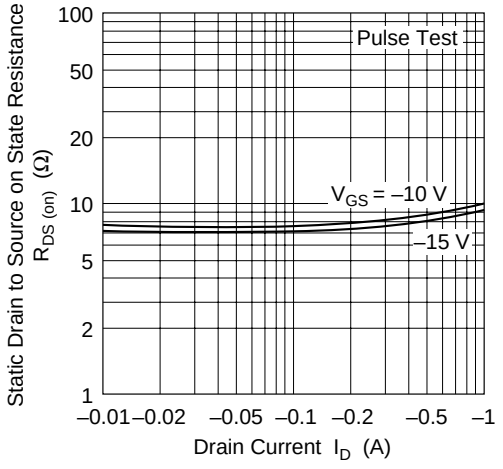
Typical Transfer Characteristics



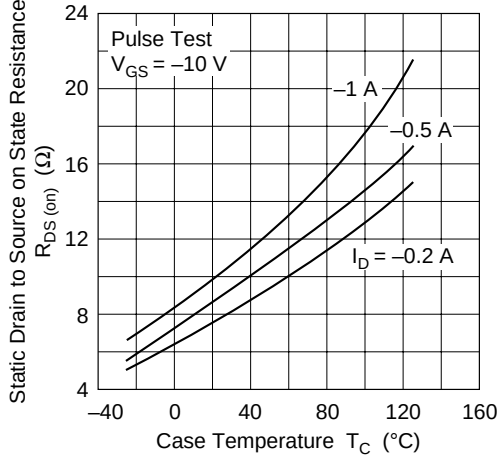
Drain to Source Saturation Voltage vs. Gate to Source Voltage



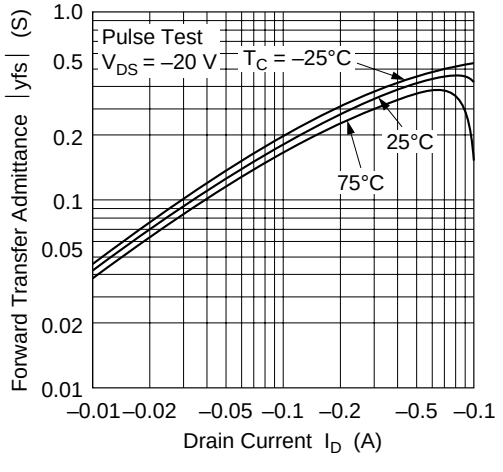
Static Drain to Source on State Resistance vs. Drain Current



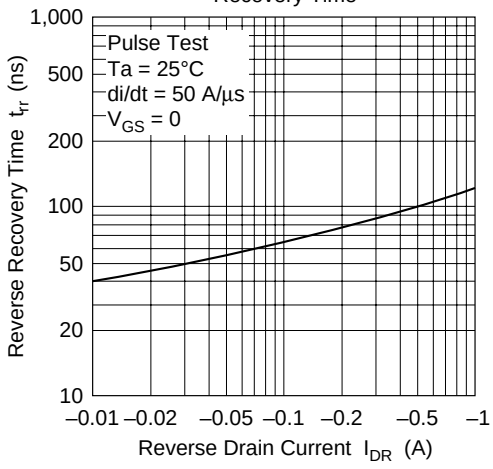
Static Drain to Source on State Resistance vs. Case Temperature



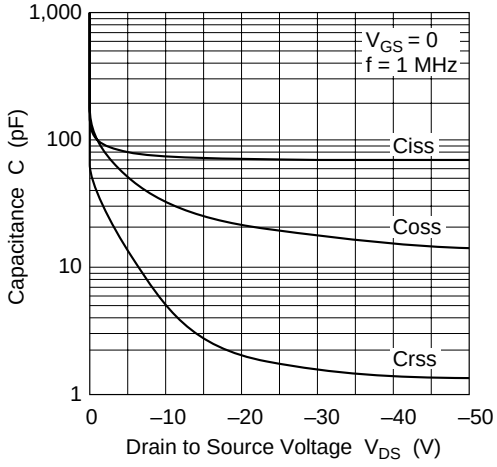
Forward Transfer Admittance vs. Drain Current



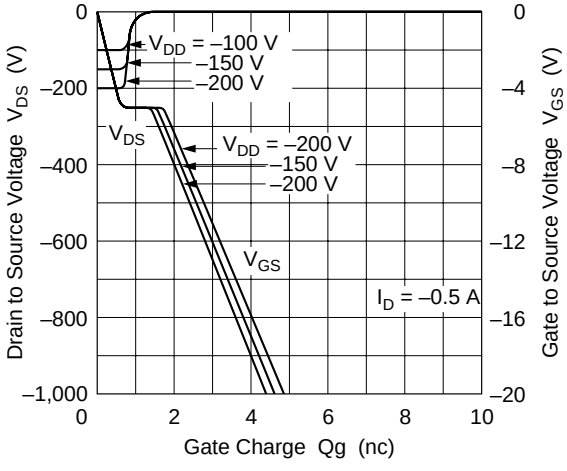
Body to Drain Diode Reverse Recovery Time



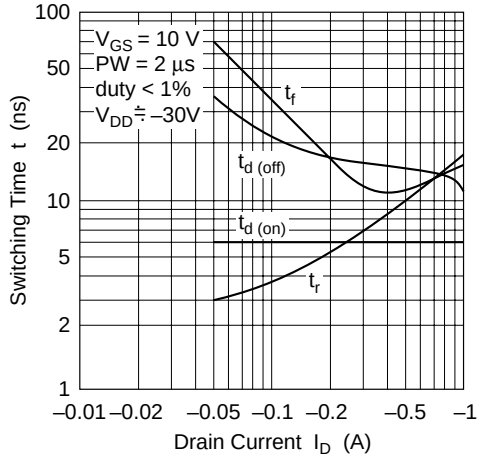
Capacitance vs. Drain to Source Voltage

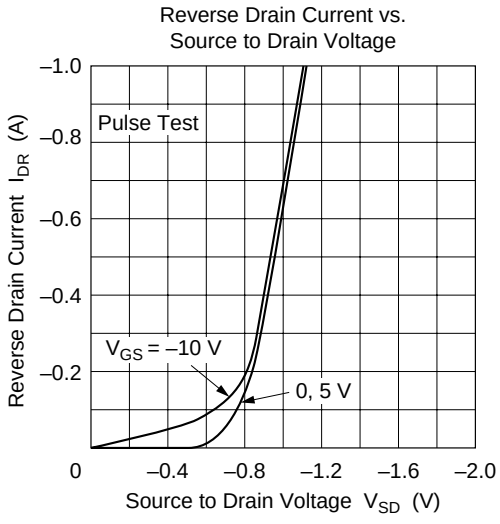


Dynamic Input Characteristics



Switching Characteristics

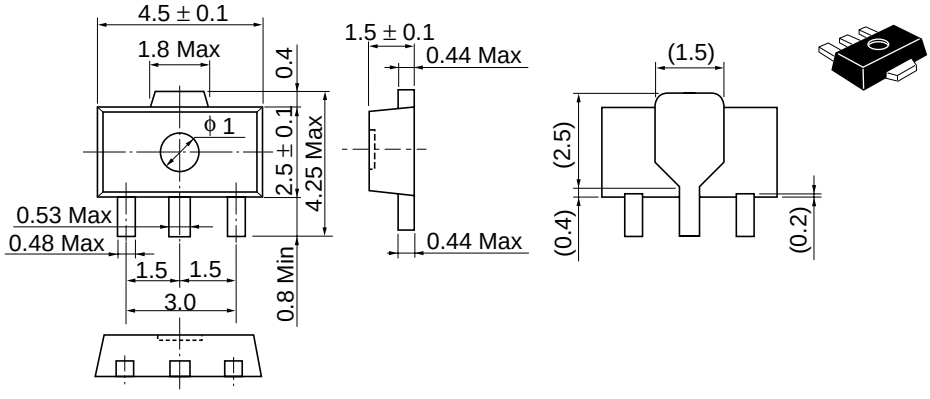



Reverse Drain Current vs.
Source to Drain Voltage
Pulse Test
Reverse Drain Current I_{DR} (A)
–1.0
–0.8
–0.6
–0.4
–0.2
0
V_{GS} = –10 V
0, 5 V
–0.4
–0.8
–1.2
–1.6
–2.0
Source to Drain Voltage V_{SD} (V)

Package Dimensions

As of January, 2001

Unit: mm



Hitachi Code	UPAK
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.050 g

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