To all our customers

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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BB503M

Build in Biasing Circuit MOS FET IC
UHF RF Amplifier

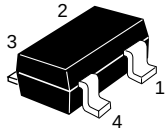
ADE-208-811C (Z)
4th. Edition
Mar. 2001

Features

- Build in Biasing Circuit; To reduce using parts cost & PC board space.
- Low noise; NF = 1.8 dB typ. at f = 900 MHz
- High gain; PG = 22 dB typ. at f = 900 MHz
- Withstanding to ESD;
  Build in ESD absorbing diode. Withstand up to 200V at C=200pF, Rs=0 conditions.
- Provide mini mold packages; MPAK-4(SOT-143Rmod)

Outline

MPAK-4



1. Source
2. Gate1
3. Gate2
4. Drain

Notes:
1. Marking is “CS–”.
2. BB503M is individual type number of HITACHI BBFET.

Absolute Maximum Ratings (Ta = 25°C)

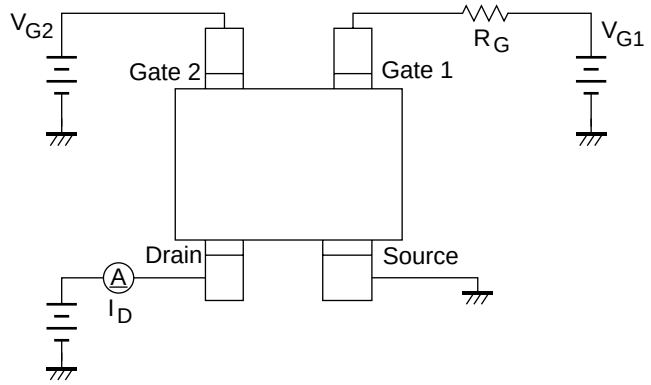
Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DS}	6	V
Gate1 to source voltage	V_{G1S}	+6	V
		–0	
Gate2 to source voltage	V_{G2S}	+6	V
		–0	
Drain current	I_D	20	mA
Channel power dissipation	Pch	150	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Electrical Characteristics (Ta = 25°C)

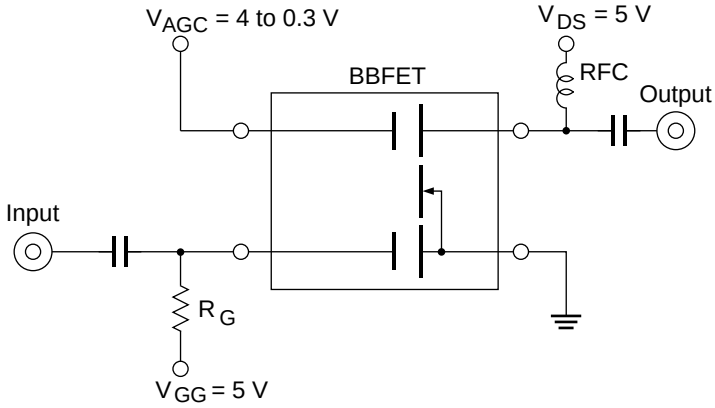
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	6	—	—	V	I_D = 200µA $V_{G1S} = V_{G2S}$ = 0
Gate1 to source breakdown voltage	$V_{(BR)G1SS}$	+6	—	—	V	I_{G1} = +10µA $V_{G2S} = V_{DS}$ = 0
Gate2 to source breakdown voltage	$V_{(BR)G2SS}$	+6	—	—	V	I_{G2} = +10µA $V_{G1S} = V_{DS}$ = 0
Gate1 to source cutoff current	I_{G1SS}	—	—	+100	nA	V_{G1S} = +5V $V_{G2S} = V_{DS}$ = 0
Gate2 to source cutoff current	I_{G2SS}	—	—	+100	nA	V_{G2S} = +5V $V_{G1S} = V_{DS}$ = 0
Gate1 to source cutoff voltage	$V_{G1S(off)}$	0.5	0.7	1.0	V	V_{DS} = 5V, V_{G2S} = 4V I_D = 100µA
Gate2 to source cutoff voltage	$V_{G2S(off)}$	0.5	0.7	1.0	V	V_{DS} = 5V, V_{G1S} = 5V I_D = 100µA
Drain current	$I_{D(op)}$	7	10	13	mA	V_{DS} = 5V, V_{G1} = 5V V_{G2S} = 4V, R_G = 47kΩ
Forward transfer admittance	$\|y_{fs}\|$	19	24	29	mS	V_{DS} = 5V, V_{G1} = 5V V_{G2S} =4V R_G = 47kΩ, f = 1kHz
Input capacitance	c_{iss}	1.4	1.7	2.0	pF	V_{DS} = 5V, V_{G1} = 5V
Output capacitance	c_{oss}	0.7	1.1	1.5	pF	V_{G2S} =4V, R_G = 47kΩ
Reverse transfer capacitance	c_{rss}	—	0.025	0.05	pF	f = 1MHz
Power gain	PG	17	22	—	dB	V_{DS} = 5V, V_{G1} = 5V V_{G2S} =4V, R_G = 47kΩ
Noise figure	NF	—	1.8	2.4	dB	f = 900MHz

Main Characteristics

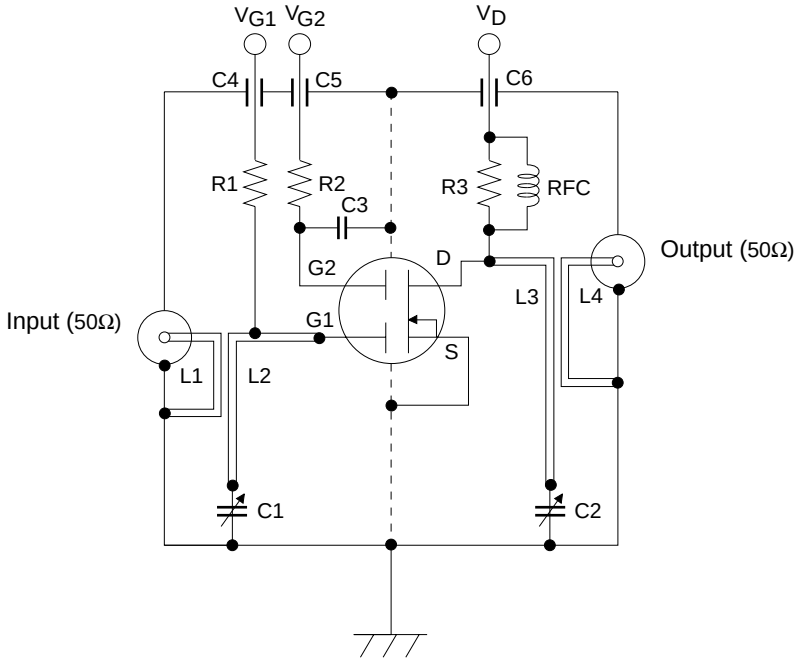
Test Circuit for Operating Items ($I_{D(op)}$, |yfs|, Ciss, Coss, Crss, NF, PG)



Application Circuit

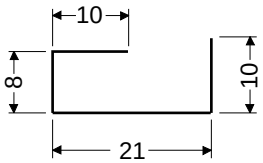


900MHz Power Gain, Noise Figure Test Circuit

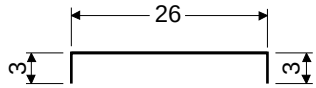


C1, C2: Variable Capacitor (10pF MAX)
C3: Disk Capacitor (1000pF)
C4 to C6: Air Capacitor (1000pF)
R1: 47 kΩ
R2: 47 kΩ
R3: 4.7 kΩ

L1:

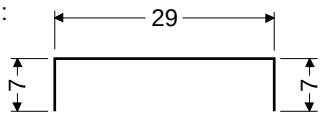


L2:

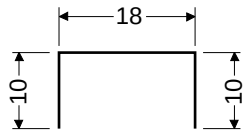


(ϕ1mm Copper wire)
Unit: mm

L3:

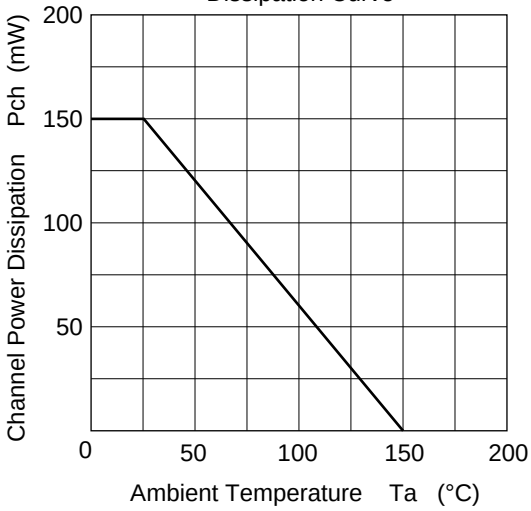


L4:

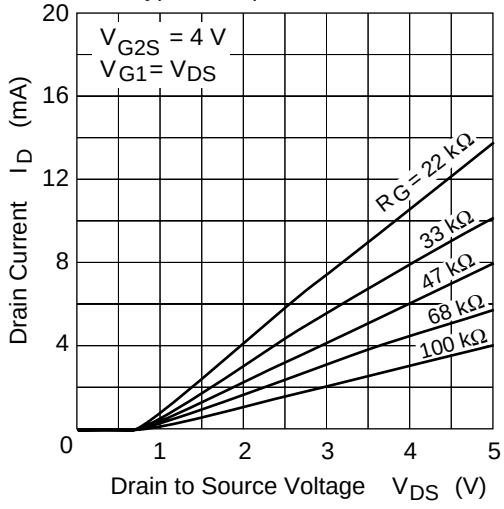


RFC: ϕ1mm Copper wire with enamel 4turns inside dia 6mm

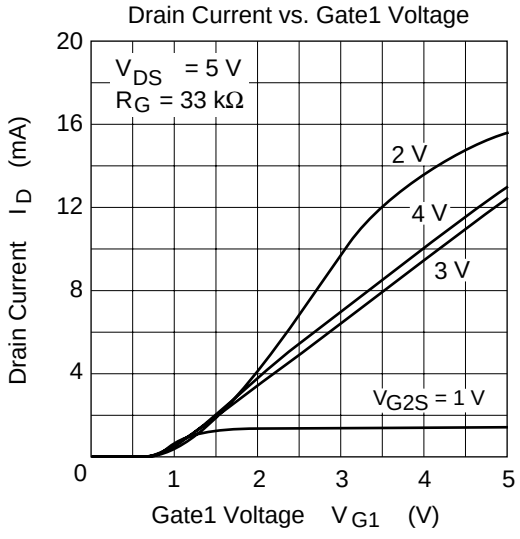
Maximum Channel Power Dissipation Curve



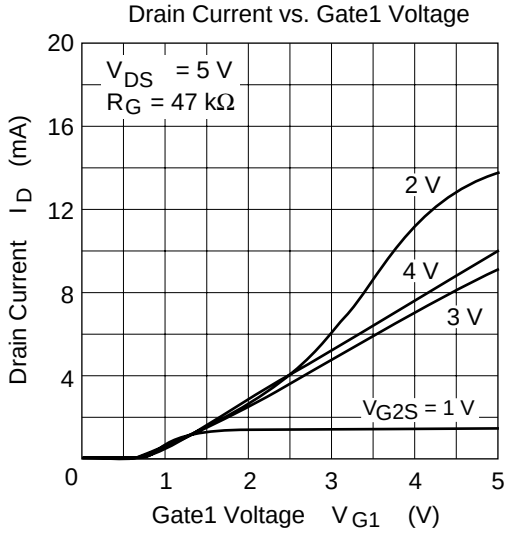
Typical Output Characteristics



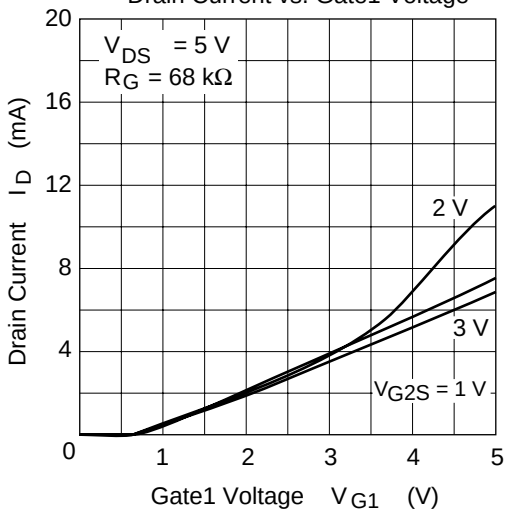
Drain Current vs. Gate1 Voltage



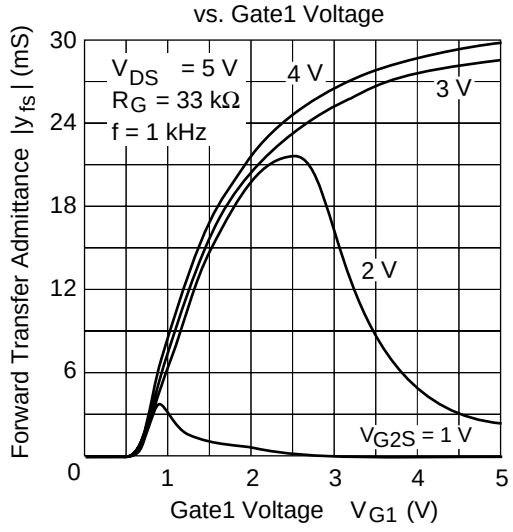
Drain Current vs. Gate1 Voltage



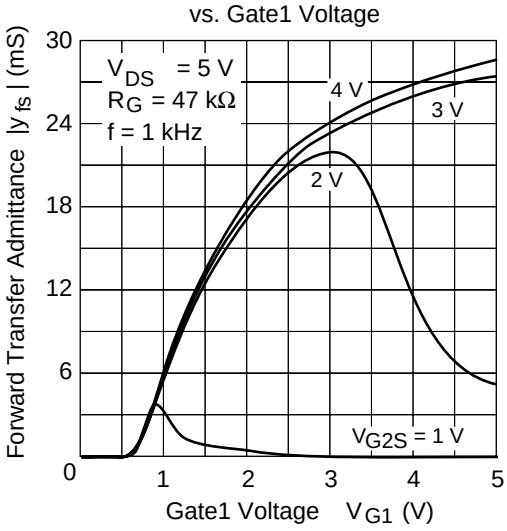
Drain Current vs. Gate1 Voltage



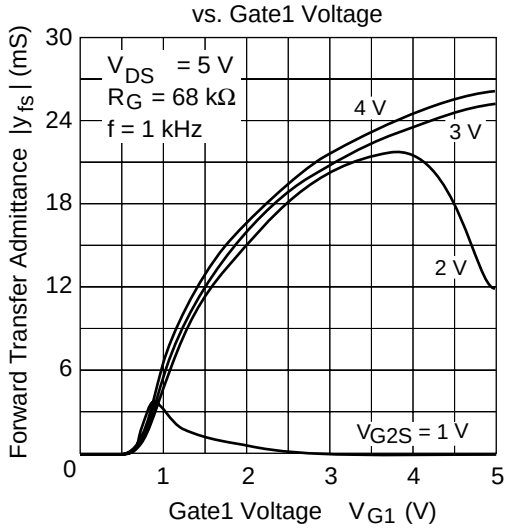
Forward Transfer Admittance vs. Gate1 Voltage



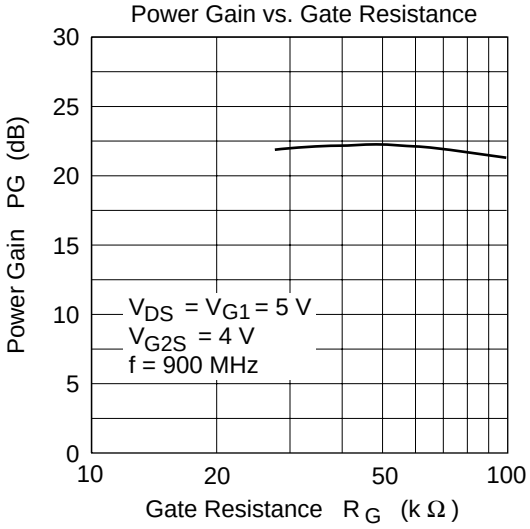
Forward Transfer Admittance vs. Gate1 Voltage



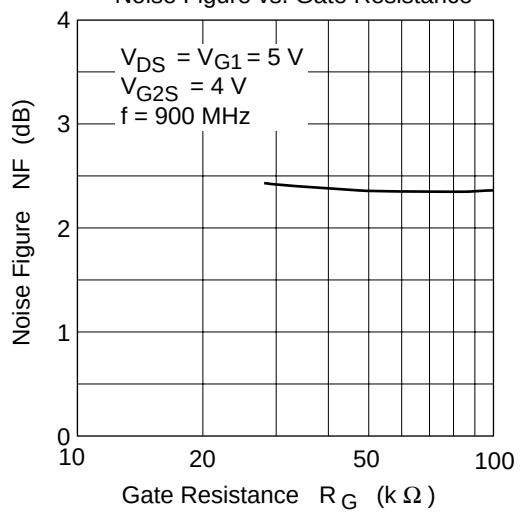
Forward Transfer Admittance vs. Gate1 Voltage



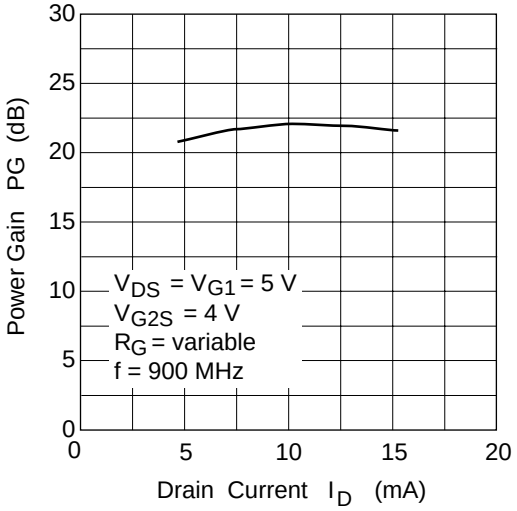
Power Gain vs. Gate Resistance



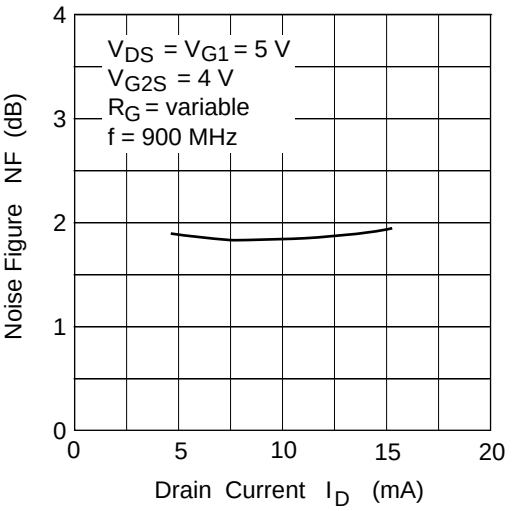
Noise Figure vs. Gate Resistance



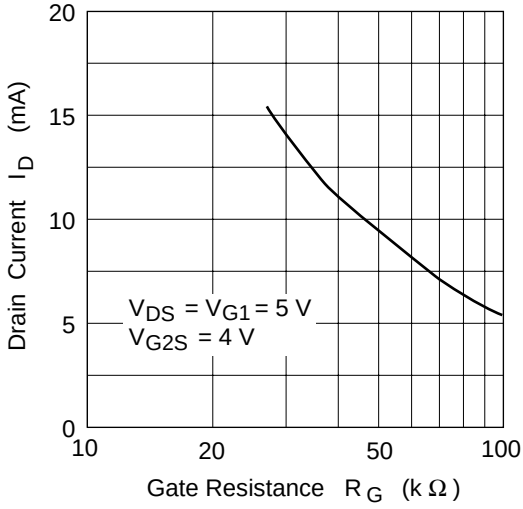
Power Gain vs. Drain Current



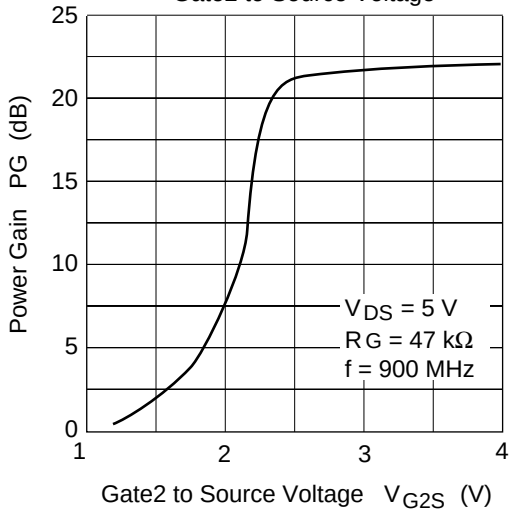
Noise Figure vs. Drain Current



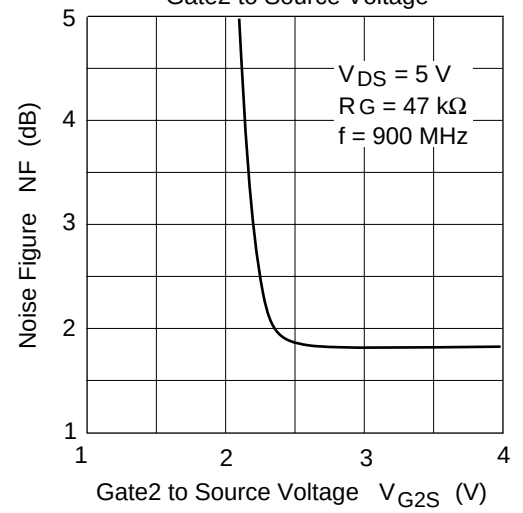
Drain Current vs. Gate Resistance



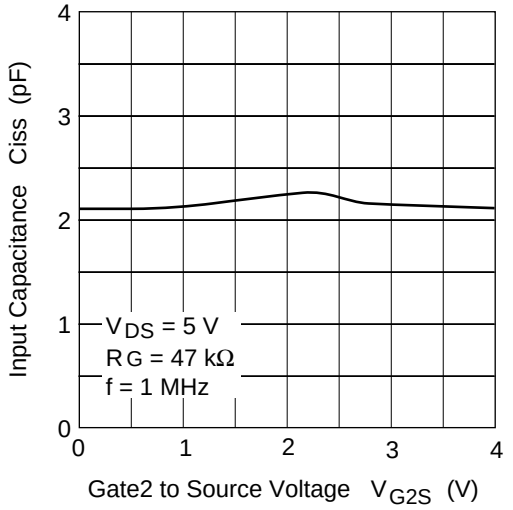
Power Gain vs.
Gate2 to Source Voltage

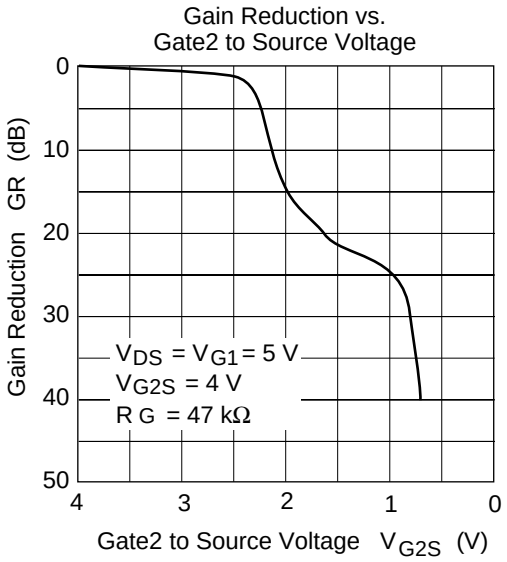


Noise Figure vs.
Gate2 to Source Voltage

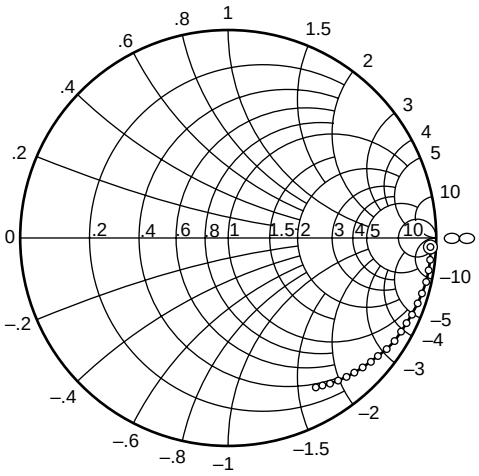


Input Capacitance vs.
Gate2 to Source Voltage




Gain Reduction vs.
Gate2 to Source Voltage
Gain Reduction GR (dB)
0
10
20
30
40
50
4
3
2
1
0
VDS = VG1 = 5 V
VG2S = 4 V
R G = 47 kΩ
Gate2 to Source Voltage VG2S (V)

S11 Parameter vs. Frequency

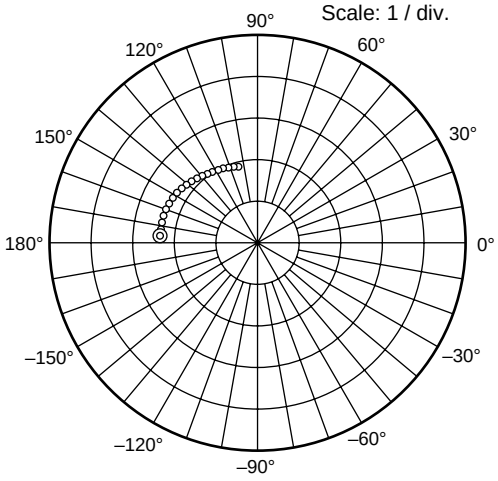


Test Condition: V_{DS} = 5 V , V_{G1} = 5 V
V_{G2S} = 4 V , R_G = 47 k Ω ,
Zo = 50 Ω

50 to 1000 MHz (50 MHz step)

S21 Parameter vs. Frequency

Scale: 1 / div.

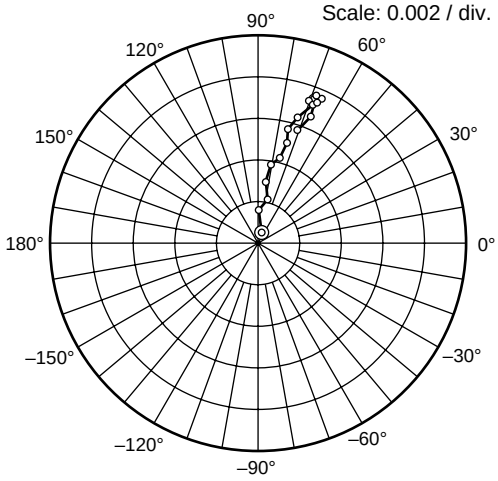


Test Condition: V_{DS} = 5 V , V_{G1} = 5 V
V_{G2S} = 4 V , R_G = 47 k Ω ,
Zo = 50 Ω

50 to 1000 MHz (50 MHz step)

S12 Parameter vs. Frequency

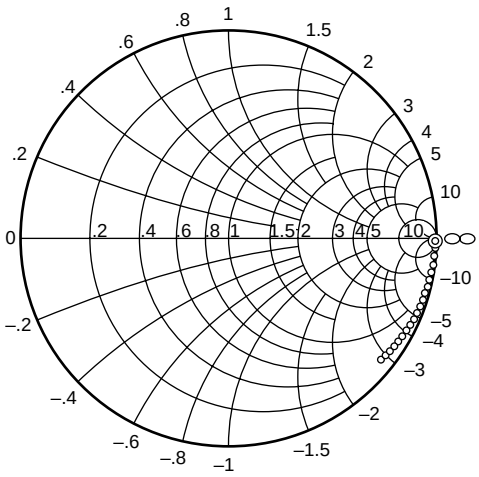
Scale: 0.002 / div.



Test Condition: V_{DS} = 5 V , V_{G1} = 5 V
V_{G2S} = 4 V , R_G = 47 k Ω ,
Zo = 50 Ω

50 to 1000 MHz (50 MHz step)

S22 Parameter vs. Frequency



Test Condition: V_{DS} = 5 V , V_{G1} = 5 V
V_{G2S} = 4 V , R_G = 47 k Ω ,
Zo = 50 Ω

50 to 1000 MHz (50 MHz step)

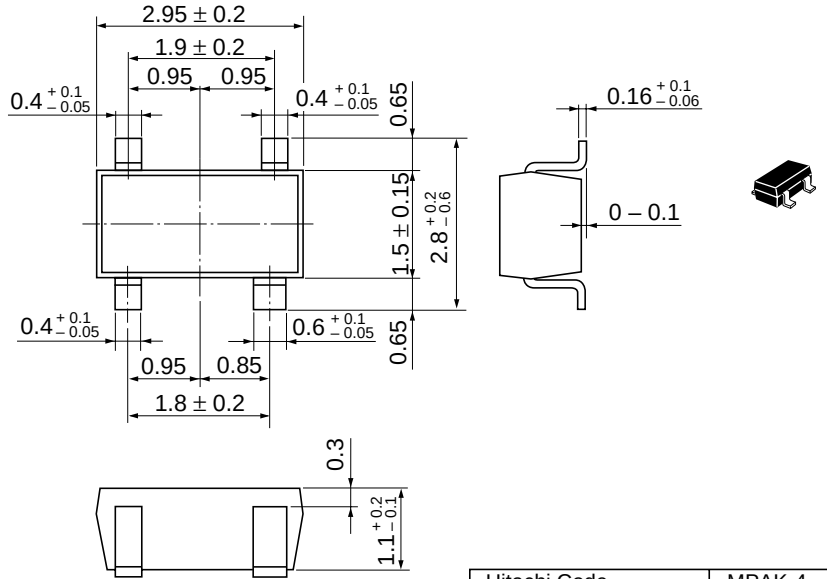
Sparameter (V_{DS} = V_{G1} = 5V, V_{G2S} = 4V, R_G = 47kΩ, Zo = 50Ω)

	S11		S21		S12		S22	
f (MHz)	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
50	0.975	–2.6	2.37	176.1	0.00097	74.4	0.995	–1.9
100	0.977	–6.5	2.37	172.1	0.00162	89.8	0.998	–3.9
150	0.975	–9.1	2.36	168.0	0.00222	78.2	0.997	–5.8
200	0.972	–12.4	2.33	163.8	0.00282	83.8	0.996	–8.0
250	0.968	–15.6	2.32	159.9	0.00388	81.1	0.994	–10.0
300	0.963	–18.9	2.30	156.0	0.00437	76.0	0.993	–11.8
350	0.954	–22.2	2.28	151.8	0.00518	73.6	0.991	–13.9
400	0.946	–25.3	2.25	148.2	0.00567	75.6	0.989	–15.8
450	0.937	–28.2	2.22	144.1	0.00631	72.5	0.986	–17.8
500	0.930	–31.5	2.19	140.2	0.00637	72.7	0.984	–19.6
550	0.920	–34.7	2.16	136.3	0.00720	70.3	0.981	–21.6
600	0.914	–37.4	2.13	132.7	0.00747	67.0	0.978	–23.4
650	0.902	–40.4	2.09	129.3	0.00738	69.2	0.975	–25.4
700	0.886	–43.5	2.07	125.4	0.00758	68.6	0.972	–27.3
750	0.879	–46.1	2.03	122.0	0.00757	66.0	0.968	–29.0
800	0.873	–48.9	1.99	118.3	0.00729	67.5	0.966	–31.0
850	0.857	–52.0	1.96	114.9	0.00723	68.8	0.962	–32.9
900	0.845	–54.5	1.93	111.4	0.00706	68.3	0.959	–34.8
950	0.838	–57.2	1.90	108.1	0.00659	67.5	0.954	–36.6
1000	0.824	–59.6	1.86	104.9	0.00574	71.0	0.952	–38.5

Package Dimensions

As of January, 2001

Unit: mm



Hitachi Code	MPAK-4
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.013 g

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