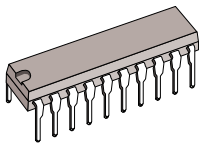
SGS-THOMSON MICROELECTRONICS

M5913

COMBINED SINGLE CHIP PCM CODEC AND FILTER

- SYNCHRONOUS CLOCKS ONLY
- AT&T D3/D4 AND CCITT COMPATIBLE
- TWO TIMING MODES:
  FIXED DATA RATE MODE 1.536MHz, 1.544MHz, 2.048MHz
  VARIABLE DATA MODE: 64KHz - 4.096MHz
- PIN SELECTABLE μ-LAW OR A-LAW OPERATION
- NO EXTERNAL COMPONENTS FOR SAMPLE-AND-HOLD AND AUTO ZERO FUNCTIONS
- LOW POWER DISSIPATION:
  0.5mW POWER DOWN
  70mW OPERATING
- EXCELLENT POWER SUPPLY REJECTION



DIP 20
ORDERING NUMBER: M5913B1

DESCRIPTION

The M5913 is fully integrated PCM (pulse code modulation) codecs and transmit/receive filter using CMOS silicon gate technology.

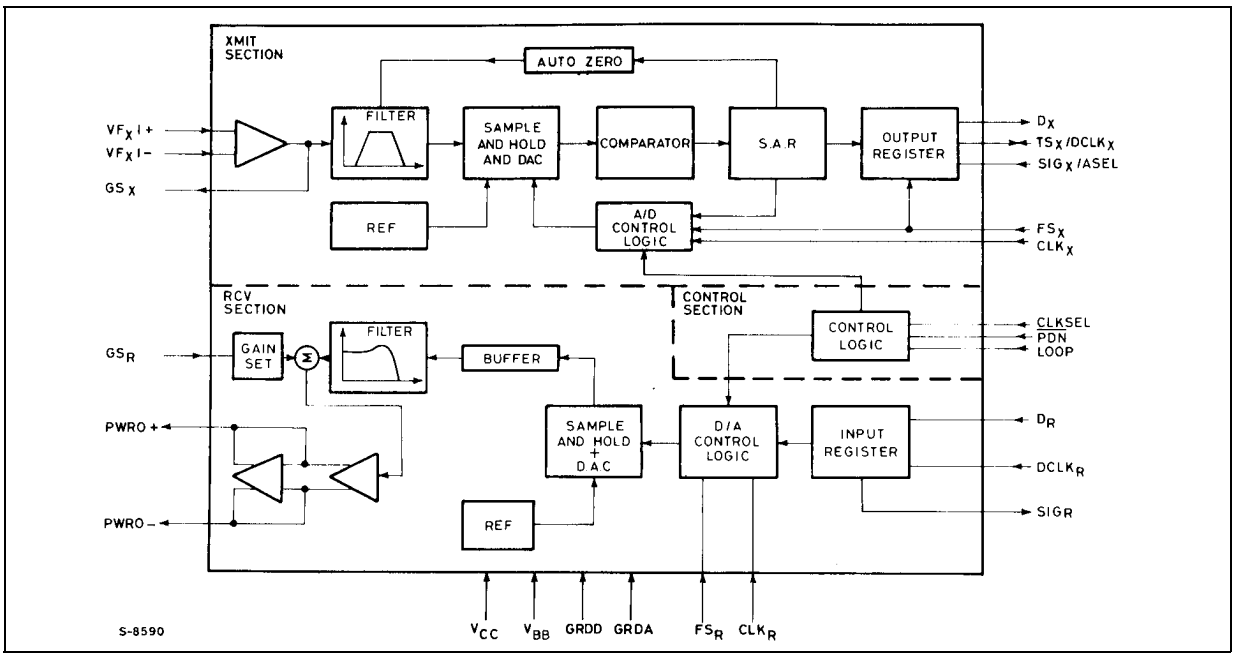
The primary applications for the M5913 are telephone systems :

- Switching - M5913-Digital PBX's and Central Office Switching Systems
- Concentration - M5913 Subscriber Carrier and Concentrators.

The wide dynamic range (78dB) and the minimal conversion time make it ideal products for other applications such as:

- Voice Store and Forward
- Secure Communications Systems
- Digital Echo Cancellers
- Satellite Earth Stations.

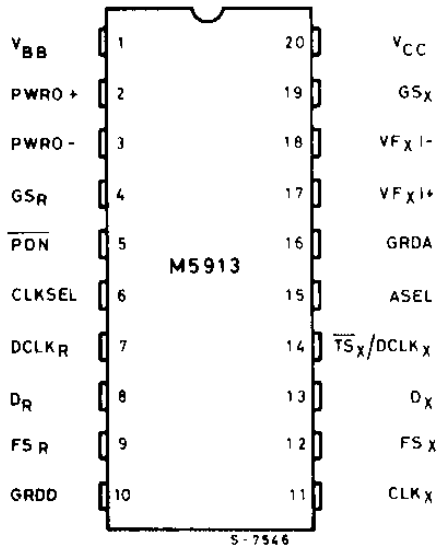
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	With Respect GRDD, GRDA = 0V	– 0.6 to 7	V
V_{BB}	With Respect GRDD, GRDA = 0V	- 0.6 to – 7	V
GRDD, GRDA	In Such Case : $0 \le V_{CC} \le +7V$, $-7V \le V_{BB} \le 0V$	± 0.3	V
$V_{I/O}$	Analog Inputs, Analog Outputs and Digital Inputs	$VBB - 0.3 \le V_{IN}/V_{OUT} \le V_{CC} + 0.3$	V
$V_{O\ DIG}$	Digital Outputs	$GRDD - 0.3 \le V_{OUT} \le V_{CC} + 0.3$	V
P_{tot}	Total Power Dissipation	1	W
T_{stg}	Storage Temperature Range	-65 to 150	°C

PIN CONNECTION (Top view)



PIN NAMES

Symbol	Parameter	Symbol	Parameter
V_{BB}	Power (-5V)	GS_X	Gain Control
PWRO+, PWRO-	Power Amplifier Outputs	VF_XI-, VF_XI+	Analog Inputs
GS_R	Gain Setting Input for receive Channel	GRDA	Analog Ground
$\overline{PDN}$	Power Pown Select	$\overline{NC}$	No Connected
CLKSEL	Master Clock Select	SIG_X	Transmit Digital Signaling Input
LOOP	Analog Loop Back	ASEL	μ or A-law Select
SIG_R	Signaling Bit Output	TS_X	Digital Output - Timeslot Strobe
$DCLK_R$	Receive Data Rate Clock	$DCLK_X$	Transmit Data Rate Clock
D_R	Receive Channel Input	D_X	Transmit (Digital) Output
FS_R	Receive Frame Synchronization Clock	FS_X	Transmit Frame Synchronization Clock
GRDD	Digital Ground	CLK_X	Transmit Master Clock
V_{CC}	Power (+5V)	CLK_R	Receive Master Clock

PIN DESCRIPTION

Symbol	Function
V_{BB}	Most Negative Supply. Input voltage is -5 volts ±5%.
PWRO+	Non-inverting Output of Power Amplifier. Can drive transformer hybrids or high impedance loads directly in either a differential or single ended configuration.
PWRO -	Inverting Output of Power Amplifier. Functionally identical and complementary to PWRO+.
GS_R	Input to the gain Setting Network on the Output Power Amplifier, Transmission level can be adjusted over a 12dB range depending on the voltage at GS_R.
$\overline{PDN}$	Power Down Select. When PDN is TTL high, the device is active.When low, the device is powered down.
CLKSEL	input which must be pinstrapped to reflect the master clock frequency at CLK_X, CLK_R. CLKSEL = V_{BB} 2.048MHz CLKSEL = GRDD 1.544MHz CLKSEL = V_{CC} 1.536MHz
LOOP	Analog Loopback. When this pin is TTL high, the receive output (PWRO+) is internally connected to VF_XI+, GS_R is internally connected to PWRO-, and VF_XI- is internally connected to GS_X. A 0dBm0 digital signal input at D_R is returned as a +3dBm0 digital signal output at D_X.
SIG_R	Signalling Bit Output, Receive Channel. In fixed data rate mode. SIG_R outputs the logical state of the eighth bit of the PCM word in the most recent signaling frame.
$DCLK_R$	Selects the fixed or variable data rate mode. When DCLKR is connected to V_{BB}, the fixed data rate mode is selected. When $DCLK_R$ is not connected to V_{BB}, the device operates in the variable data rate mode. In this mode $DCLK_R$ becomes the receive data clock wich operates at TTL levels from 64kB to 4.096MB data rates
D_R	Receive PCM Input. PCM data is clocked in on this lead on eight consecutive negative transitions of the receive data clock: CLKR in the fixed data rate mode and $DCLK_R$ in variable data rate mode.
FS_R	8kHz frame synchronization clock input/timeslot enable, receive channel. A multifunction input which in fixed data rate mode distinguishes between signaling and non-signaling frames by means of a double or single wide pulse respectively. In variable data rate mode this signal must remain high for the entire length of the timeslot. The receive channel enters the standby state whenever FSR is TTL low for 30 miliseconds
GRDD	Digital Ground for all Internal Logic Circuits. Not internally tied to GRDA.
CLK_R	Receive master and data clock for the fixed data rate mode; receive master clock only in variable data rate mode.
CLK_X	Transmit master and data clock for the fixed data rate mode; transmit master clock only in variable data rate mode.
FS_X	8kHz frame synchronization clock input/timeslot enable, transmit channel. Operates independently but in an analogous manner to FSR. The transmit channel enters the standby state whenever FS_X is TTL low for 30 milliseconds.
D_X	Transmit PCM Output. PCM data is clocked out on this lead on eight consecutive positive transitions of the transmit data clock : CLK in fixed data rate mode and $DCLK_X$ in variable data rate mode.
$\overline{TS_X}/DCLK_X$	Transmit channel timeslot strobe (output) or data clock (input) for the transmit channel. In fixed data rate mode, this pin becomes the transmit data clock which operates at TTL levels from 64kB to 4.096MB data rates.
SIG_X/ASEL	A dual purpose selects μ-law and pin. When connected to V_{BB}. A law operation is selected. When it is not connected to V_{BB} pin is a TTL level input for signaling operation. This input is transmitted as the eighth bit of the PCM word during signaling frames on the D_X lead.
NC	Not Connected.
GRDA	Analog ground return for all internal voice circuits. Not internally connected to GRDD.
VF_XI+	Non inverting analog input to uncommitted transmit operational amplifier.
VF_XI-	Inverting analog input to uncommitted transmit operational amplifier.
GS_X	Output terminal of on-chip uncommitted op amp. Internally, this is the voice signal input to the transmit filter.
V_{CC}	Most positive supply ; input voltage is + 5 volts ±5%

FUNCTIONAL DESCRIPTION

The M5913 provides the analog-to-digital and the digital-to-analog conversion and the transmit and receive filtering necessary to interface a full duplex (4 wires) voice telephone circuit with the PCM highway of a time division multiplexed (TDM) system. It is intended to be used at the analog termination of a PCM line.

The following major functions are provided :

- Bandpass filtering of the analog signals prior to encoding and after decoding
- Encoding and decoding of voice and call progress information
- Encoding and decoding of the signaling and supervision information

GENERAL OPERATION

System Reliability Features

The combo-chip can be powered up by pulsing FS_X and/or FS_R while a TTL high voltage is applied to $\overline{PDN}$, provided that all clocks and supplies are connected. The M5913 has internal resets on power up (or when V_{BB} or V_{CC} are re-applied) in order to ensure validity of the digital outputs and thereby maintain integrity of the PCM highway.

On the transmit channel, digital outputs D_X and $\overline{TS}_X$ are held in a high impedance state for approximately four frames (500µs) after power up or application of V_{BB} or V_{CC}. After this delay, D_X and $\overline{TS}_X$ will be functional and will occur in the proper timeslot. The analog circuits on the transmit side require approximately 40 milliseconds to reach their equilibrium value due to the autozero circuit setting time. Thus, valid digital information, such as for on/off hook detection, is available almost immediately, while analog information is available after some delay.

On the receive channel, the digital output SIG_R is also held low for a maximum of four frames after power up or application of V_{BB} or V_{CC}, SIG_R will remain low thereafter until it is updated by a signaling frame.

To further enhance system reliability, $\overline{TS}_X$ and $\overline{D_X}$ will be placed in a high impedance state approximately 20µs after an interruption of CLK_X. Similarly SIG_R will be held low approximately 20µs after an interruption of CLK_R. These interruptions could possibly occur with some kind of fault condition.

Power Down And Standby Modes

To minimize power consumption, two power down modes are provided in which most M5913 functions are disabled. Only the power down, clock, and frame sync buffers, which are required to power up the device, are enabled in these modes. As shown in table 1, the digital outputs on the appropriate channels are placed in a high impedance state until the device returns to the active mode.

The Power Down mode utilizes an external control signal to the $\overline{PDN}$ pin. In this mode, power consumption is reduced to an average of 0.5mW. The device is active when the signal is high and inactive when it is low. In the absence of any signal, the $\overline{PDN}$ pin floats to TTL high allowing the device to remain active continuously.

The Standby mode leaves the user an option of powering either channel down separately or powering the entire down by selectively removing FS_X and/or FS_R. With both channels in the standby state, power consumption is reduced to an average of 1mW. If transmit only operation is desired, FS_X should be applied to the device while FS_R is held low. Similarly, if receive only operation is desired, FS_R should be applied while FS_X is held low.

Fixed Data Rate Mode

Fixed data rate timing, is selected by connecting $DCLK_R$ to V_{BB}. It employs master clock CLK_X, and CLK_R, frame synchronization clocks FS_X and FS_R, and output $\overline{TS}_X$.

CLK_X, and CLK_R, serve both as the master clock to operate the codec and filter sections and bit clocks to clock the data in and out from the PCM highway. FS_X and FS_R are 8kHz inputs which set the sampling frequency and distinguish between signaling and non-signaling frames by thir pulse width. A frame synchronization pulse which is one master clock wide designates a non-signaling frame, while a double wide sync pulse enables

Table 1: Power Down Methods

Device Status	Power Down Methods	Digital Outputs Status
Power Down Mode	$\overline{PDN}$ = TTL low	$\overline{TS}_X$ and D_X are placed in a high impedance state and SIG_R is placed in a TTL low state within 10µs.
Stand-by Mode	FS_X and FS_R are TTL low	$\overline{TS}_X$ and D_X are placed in a high impedance state and SIG_R is placed in a TTL low state 30ms after FS_X and FS_R are removed.
Only transmit is on stand-by	FS_X is TTL low	$\overline{TS}_X$ and D_X are placed in a high impedance state within 30ms.
Only receive is on stand-by	FS_R is TTL low	SIG_R is placed in a TTL low state within 30ms.

the signaling function. TS_X is a timeslot strobe/buffer enable output which gates the PCM word onto the PCM highway when an external buffer is used to drive the line.

Data is transmitted on the highway at D_X on the first eight positive transitions of CLK_X following the rising edge of FS_X. Similarly, on the receive side, data is received on the first eight falling edges of CLK_R. The frequency of CLK_X and CLK_R is selected by the CLKSEL pin to be either 1.536, 1.544 or 2.048MHz. No other frequency of operation is allowed in the fixed data rate mode.

Variable Data Rate Mode

Variable data rate timing is selected by connecting $DCLK_R$ to the bit clock for the receive PCM highway rather than to V_{BB}. It employes master clocks CLK_X and CLK_R, bit clocks $DCLK_R$ and $DCLK_X$ and frame synchronization clocks FS_R and FS_X.

Variable data rate timing allows for a flexible data frequency. It provides the ability to vary the frequency of the bit clocks, from 64kHz to 4096MHz. Master clocks inputs are still restricted to 1.536, 1.544, or 2.048MHz.

In this mode, $DCLK_R$ and $DCLK_X$ become the data clocks for the receive and transmit PCM highways. While FS_X is high, PCM data from D_X is transmitted onto the highway on the next eight consecutive positive transitions of $DCLK_X$. Similarly, while FS_R is high, each PCM bit from the highway is received by D_R on the next eight consecutive negative transitions of $DCLK_R$.

On the transmit side, the PCM word will be repeated in all remaining timeslots in the 125µs frame as long as $DCLK_X$ is pulsed and FS_X is held high. This feature allows the PCM word to be transmitted to the PCM highway more than once per frame, if desired, and is only available in the variable data rate mode. Conversely, signaling is only allowed in the fixed data rate mode since the variable mode provides no means with which to specify a signaling frame.

Precision Voltage References

No external components are required with the combochip to provide the voltage reference function. Voltage references are generated on-chip and are calibrated during the manufacturing process. The technique use the bandgap principle to derive a temperature and bias stable reference voltage. These references determine the gain and dynamic range characteristics of the device.

Separate references are supplied to the transmit and receive sections. Transmit and receive section are trimmed independently in the filter stages to a final precision value. With this method the combochip can achieve manufacturing tolerances of typically ± 0.04dB in absolute gain for each half channel, providing the user a significant margin for error in other board components.

Conversion Laws

The M5913 is designed to operate in both µ-law and A-law systems. The user can select either conversion law according to the voltage present on the SIG_X/ASEL pin . In each case the coder and decoder process a companded 8-bit PCM word following CCITT recommandation G.711 for µ-law and A-law conversion. If A-law operation is desired, SIG_X should be tied to V_{BB}. Thus, signaling is not allowed during A-law operation. If µ = 255-law operation is selected, then SIG_X is a TTL level input which modifies the LSB on the PCM output in signaling frames

TRANSMIT OPERATION

Transmit Filter

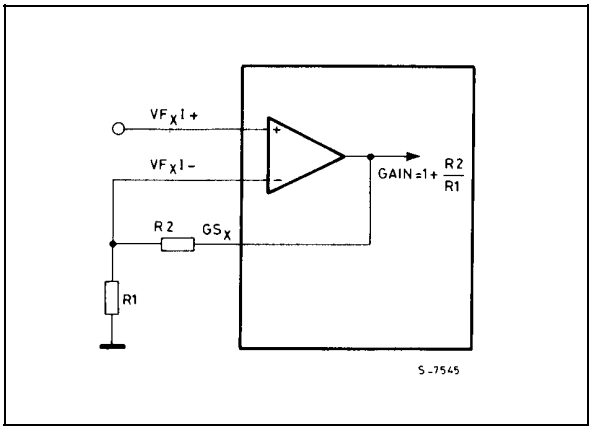
The input section provides gain adjustment in the passband by means of an on-chip uncommitted operational amplifier. This operational amplifier has a common mode range of 2.17V, a maximum DC offset of 25mV, a minimum voltage gain of 5000, and a unity gain bandwidth of typically 1MHz. Gain of up to 20dB can be set without degrading the performance of the filter. The load impedance to ground (GRDA) at the amplifier output (GS_X) must be greater than 10kΩ in parallel high less than 50pF. The input signal on lead VF_XI+ can be either AC or DC coupled. The input op amp can also be used in the inverting mode or differential amplifier mode (see figure 3).

A low pass anti-aliasing section is included on-chip. This section typically provides 35dB attenuation at the sampling frequency. No external components are required to provide the necessary anti-aliasing function for the switched capacitor section of the transmit filter.

The passband section provides flatness and stopband attenuation which fulfills the AT&T D3/D4 channel bank transmission specification and CCITT recommendation G.712.
The M5913 specifications meet or exceed digital class 5 central office switching systems requirements. The transmit filter transfer characteristics and specifications will be within the limits shown the relative table.

A high pass section configuration was chosen to reject low frequency noise from 50 and 60Hz power lines, 17Hz European electric railroads, ringing frequencies and their harmonics, and other low frequency noise.
Even though there is high rejection at these frequencies, the sharpness of the band edge gives low attenuation at 200Hz. This feature allows the use of low-cost transformer hybrids without external components.

Figure 3: Transmit Filter Gain Adjustment.



Encoding

The encoder internally samples the output of the transmit filter and holds each sample on an internal sample and hold capacitor.
The encoder then performs an analog to digital conversion on a switched capacitor array. Digital data representing the sample is transmitted on the first eight data clock bits of the next frame.

An on-chip autozero circuit corrects for DC-offset on the input signal to the encoder. This autozero circuit uses the sign bit averaging technique. In this way, all DC offset is removed from the encoder input waveform.

RECEIVE OPERATION

Decoding

The PCM word at the D_R lead is serially fetched on the first eight data clock bits of the frame.
A D/A conversion is performed on the digital word and the corresponding analog sample is held on an internal sample and hold capacitor. This sample is then transferred to the receive filter.

Receive Filter

The receive section of the filter provides passband flatness and stopband rejection which fulfills both the AT&T D3/D4 specification and CCITT recommendation G.712. The filter contains the required compensation for the (sin X)/X response of such decoders. The receive filter characteristics and specifications are shown in the relative table.

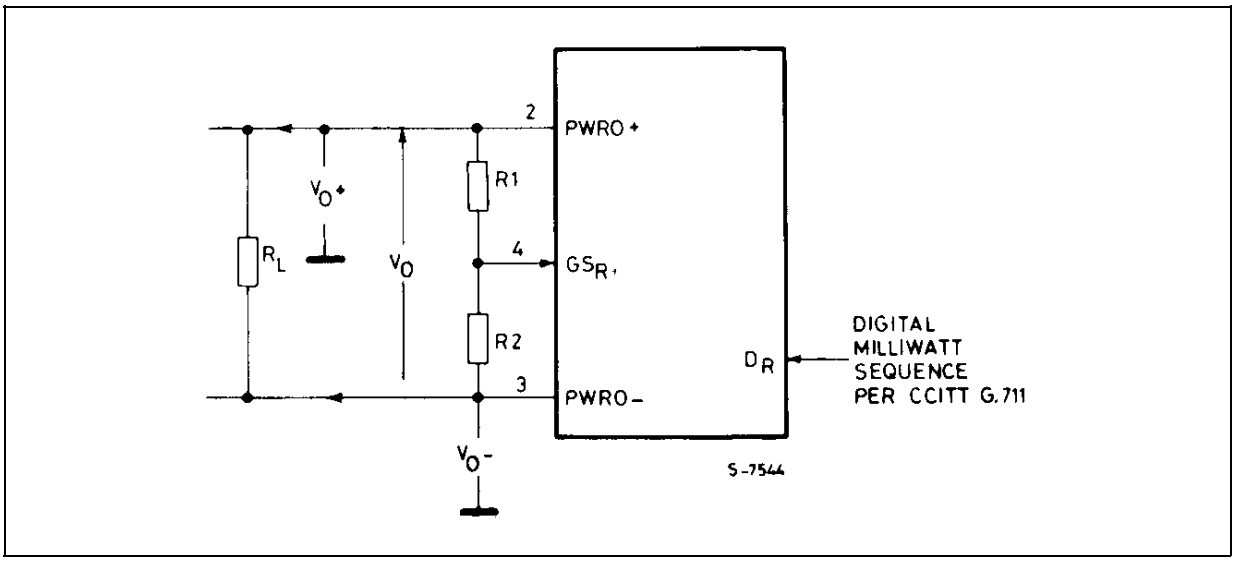
Receive Output Power Amplifiers

A balanced output amplifier is provided in order to allow maximum flexibility in output configuration. Either of the two outputs can be used single ended (referenced to GRDA) to drive single ended loads. Alternatively, the differential output will drive a bridged load directly. The output stage is capable of driving loads as low as 300 ohms single ended to a level of 12dBm or 600 ohms differentially to a level of 15dBm.

The receive channel transmission level may be adjusted between specified limits by manipulation of the GS_R input. GS_R is internally connected to an analog gain setting network. When GS_R is strapped to PWRO–, the receive level is minimized; when it is tied to PWRO+, the level is minimized. The output transmission level interpolates between 0 and -12dB as GSR is interpolated (with potentiometer) between PWRO- and PWRO+. The use of the output gain set is illustrated in figure 4.

Transmission levels are specified relative to the receive channel output under digital milliwatt conditions, that is, when the digital input at D_R is the eight-code sequence specified in CCITT recommendation G.711.

Figure 4: Gain Setting Configuration.



OUTPUT GAIN SET: DESIGN CONSIDERATIONS (refer to figure 4)

PWRO+ and PWRO– are low impedance complementary outputs. The voltages at the nodes are:

V_O at PWRO+

V_O at PWRO

$V_O = V_O+ V_O–$ (total differential response)

R1 and R2 are a gain setting resistor network with the center tap connected to the GS_R input. A value greater than 10KΩ and less than 100KΩ for R1 + R2 is recommended because:

a) The parallel combination of R1 + R2 and RL sets the total loading.

b) The total capacitance at the GS_R input and the parallel combination of R1 and R2 define a time constant which has to be minimized to avoid inaccuracies.

If VA represents the output voltage without any gain setting network connected, you can have:

$$V_O = AV_A$$

$$\text{where } A = \frac{1 + (R_1 / R_2)}{4 + (R_1 / R_2)}$$

For design purposes, a useful form is R1/R2 as a function of A.

$$R1 / R2 = \frac{4A - 1}{1 - A}$$

(allowable values for A are those which make R1/R2 positive)

Examples are:

If A = 1 (maximum output), then
R1/R2 = ∞ or $V(GS_R) = V_O$;
i.e., GS_R is tied to PWRO+

If A = 1/2. then
R1/R2 = 2

If A = 1/4 (minimum output) then
R1/R2 = 0 or $V(GS_R) = V_{O+}$;
i.e., GSR is tied to PWRO+

DC CHARACTERISTICS (T_{amb} = 0 to 70°C, V_{CC} = +5V ± 5%, V_{BB} = – 5V ± 5%, GRDA = 0V,unless otherwise specified) Typical values are for T_{amb} = 25°C and nominal power supply values.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DIGITAL INTERFACE						
I_{IL}	Low Level Input Current	GRDD ≤ V_{IN} ≤ V_{IL} (note 1)			10	µA
I_{IH}	High Level Input Current	V_{IH} ≤ V_{IN} ≤ V_{CC}			10	µA
V_{IL}	Input Low Voltage, Except CLKSEL				0.8	V
V_{IH}	Input High Voltage, Except CLKSEL		2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 3.2mA at D_X, $\overline{TS_X}$ and SIG_R			0.4	V
V_{OH}	Output High Voltage	I_{OH} = 9.6mA at D_X I_{OH} = 1.2mA at SIG_R	2.4			V
V_{ILO}	Input Low Voltage, CLKSEL (note 2)		V_{BB}		V_{BB} + 0.5	V
V_{IIO}	Input Intermediate Voltage, CLKSEL		GRDD -0.5		0.5	V
V_{IHO}	Input High Voltage, CLKSEL		V_{CC} - 0.5		VCC	V
C_{OX}	Digital Output Capacitance (note 3)			5		pF
C_{IN}	Digital Input Capacitance			5	10	pF

Notes:

1. V_{IN} is the voltage on any digital pin.

2. SIG_X and $DCLK_R$ are TTL level inputs between GRDD and V_{CC}; they are also pinstraps for mode selection when tied to V_{BB}. Under these conditions V_{ILO} is the input low voltage requirement.

3. Timing parameters are guaranteed based on a 100pF load capacitance. Up to eight digital outputs may be connected to a common PCM highway without buffering, assuming a board capacitance of 60pF.

DC CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max	Unit
POWER DISSIPATION All measurements made at f_{DCLK} = 2.048MHz, outputs unloaded						
I_{CC1}	V_{CC} Operating Current			6	10	mA
I_{BB1}	V_{BB} Operating Current			6	9	mA
I_{CC0}	V_{CC} Power Down Current	PDN ≤ V_{IL} ; after 10µs		40	300	µA
I_{BB0}	V_{BB} Power Down Current	PDN ≤ V_{IL} ; after 10µs		40	300	µA
I_{CCS}	V_{CC} Standby Current	FS_X, FS_R ≤ V_{IL} ; after 30ms		300	600	µA
I_{BBS}	V_{BB} Standby Current	FS_X, FS_R ≤ V_{IL} ; after 30ms		40	300	µA
P_{D1}	Operating Power Dissipation			60	100	mW
P_{D0}	Power Down Dissipation	PDN ≤ V_{IL} ; after 10µs		0.4	3	mW
P_{ST}	Standby Power Dissipation	FSX, FS_R ≤ V_{IL} ; after 30ms		1.7	5	mW
ANALOG INTERFACE, RECEIVE FILTER DRIVER AMPLIFIER STAGE						
I_{BX1}	Input Leakage Current, VF_XI+, VF_XI-	-2.17V ≤ V_{IN} ≤ 2.17V			100	nA
R_{IXI}	Input Resistance, VF_XI+, VF_XI-		10			MΩ
V_{OSXI}	Input Offset Voltage, VF_XI+, VF_XI-				25	mV
CMRR	Common Mode Rejection, VF_XI+, VF_XI-	-2.17V ≤ V_{IN} ≤ 2.17V	55			dB
A_{VOL}	DC Open Loop Voltage Gain, GS_X	R_L = 10K	5000	20.000		
f_C	Open Loop Unity Gain Bandwidth, GS_X			1		MHz
V_{OXI}	Output Voltage Swing GS_X	R_L ≥ 10kΩ	– 2.17		2.17	V
C_{LXI}	Load Capacitance, GS_X				50	pF
R_{LXI}	Minimum Load Resistance, GS_X		10			kΩ
ANALOG INTERFACE, RECEIVE FILTER DRIVER AMPLIFIER STAGE						
R_{ORA}	Output Resistance, PWRO+, PWRO-			1		Ω
V_{OSRA}	Single-ended Output DC Offset, PWRO+, PWRO-	Relative to GRDA	-150	75	150	mV
C_{LRA}	Load Capacitance, PWRO+, PWRO-				100	pF

AC CHARACTERISTICS - TRANSMISSION PARAMETERS

Unless otherwie noted, the analog input is a 0dBm0, 1020Hz sine wave[1]. Input amplifier is set for unity gain, noninverting. The digital inputs is a PCM bit stream generated by passing a 0dBm0, 1020Hz sine wave through an ideal encoder. Receive output is measured single ended, maximum gain configuration[2]. All output levels are (sin X)/X corrected.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
GAIN AND DYNAMIC RANGE						
EmW	Encoder Milliwatt Response (transmit gain tolerance)	T_{amb} = 25°C, V_{BB} = – 5V, V_{CC} = + 5V	-0.15	± 0.04	+0.15	dBm0
EmW_{TS}	EmW Variation with Temperature and Supplies	± 5% Supplies, 0 to 70°C Relative to Nominal Conditions	-0.12		+0.12	dB
DmW	Digital Milliwatt Response (receive gain tolerance)	T_{amb} = 25°C ; V_{BB} = – 5V, V_{CC} = + 5V	-0.15	± 0.04	+0.15	dBm0
DmW_{TS}	DmW Variation with Temperature and Supplies	± 5%, 0 to 70°C	-0.08		+0.08	dB
$0TLP_{1X}$	Zero Transmission Level Point Transmit Channel (0dBm0) µ-law	Referenced to 600Ω Referenced to 900Ω		+ 2.76 + 1.00		dBm dBm
$0TLP_{2X}$	Zero Transmission Level Point Transmit Channel (0dBm0) A-law	Referenced to 600Ω Referenced to 900Ω		+ 2.79 + 1.03		dBm dBm
$0TLP_{1R}$	Zero Receive Level Point Receive Channel (0dBm0) µ-law	Referenced to 600Ω Referenced to 900Ω		+ 5.76 + 4.00		dBm dBm
$0TLP_{2R}$	Zero Transmission Level Point Transmit Channel (0dBm0)) A-law	Referenced to 600Ω Referenced to 900Ω		+ 5.79 + 4.03		dBm dBm

AC CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
GAIN TRACKING Reference Level = – 10dBm0						
$GT1_X$	Transmit Gain Tracking Error Sinusoidal Input; μ-law	+ 3 to – 40dBm0 – 40 to – 50dBm0 – 50 to – 55dBm0			± 0.2 ± 0.4 ± 1.0	dB dB dB
$GT2_X$	Transmit Gain Tracking Error Sinusoidal Input; A-law	+ 3 to – 40dBm0 – 40 to – 50dBm0 – 50 to – 55dBm0			± 0.2 ± 0.4 ± 1.0	dB dB dB
$GT1_R$	Receive Gain Tracking Error Sinusoidal Input; μ-law	+ 3 to – 40dBm0 – 40 to – 50dBm0 – 50 to – 55dBm0			± 0.2 ± 0.4 ± 1.0	dB dB dB
$GT2_R$	Receive Gain Tracking Error Sinusoidal Input; A-law	+ 3 to – 40dBm0 – 40 to – 50dBm0 – 50 to – 55dBm0			± 0.2 ± 0.4 ± 1.0	dB dB dB
NOISE						
N_{XC1}	Transmit Noise, C-message Weighted	VF_XI+ = GRDA, VF_XI- = GS_X		0	13	dBrnc0
N_{XC2}	Transmit Noise, C-message Weighted with Eighth Bit Signaling	VF_XI+ = GRDA, VF_XI- = GS_X 6 th Frame Signaling		13	18	dBrnc0
N_{XP}	Transmit Noise, Psophometrically Weighted	VF_XI+ = GRDA, VF_XI- = GS_X		(note 3)	– 80	dBrnc0
N_{RC1}	Receive Noise, C-message Weighted: Quiet Code	D_R = 11111111 Measure at PWRO+		1	9	dBrnc0
N_{RC2}	Receive Noise, C-message Weighted: Sign Bit Toggle	Input to D_R is 0 code with Sign Bit Toggle at 1KHz Rate		1	10	dBm0p
N_{RP}	Receive Noise, Psophometrically Weighted	D_R = Lowest Positive Decode Level		-90	– 81	dB0p
N_{SF}	Single Frequency NOISE End to End Measurement	CCITT G.712.4.2			– 50	dBm0
$PSRR_1$	V_{CC} Power Supply Rejection, Transmit Channel	Idle Channel ; 200mV P-P Signal on Supply ; 0 to 50kHz, Measure at D_X		– 40		dB
$PSRR_2$	V_{BB} Power Supply Rejection, Transmit Channel	Idle Channel ; 200mV P-P Signal on Supply ; 0 to 50kHz, Measure at D_X		– 40		dB
$PSRR_3$	V_{CC} Power Supply Rejection, Receive Channel	Idle Channel ; 200mV P-P Signal on Supply ; Measure Narrow Band at PWRO+ Single Ended, 0 to 50kHz		– 40		dB
$PSRR_4$	V_{BB} Power Supply, Rejection Receive Channel	Idle Channel ; 200mV P-P Signal on Supply ; Measure Narrow Band at PWRO+ Single Ended, 0 to 50kHz		– 40		dB
CT_{TR}	Crosstalk, Transmit to Receive, Single Ended Outputs	VF_XI+ = 0dBm0, 1.02kHz, D_R = Lowest Positive Decode Level, Measure at PWRO+			– 80	dB
CT_{RT}	Crosstalk, Receive to Transmit, Single Ended Outputs	D_B = 0dBm0, 1.02kHz, VF_XI+ = GRDA, Measure at D_X			– 80	dB

Notes:

1. 0dBm0 is defined as the zero reference point of the channel under test (0TLP). This corresponds to an analog signal input of 1.064 V_{rms} or an output of 1.503 V_{rmst} (μLaw) dual 1.068 V_{rmst} or a output 1.516 V_{rmst} (A-Law)

2. Unity gain input amplifier : GS_X is connected to VF_XI, Signal input VF_XI+; Maximum gain output amplifier: GS_R is connected to PWRO, output to PWRO+.

3. Noise free: DX PCM Code stable at 01010101.

A.C. CHARACTERISTICS (continued)

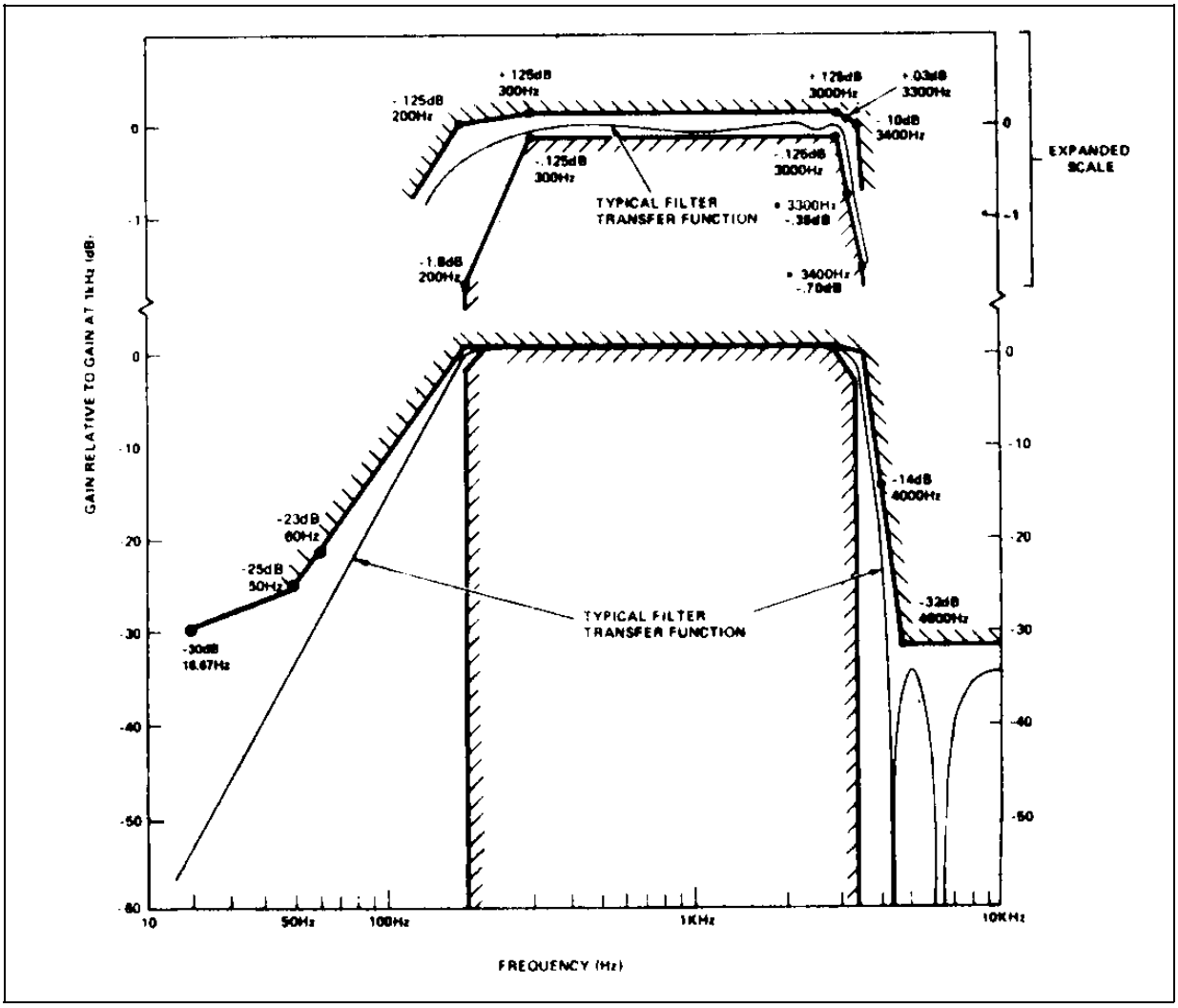
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DISTORTION						
$SD1_X$	Transmit Signal to Distortion, μ-law Sinusoidal Input; CCITT G.712-method 2	$0 \le VF_XI+ \le -30$dBm0 – 40dBm0 – 45dBm0	36 30 25			dB dB dB
$SD2_X$	Transmit Signal to Distortion, A-law Sinusoidal Input, CCITT G.712-method 2	$0 \le VF_XI+ \le -30$dBm0 – 40dBm0 – 45dBm0	36 30 25			dB dB dB
$SD1_R$	Transmit Signal to Distortion, μ-law Sinusoidal Input , CCITT G.712-method 2	$0 \le VF_XI+ \le -30$dBm0 – 40dBm0 – 45dBm0	36 30 25			dB dB dB
$SD2_R$	Receive Signal to Distortion, A-law Sinusoidal Input; CCITT G.712-method 2	$0 \le VF_XI+ \le -30$dBm0 – 40dBm0 – 45dBm0	36 30 25			dB dB dB
DP_{X1}	Transmit Single Frequency Distortion Products	AT & T Adivisory # 64 (3.8) 0dBm0 Input Signal			– 46	dB
DP_{R1}	Receive Single Frequency Distortion Products	AT & T Adivisory # 64 (3.8) 0dBm0 Input Signal			– 46	dB
IMD_1	Intermodulation Distortion, End to End Measurement	CCITT G.712 (7.1)			– 35	dB
IMD_2	Intermodulation Distortion, End to End Measurement	CCITT G.712 (7.2)			– 49	dB
SOS	Spurious Out of Band Signals, End to End Measurement	CCITT G.712 (6.1)			– 30	dBm0
SIS	Spurious in Band Signals, End to End Measurement	CCITT G.712 (9)			– 40	dBm0
D_{AX}	Transmit Absolute Delay	Fixed Data Rate CLK_X = 2.048MHz, 0dBm0, 1.02kHz Signal at VF_XI+ Measure at D_X		300		μs
D_{DX}	Transmit Differential Envelope Delay Relative to D_{AX}	f = 500 – 600Hz f = 600 – 1000Hz f = 1000 – 2600Hz f = 2600 – 2800Hz		170 95 45 80		μs μs μs μs
D_{AR}	Receive Absolute Delay	Fixed data rate, CLK_R = 2.048MHz; Digital input is DMW codes. Measure at PWRO+			190	μs
D_{DR}	Receive Differential Envelope Delay Relative to D_{AR}	f = 500 – 600Hz f = 600 – 1000Hz f = 1000 – 2600Hz f = 2600 – 2800Hz		10 10 85 110		μs μs μs μs

A.C. CHARACTERISTICS (continued)

TRANSMIT CHANNEL TRANSFER CHARACTERISTICS
(Input amplifier is set for unity gain, noninverting; maximum gain output.)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
G_{RX}	Gain Relative to Gain at 1.02 kHz	0 dBm0 Signal Input at VF_XI+				
	16.67Hz				– 30	dB
	50Hz				– 25	dB
	60Hz				– 23	dB
	200Hz		– 1.8		– 0.125	dB
	300 to 3000Hz		– 0.125		+ 0.125	dB
	3300Hz		– 0.35		+ 0.03	dB
	3400Hz		– 0.7		– 0.10	dB
	4000Hz				– 14	dB
	4600Hz and Above				– 32	dB

Figure 5: Transmit Filter

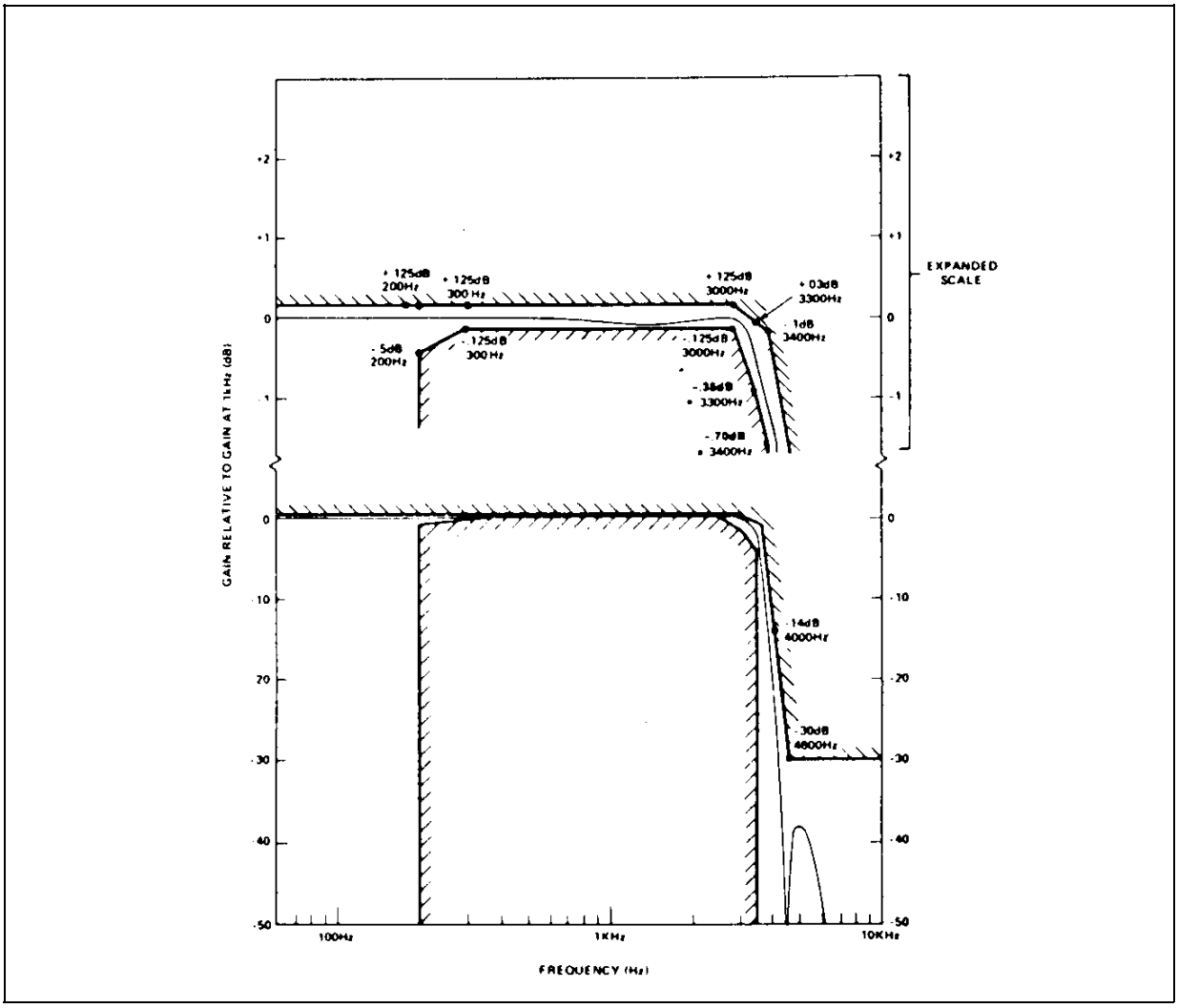


A.C. CHARACTERISTICS (continued)

RECEIVE CHANNEL TRANSFER CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
G_{RR}	Gain Relative to Gainat 1.02kHz	0dBm0 Signal Input at D_R				
	below 200Hz				+ 0.125	dB
	200Hz		– 0.5		+ 0.125	dB
	300 to 3000Hz		– 0.125		+ 0.125	dB
	3300Hz		– 0.35		+ 0.03	dB
	3400Hz		– 0.7		– 0.1	dB
	4000Hz				– 14	dB
	4600Hz and Above				– 30	dB

Figure 6: Receive Filter



AC CHARACTERISTICS - TIMING PARAMETERS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CLOCK SECTION						
t_{CY}	Clock Period, CLK_X, CLK_R	$f_{CLKX} = f_{CLKR} = 2.048MHz$	488			ns
t_{CLK}	Clock Pulse Width	CLK_X, CLK_R	195			ns
t_{DCLK}	Data Clock Pulse Width[1]	$64kHz \leq f_{DCLK} \leq 2.048MHz$	195			ns
t_{CDC}	Clock Duty Cycle	CLK_X, CLK_R	40	50	60	%
t_r, t_f	Clock Rise and Fall Time		5		30	ns
TRANSMIT SECTION, FIXED DATA RATE MODE[2]						
t_{DZX}	Data Enabled on TS Entry	$0 < C_{LOAD} < 100pF$	0		145	ns
t_{DDX}	Data Delay from CLK_X	$0 < C_{LOAD} < 100pF$	0		145	ns
t_{HZX}	Data Float on TS Exit	$C_{LOAD} = 0$	60		190	ns
t_{SON}	Timeslot X to Enable	$0 < C_{LOAD} < 100pF$	0		145	ns
t_{SOFF}	Timeslot X to Disable	$C_{LOAD} = 0$	50		190	ns
t_{FSD}	Frame Sync Delay		0		120	ns
t_{SS}	Signal Setup Time		0			ns
t_{SH}	Signal Setup Time		0			ns
RECEIVE SECTION, FIXED DATA RATE MODE						
t_{DSR}	Receive Data Setup		10			ns
t_{DHR}	Receive Data Hold		60			ns
t_{FSD}	Frame Sync Delay		0		120	ns
t_{SIGR}	SIG_R Update		0		2	µs
TRANSMIT SECTION, FIXED DATA RATE MODE[2]						
t_{TSDX}	Timeslot Delay from $DCLK_X$		-80		80	ns
t_{FSD}	Frame Sync Delay		0		120	ns
t_{DDX}	Data Delay from $DCLK_X$	0 < CLOAD < 100pF	0		100	ns
t_{DON}	Timeslot to D_X Active	$0 < C_{LOAD} < 100pF$	0		50	ns
t_{DOFF}	Timeslot to D_X Inactive	$0 < C_{LOAD} < 100pF$	0		80	ns
f_{DX}	Data Clock Frequency		64		2048[1]	KHz
t_{DFSX}	Data Delay from FS_X	$t_{TSDX} = 80ns$	0		140	ns
RECEIVE SECTION, FIXED DATA RATE MODE						
t_{TSDR}	Timeslot Delay from $DCLK_R$		-80		80	ns
t_{FSD}	Frame Sync Delay		0		120	ns
t_{DSR}	Receive Data Setup Time		10			ns
t_{DHR}	Receive Data Hold Time		60			ns
t_{DR}	Data Clock Frequency		64		2048[1]	kHz
t_{SER}	Timeslot End Receive Time		0			ns
64KB OPERATION, VARIABLE DATA RATE MODE						
t_{FSLX}	Transmit Frame Sync Minimum Downtime	FS_X is TTL high for remainder of frame	488			ns
t_{FSLR}	Receive Frame Sync Miniumum Downtime	FS_R is TTL high for remainder of frame	1952			ns
t_{DCLK}	Data Clock Pulse Width		10			µs

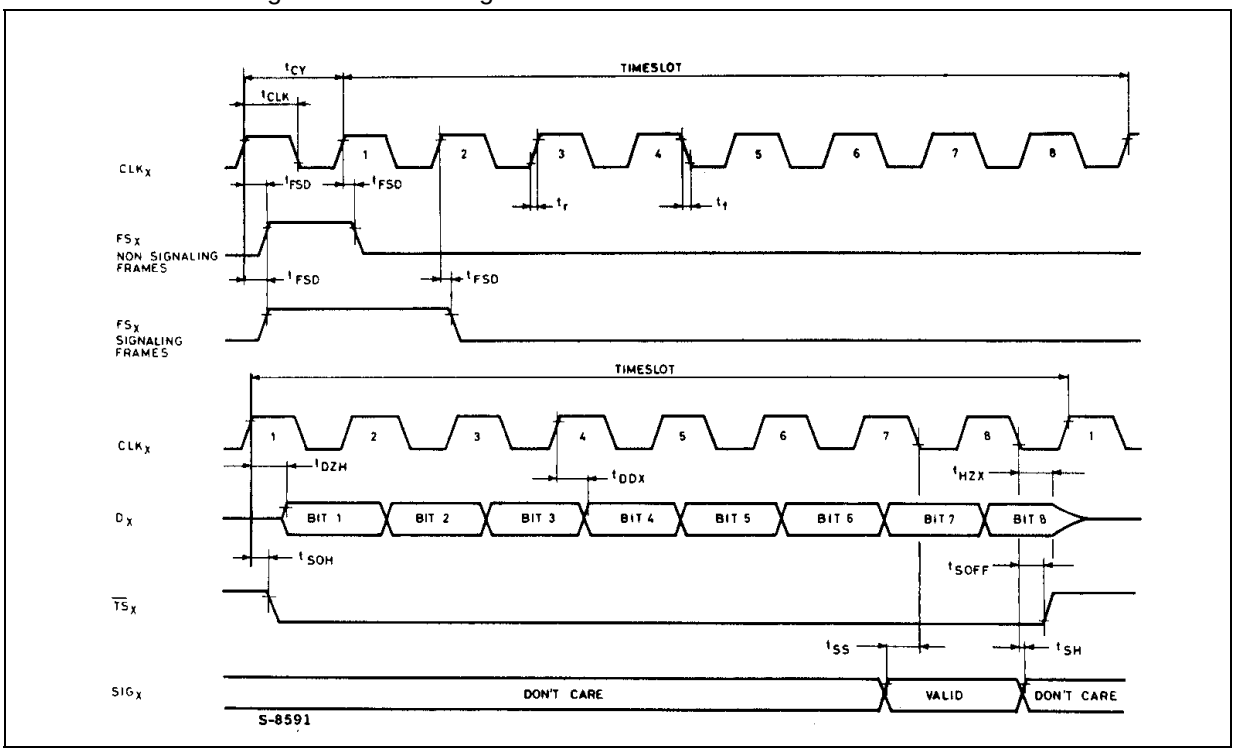
Notes:

1. Devices are available wich operate at data rates up to 4.096MHz; the minimum data clock pulse width for these devices is 110ns

2. Timing parameters t_{DZX}, t_{HZX}, and t_{SOFF} are referenced to a high impedance state.

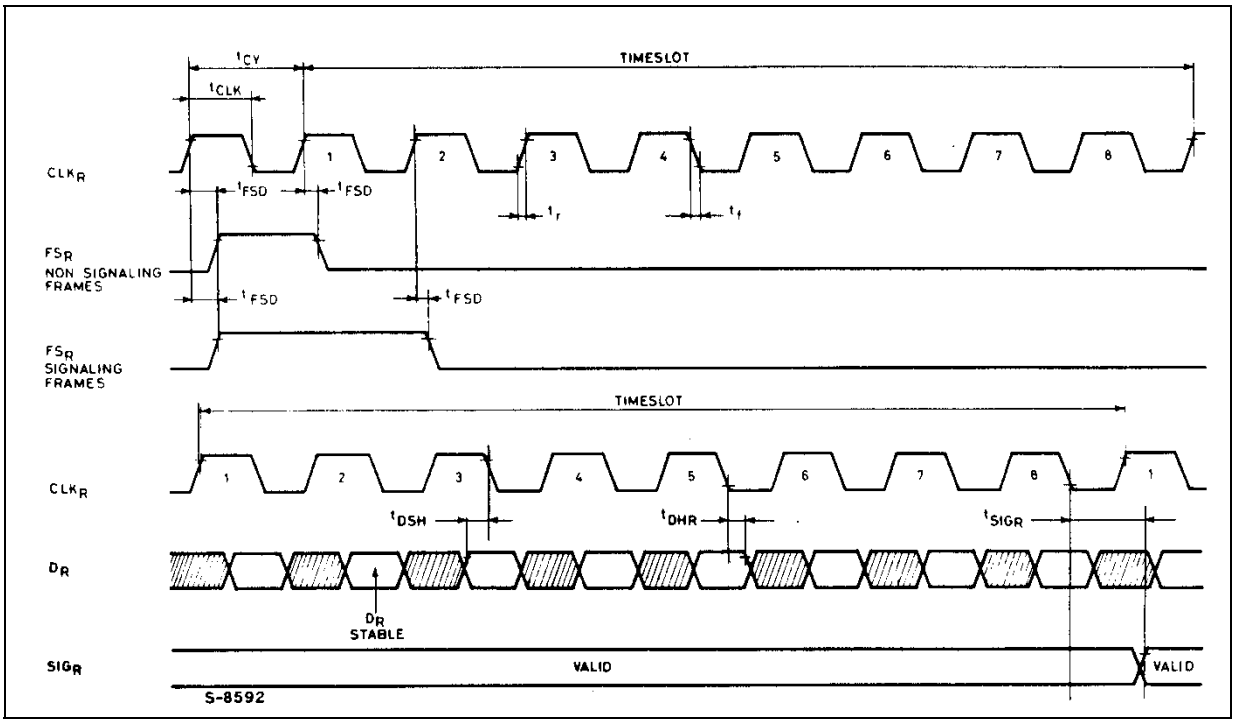
WAVEFORMS:

Fixed Data Rate Timing - Transmit Timing



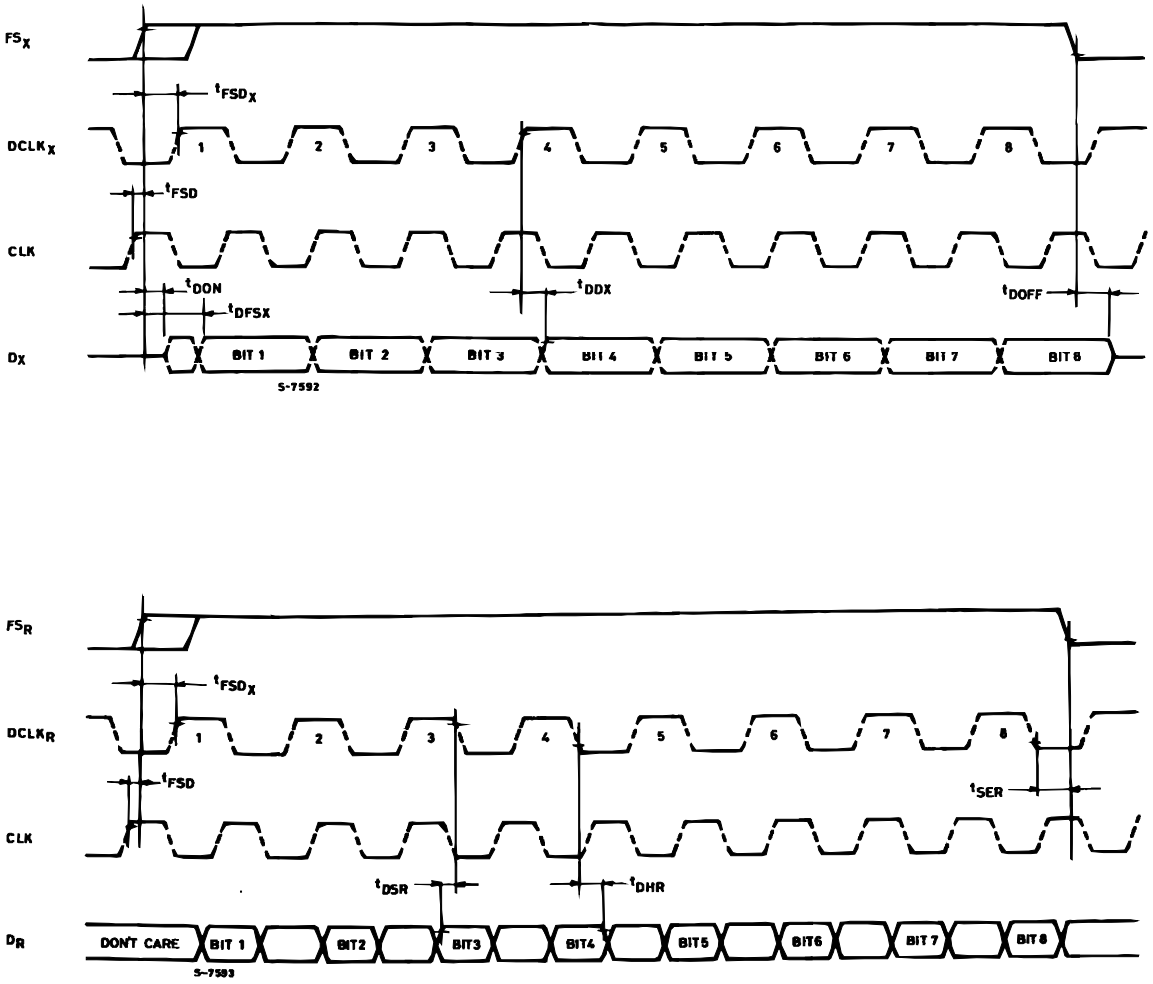
NOTE: All timing parameters referenced to V_{IH} and V_{IL} except t_{DZX}, t_{SOFF} and t_{HZX} which reference a high impedance state.

Receive Timing

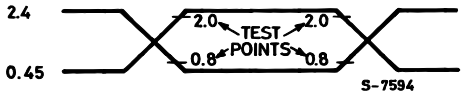


NOTE: All timing parameters referenced to V_{IH} and V_{IL}

VARIABLE DATA RATE TIMING



AC Timing Input, Output Waveform



DIP20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053