

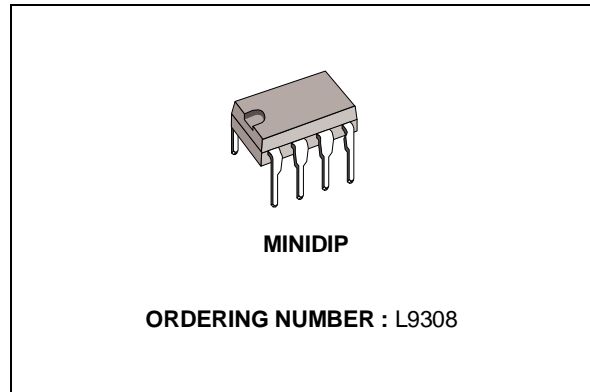
DUAL LOW SIDE DRIVER

- DARLINGTON OUTPUT STAGE
- INPUT COMPARATOR WITH WIDE RANGE COMMON MODE OPERATION AND GROUND COMPATIBLE INPUTS
- INPUT COMPARATOR HYSTERESIS
- SHORT CIRCUIT PROTECTION OF OUTPUT WITH SOA PROTECTION
- INTERNAL THERMAL PROTECTION WITH HYSTERESIS
- SINGLE SUPPLY VOLTAGE FROM 3.5V UP TO 28V

DESCRIPTION

The L9308 is a monolithic interface circuit with differential input comparator and open collector output able to sink current specifically to drive lamps, relays, d.c. motors, electro valves etc.

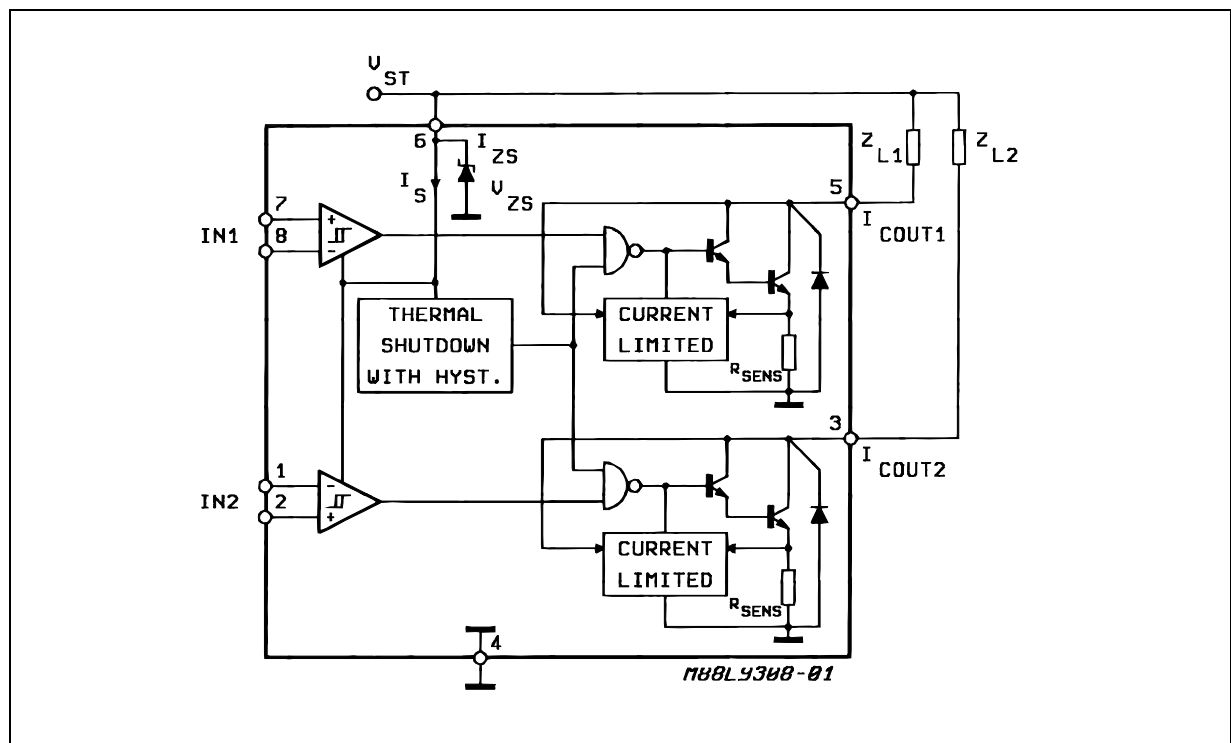
Particular care has been taken to protect the device against destructive failures - short circuit of outputs to V_S , SOA protection, supply overvoltage.



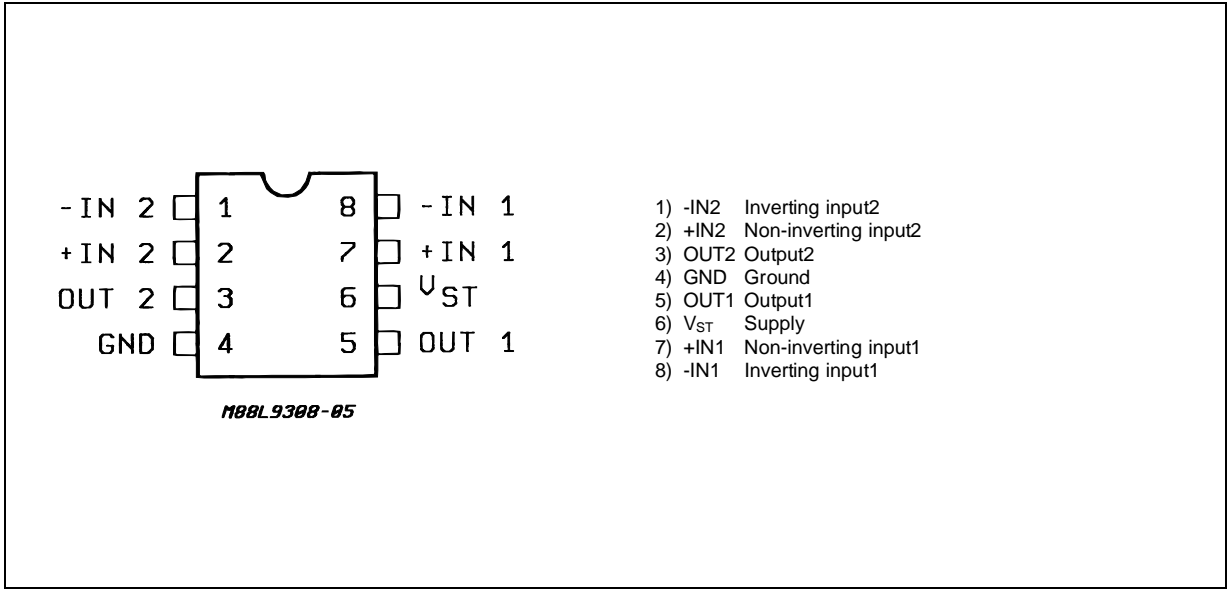
A built in thermal shut-down switches off the device when the IC's internal dissipation becomes too high and the chip temperature exceeds the security threshold.

The input comparator hysteresis increases the interface's noise immunity allowing the correct use in critical environments as automotive applications.

BLOCK DIAGRAM



PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
I _{zs}	Current Into Supply	30	mA
	Clamp Zener Diode	80	mA
V _s	Supply Voltage	28	V(**)
I _o	Output Current	Internally Limited	
T _j , T _{stg}	Junction and Storage Temperature	– 55 to +150	°C
P _{tot}	Power Dissipation at T _{amb} = 85°C	650	mW

(*) TON ≤ 2.5ms ; repetition time > 30ms.

(**) The maximum allowed supply voltage without limiting resistor is limited by the built-in protection zener diode : see V_{zs} spec. values. If V_s is higher than V_{zs} a resistor R_s is necessary to limit the zener current I_{zs}.

THERMAL DATA

Symbol	Parameter	Value	Unit
R _{th j-amb}	Thermal Resistance Junction-ambient	Max 100	°C/W

ELECTRICAL CHARACTERISTICS ($V_S = 14.4V$; $-40^{\circ}C \leq T_{amb}, \leq 85^{\circ}C$; $R_S = 100\Omega$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Hysteresis of the Input Comparater	$V_{IN} = 200mV_{pp}$; $f = 1kHz$	20		80	mV
I_B	Input Bias Current	$V_I^+ = V_I^- = 0$		0.2	1.0	μA
I_{OS}	Input Offset Current	$V_I^+ = V_I^- = 0$		± 50	± 400	nA
CMR	Input Common Mode Range	$V_S = 6 - 18V$ $T_{amb} = 25^{\circ}C$	0		$V_{ST} - 1.6$	V
I_{SC}	Output Short Circuit Current for Each Channel (see fig. 4)	$V_{IN} - V_{IN} > 70mV$ $V_S = 16V$ $T_{amb} = 25^{\circ}C$ to $85^{\circ}C$ $T_{amb} = -40^{\circ}C$ to $25^{\circ}C$ $V_{OUT\ 1, 2} = 6V$			0.6 0.7 1.2	A A A
V_{CSAT}	On Status Saturation Voltage	$T_{amb} = -40^{\circ}C$ to $25^{\circ}C$ $V_I^- - V_I^+ > 70mV$ $I_{OUT\ 1, 2} = 300mA$ $T_{amb} = 25^{\circ}C$ to $85^{\circ}C$		1.0	1.5 1.4	V V
I_{OL}	Output Leakage Current	$V_I^- - V_I^+ > 70mV$ $V_S = 18V$ $V_S = 5V$		10	300 20	μA μA
V_{ST}	Supply voltage (pin 6)		3.5		18	V
$I_{"st.by"}$	Supply Current	$V_I^+ - V_I^- > 70mV$		5	8	mA
I_{ON^+}	Supply Current	$V_I^- - V_I^+ > 70mV$		18		mA
V_{ZS}	Voltage Clamp Supply Protection	$I_{ZS} = 10mA$	20		27	V
I_{Omin}	Minimum Output Current wiyth the Outputs connected Together	$V_{CSAT} = 1.5V$	400			mA
t_r t_f	Rise Time (see fig. 2) Fall Time	$I_{OUT} = 50mA$ $T_{amb} = 25^{\circ}C$			2 2	μs
t_{don} t_{doff}	Delay Time on Delay Time off	$I_{OUT} = 50mA$ $T_{amb} = 25^{\circ}C$			10 10	μs

Figure 1 : Switching Time Test Circuit.

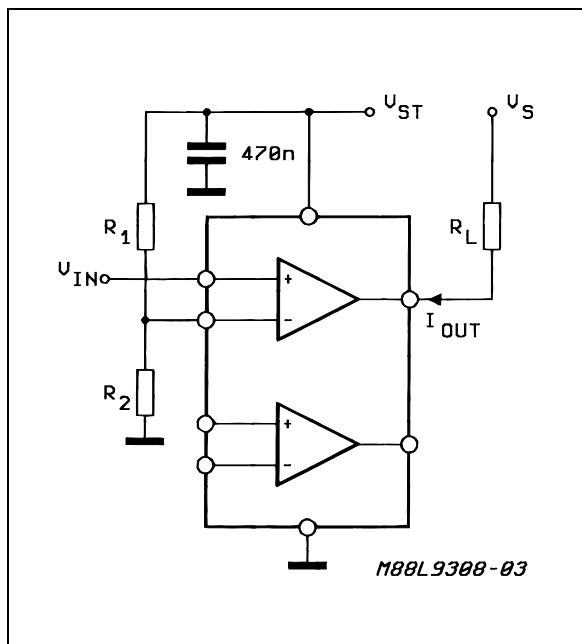


Figure 2 : Switching Time Waveforms for Resistive Loads.

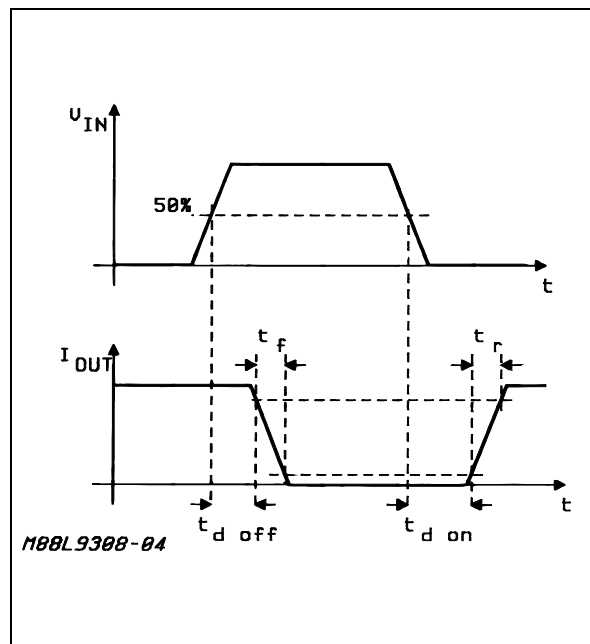
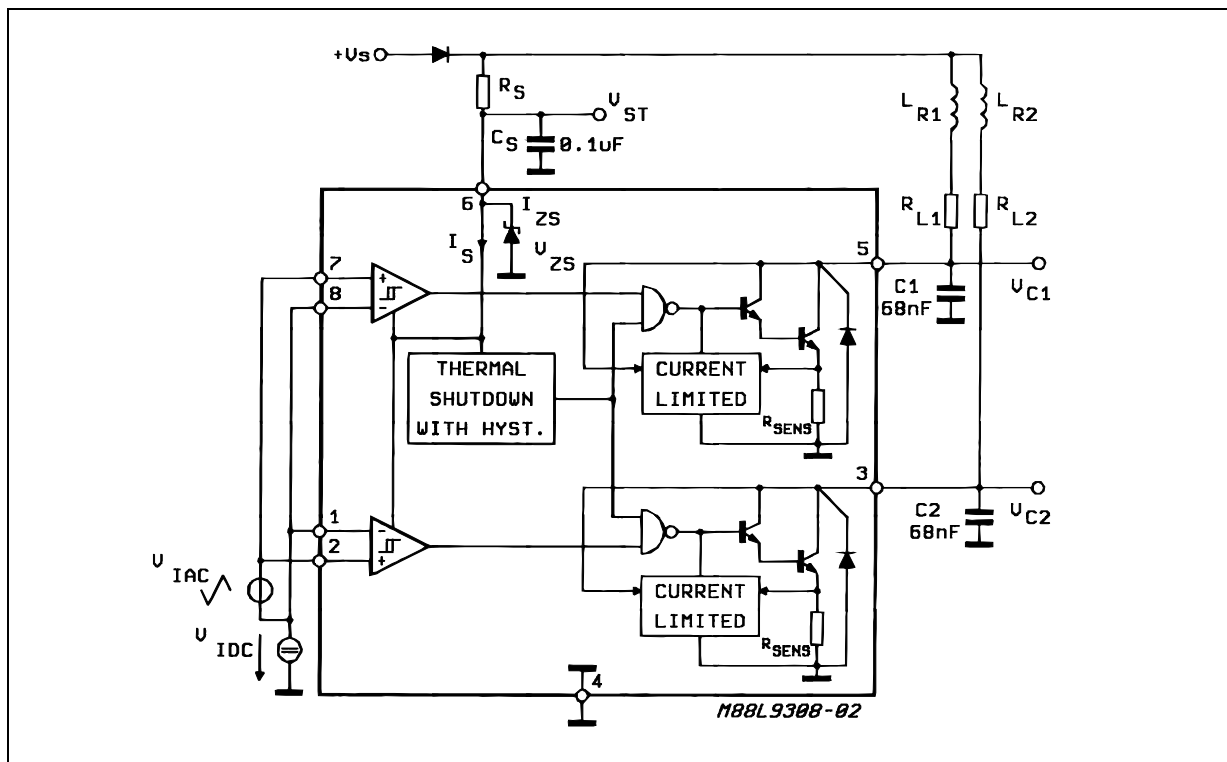
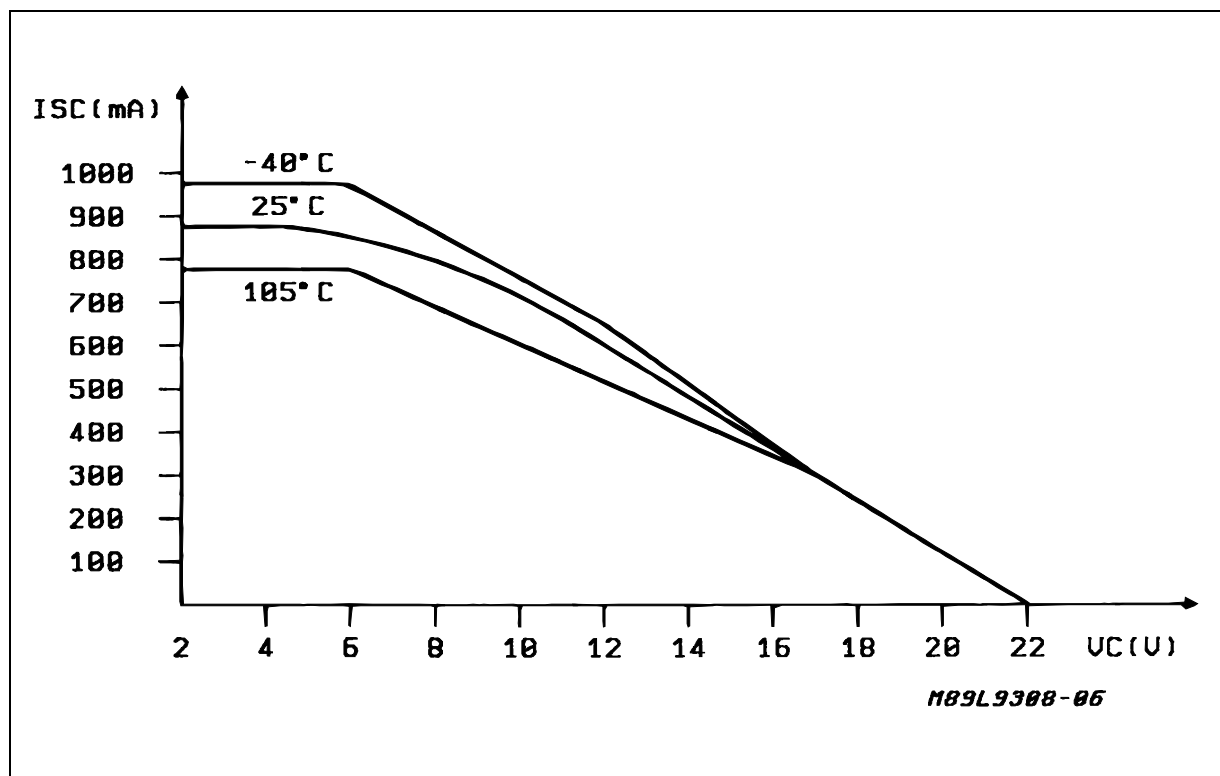


Figure 3 : Typical Application and Test Circuit.

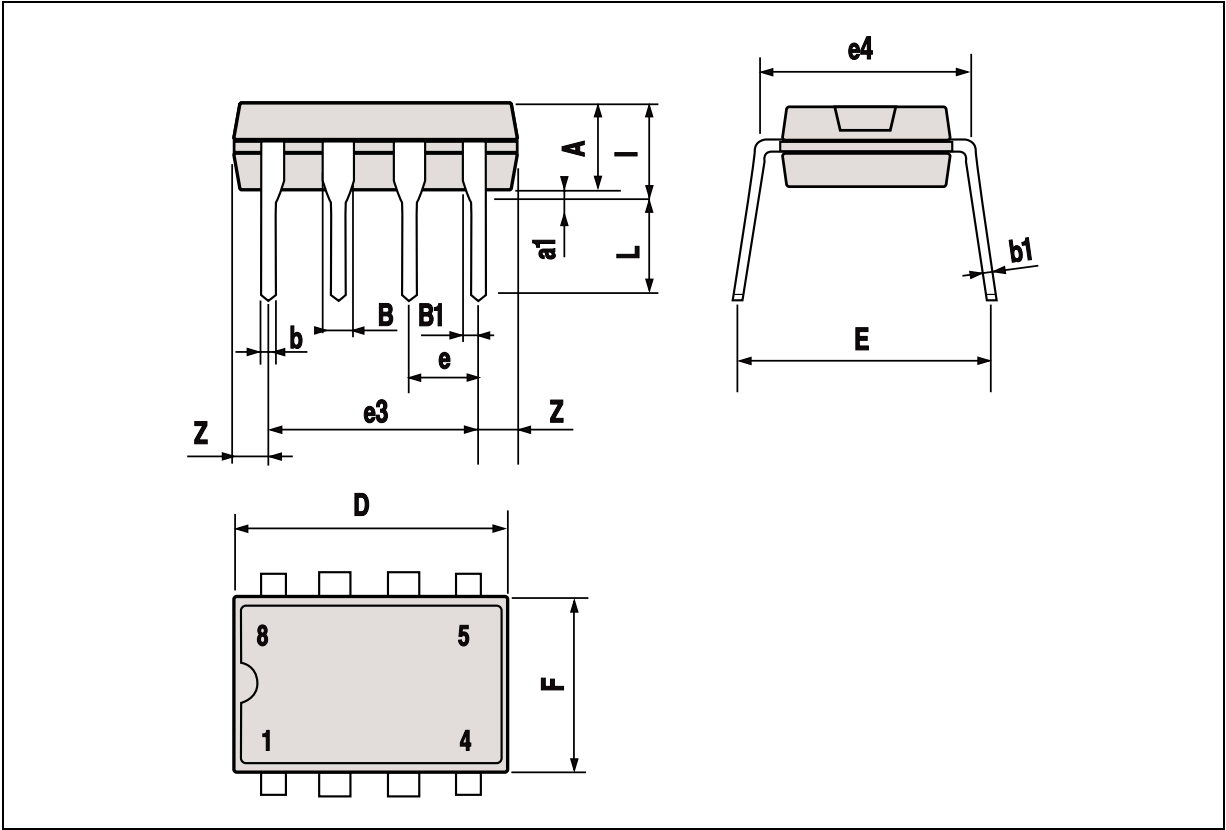


Notes : a) R_S required only to limit I_{ZS} whenever V_S exceeds V_{ZS} voltage value.
b) C_1 , C_2 cut high frequency gain during current limiting.

Figure 4 : Typical SOA Characteristic.

MINIDIP PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060



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