MCP3021

Low Power 10-Bit A/D Converter With I²C™ Interface

Features

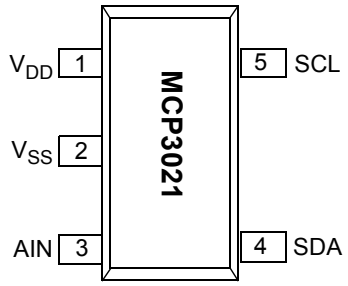
- 10-bit resolution
- ±1 LSB DNL, ±1 LSB INL max.
- 250 µA max conversion current
- 5 nA typical standby current, 1 µA max.
- I²C™ compatible serial interface
  - 100 kHz I²C Standard mode
  - 400 kHz I²C Fast mode
- Up to 8 devices on single 2-wire bus
- 22.3 ksps in I²C Fast mode
- Single-ended analog input channel
- On-chip sample and hold
- On-chip conversion clock
- Single supply specified operation: 2.7V to 5.5V
- Temperature range:
  - Extended: -40°C to +125°C
- Small SOT-23 package

Applications

- Data Logging
- Multi-zone Monitoring
- Hand Held Portable Applications
- Battery Powered Test Equipment
- Remote or Isolated Data Acquisition

Package Type

5-Pin SOT-23A



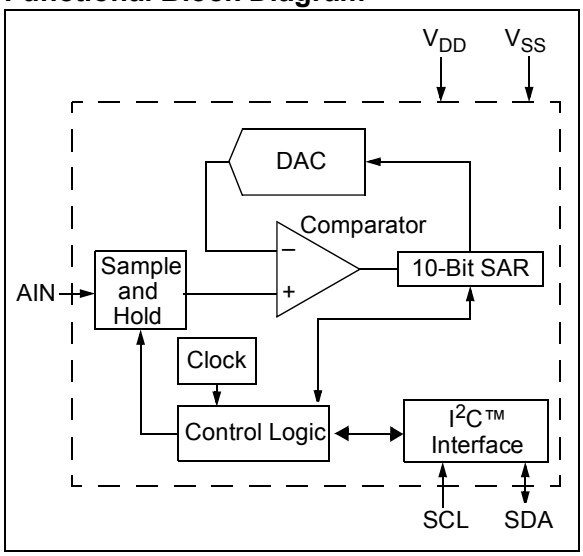
Description

The Microchip Technology Inc. MCP3021 is a successive approximation A/D converter (ADC) with 10-bit resolution. Available in the SOT-23 package, this device provides one single-ended input with very low power consumption. Based on an advanced CMOS technology, the MCP3021 provides a low maximum conversion current and standby current of 250 µA and 1 µA, respectively. Low current consumption, combined with the small SOT-23 package, make this device ideal for battery-powered and remote data acquisition applications.

Communication to the MCP3021 is performed using a 2-wire I²C compatible interface. Standard (100 kHz) and Fast (400 kHz) I²C modes are available with the device. An on-chip conversion clock enables independent timing for the I²C and conversion clocks. The device is also addressable, allowing up to eight devices on a single 2-wire bus.

The MCP3021 runs on a single supply voltage that operates over a broad range of 2.7V to 5.5V. This device also provides excellent linearity of ±1 LSB differential non-linearity (DNL) and ±1 LSB integral non-linearity (INL), maximum.

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{DD}.....7.0V

Analog input pin w.r.t. V_{SS}..... ..... -0.6V to V_{DD} +0.6V

SDA and SCL pins w.r.t. V_{SS}..... .....-0.6V to V_{DD} +1.0V

Storage temperature .....-65°C to +150°C

Ambient temp. with power applied .....-65°C to +125°C

Maximum Junction Temperature .....150°C

ESD protection on all pins (HBM) .....≥ 4 kV

† Stresses above those listed under “Maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
V_{DD}	+2.7V to 5.5V Power Supply
V_{SS}	Ground
AIN	Analog Input
SDA	Serial Data In/Out
SCL	Serial Clock In

DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise noted, all parameters apply at V_{DD} = 5.0V, V_{SS} = GND, R_{PU} = 2 kΩ T_A = -40°C to +85°C, I^2C Fast Mode Timing: f_{SCL} = 400 kHz (**Note 3**).

Parameters	Sym	Min	Typ	Max	Units	Conditions
DC Accuracy						
Resolution			10		bits	
Integral Nonlinearity	INL	—	±0.25	±1	LSB	
Differential Nonlinearity	DNL	—	±0.25	±1	LSB	No missing codes
Offset Error		—	±0.75	±3	LSB	
Gain Error		—	-1	±3	LSB	
Dynamic Performance						
Total Harmonic Distortion	THD	—	-70	—	dB	V_{IN} = 0.1V to 4.9V @ 1 kHz
Signal to Noise and Distortion	SINAD	—	60	—	dB	V_{IN} = 0.1V to 4.9V @ 1 kHz
Spurious Free Dynamic Range	SFDR	—	74	—	dB	V_{IN} = 0.1V to 4.9V @ 1 kHz
Analog Input						
Input Voltage Range		V_{SS}-0.3	—	V_{DD}+0.3	V	2.7V ≤ V_{DD} ≤ 5.5V
Leakage Current		-1	—	+1	µA	
SDA/SCL (open-drain output)						
Data Coding Format			Straight Binary			
High-level input voltage	V_{IH}	0.7 V_{DD}	—	—	V	
Low-level input voltage	V_{IL}	—	—	0.3 V_{DD}	V	
Low-level output voltage	V_{OL}	—	—	0.4	V	I_{OL} = 3 mA, R_{PU} = 1.53 kΩ
Hysteresis of Schmitt trigger inputs	V_{HYST}	—	0.05V_{DD}	—	V	f_{SCL} = 400 kHz only

Note 1: Sample time is the time between conversions after the address byte has been sent to the converter. Refer to Figure 5-6.

2: This parameter is periodically sampled and not 100% tested.

3: R_{PU} = Pull-up resistor on SDA and SCL.

4: SDA and SCL = V_{SS} to V_{DD} at 400 kHz.

5: t_{ACQ} and t_{CONV} are dependent on internal oscillator timing. See Figure 5-5 and Figure 5-6 for relation to SCL.

DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Unless otherwise noted, all parameters apply at V_{DD} = 5.0V, V_{SS} = GND, R_{PU} = 2 kΩ T_A = -40°C to +85°C, I^2C Fast Mode Timing: f_{SCL} = 400 kHz (**Note 3**).

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input leakage current	I_{LI}	-1	—	+1	µA	$V_{IN} = V_{SS}$ to V_{DD}
Output leakage current	I_{LO}	-1	—	+1	µA	$V_{OUT} = V_{SS}$ to V_{DD}
Pin capacitance (all inputs/outputs)	C_{IN}, C_{OUT}	—	—	10	pF	T_{AMB} = 25°C, f = 1 MHz; (**Note 2**)
Bus Capacitance	C_B	—	—	400	pF	SDA drive low, 0.4V
Power Requirements						
Operating Voltage	V_{DD}	2.7	—	5.5	V	
Conversion Current	I_{DD}	—	175	250	µA	
Standby Current	I_{DDS}	—	0.005	1	µA	SDA, SCL = V_{DD}
Active bus current	I_{DDA}	—	—	120	µA	**Note 4**
Conversion Rate						
Conversion Time	t_{CONV}	—	8.96	—	µs	**Note 5**
Analog Input Acquisition Time	t_{ACQ}	—	1.12	—	µs	**Note 5**
Sample Rate	f_{SAMP}	—	—	22.3	ksps	f_{SCL} = 400 kHz (**Note 1**)

Note 1: Sample time is the time between conversions after the address byte has been sent to the converter. Refer to Figure 5-6.

2: This parameter is periodically sampled and not 100% tested.

3: R_{PU} = Pull-up resistor on SDA and SCL.

4: SDA and SCL = V_{SS} to V_{DD} at 400 kHz.

5: t_{ACQ} and t_{CONV} are dependent on internal oscillator timing. See Figure 5-5 and Figure 5-6 for relation to SCL.

TEMPERATURE SPECIFICATIONS

Electrical Characteristics: All parameters apply across the operating voltage range.

Parameters	Symbol	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Extended Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SOT23A	θ_{JA}	—	256	—	°C/W	

TIMING SPECIFICATIONS

Electrical Characteristics: All parameters apply at V_{DD} = 2.7V - 5.5V, V_{SS} = GND, T_A = -40°C to +85°C.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
I^2C Standard Mode						
Clock frequency	f_{SCL}	0	—	100	kHz	
Clock high time	T_{HIGH}	4000	—	—	ns	
Clock low time	T_{LOW}	4700	—	—	ns	
SDA and SCL rise time	T_R	—	—	1000	ns	From V_{IL} to V_{IH} (**Note 1**)
SDA and SCL fall time	T_F	—	—	300	ns	From V_{IL} to V_{IH} (**Note 1**)
START condition hold time	$T_{HD:STA}$	4000	—	—	ns	
START condition setup time	$T_{SU:STA}$	4700	—	—	ns	
Data input setup time	$T_{SU:DAT}$	250	—	—	ns	
STOP condition setup time	$T_{SU:STO}$	4000	—	—	ns	
STOP condition hold time	$T_{HD:STD}$	4000	—	—	ns	
Output valid from clock	T_{AA}	—	—	3500	ns	
Bus free time	T_{BUF}	4700	—	—	ns	**Note 2**
Input filter spike suppression	T_{SP}	—	—	50	ns	SDA and SCL pins **(Note 1)**
I^2C Fast Mode						
Clock frequency	F_{SCL}	0	—	400	kHz	
Clock high time	T_{HIGH}	600	—	—	ns	
Clock low time	T_{LOW}	1300	—	—	ns	
SDA and SCL rise time	T_R	20 + 0.1C_B	—	300	ns	From V_{IL} to V_{IH} **(Note 1)**
SDA and SCL fall time	T_F	20 + 0.1C_B	—	300	ns	From V_{IL} to V_{IH} **(Note 1)**
START condition hold time	$T_{HD:STA}$	600	—	—	ns	
START condition setup time	$T_{SU:STA}$	600	—	—	ns	
Data input hold time	$T_{HD:DAT}$	0	—	0.9	ms	
Data input setup time	$T_{SU:DAT}$	100	—	—	ns	
STOP condition setup time	$T_{SU:STO}$	600	—	—	ns	
STOP condition hold time	$T_{HD:STD}$	600	—	—	ns	
Output valid from clock	T_{AA}	—	—	900	ns	
Bus free time	T_{BUF}	1300	—	—	ns	**Note 2**
Input filter spike suppression	T_{SP}	—	—	50	ns	SDA and SCL pins **(Note 1)**

Note 1: This parameter is periodically sampled and not 100% tested.

2: Time the bus must be free before a new transmission can start.

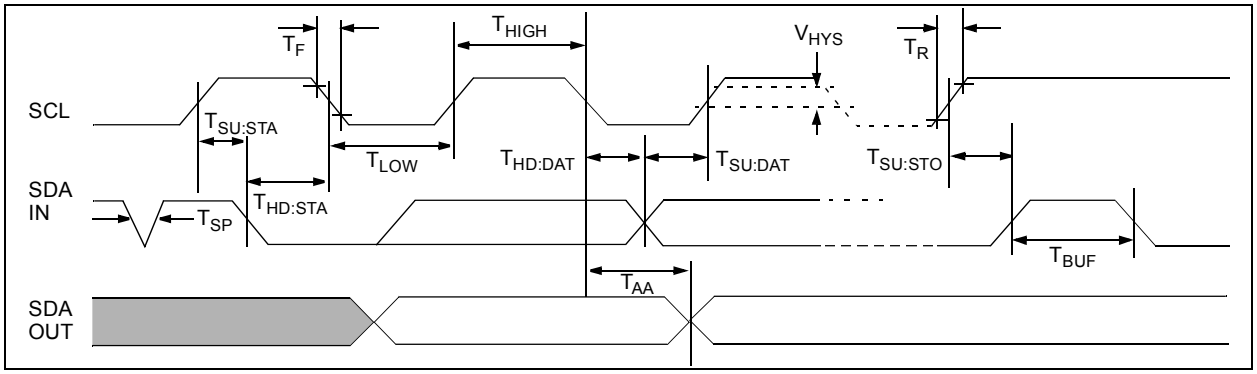


FIGURE 1-1: *Standard and Fast Mode Bus Timing Data.*

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, V_{DD} = 5V, V_{SS} = 0V, I^2C Fast Mode Timing (SCL = 400 kHz), Continuous Conversion Mode (f_{SAMP} = 22.3 ksps), T_A = +25°C.

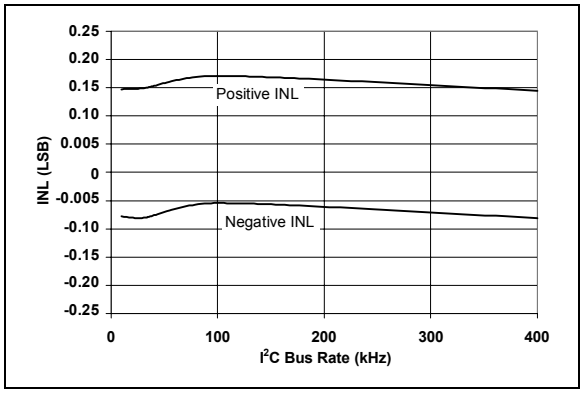


FIGURE 2-1: *INL vs. Clock Rate.*

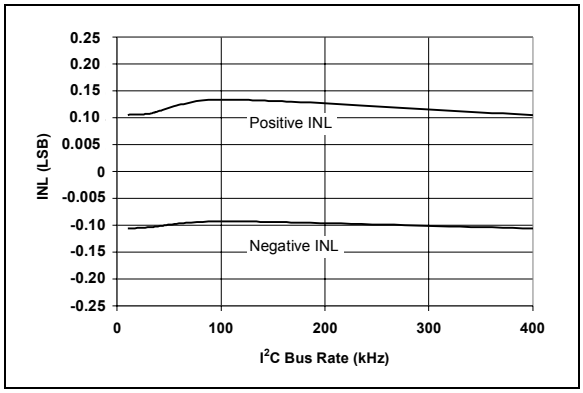


FIGURE 2-4: *INL vs. Clock Rate (V_{DD} = 2.7V).*

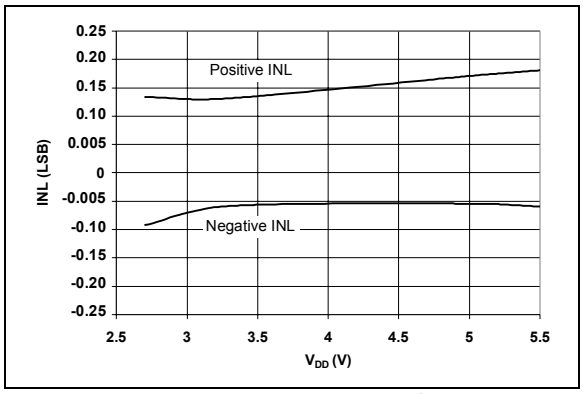


FIGURE 2-2: *INL vs. V_{DD} - I^2C Standard Mode (f_{SCL} = 100 kHz).*

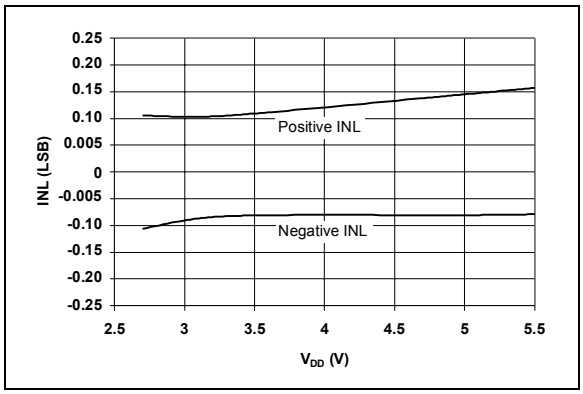


FIGURE 2-5: *INL vs. V_{DD} - I^2C Fast Mode (f_{SCL} = 400 kHz).*

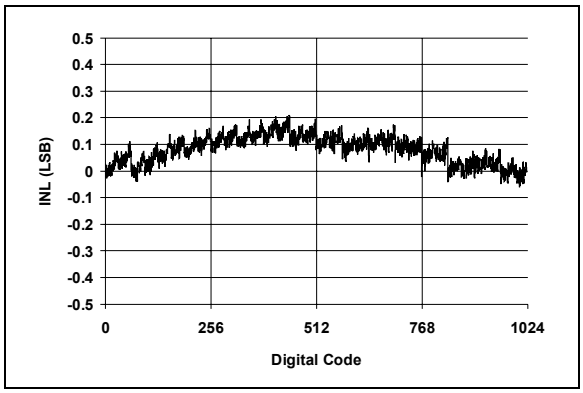


FIGURE 2-3: *INL vs. Code (Representative Part).*

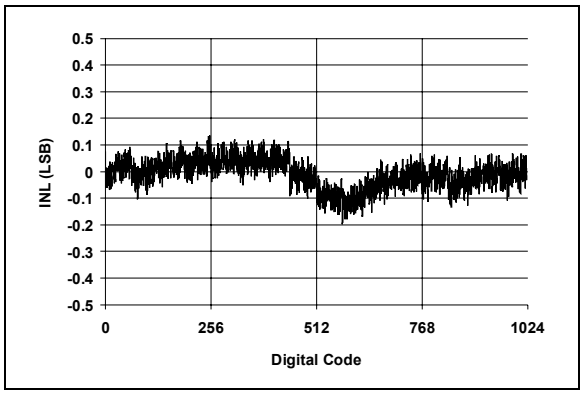


FIGURE 2-6: *INL vs. Code (Representative Part, V_{DD} = 2.7V).*

Note: Unless otherwise indicated, V_{DD} = 5V, V_{SS} = 0V, I^2C Fast Mode Timing (SCL = 400 kHz), Continuous Conversion Mode (f_{SAMP} = 22.3 ksps), T_A = +25°C.

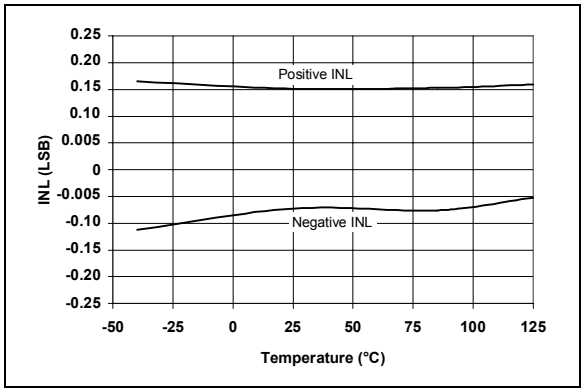


FIGURE 2-7: *INL vs. Temperature.*

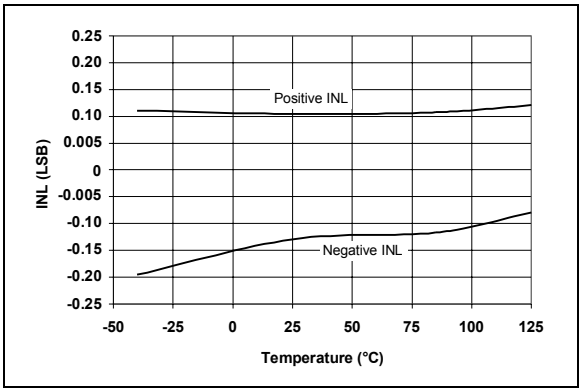


FIGURE 2-10: *INL vs. Temperature (V_{DD} = 2.7V).*

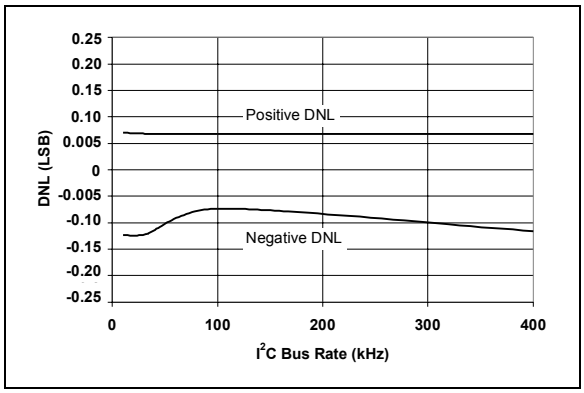


FIGURE 2-8: *DNL vs. Clock Rate.*

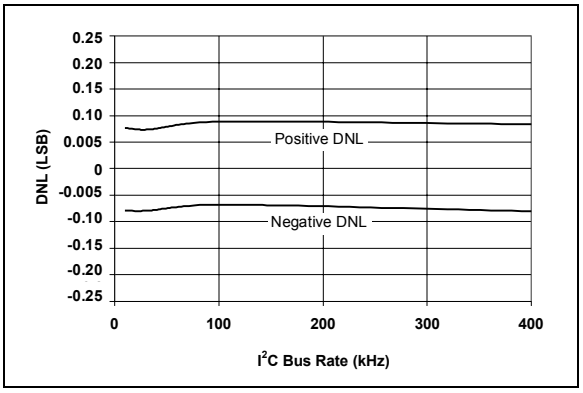


FIGURE 2-11: *DNL vs. Clock Rate (V_{DD} = 2.7V).*

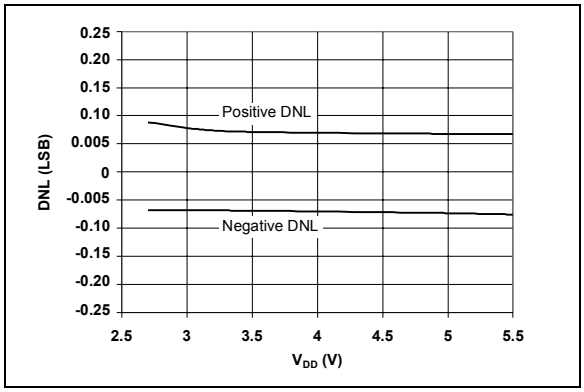


FIGURE 2-9: *DNL vs. V_{DD} - I^2C Standard Mode (f_{SCL} = 100 kHz).*

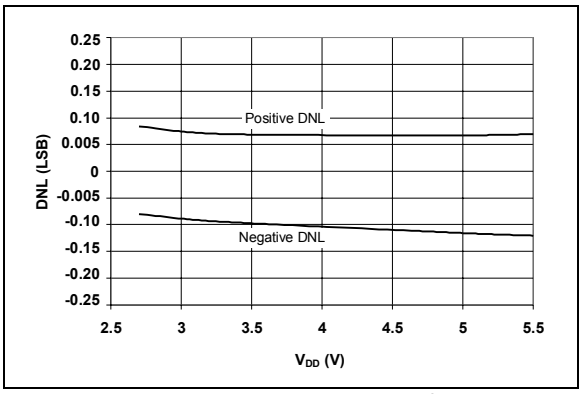


FIGURE 2-12: *DNL vs. V_{DD} - I^2C Fast Mode (f_{SCL} = 400 kHz).*

Note: Unless otherwise indicated, V_{DD} = 5V, V_{SS} = 0V, I^2C Fast Mode Timing (SCL = 400 kHz), Continuous Conversion Mode (f_{SAMP} = 22.3 ksps), T_A = +25°C.

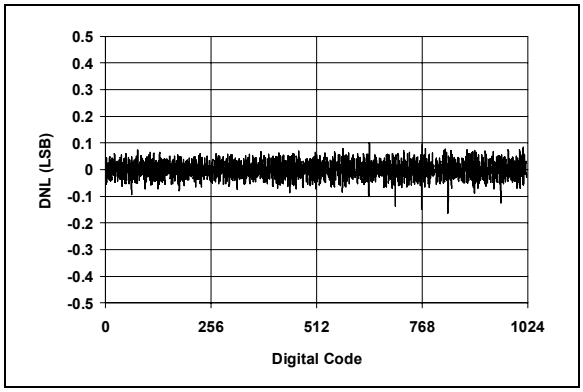


FIGURE 2-13: *DNL vs. Code (Representative Part).*

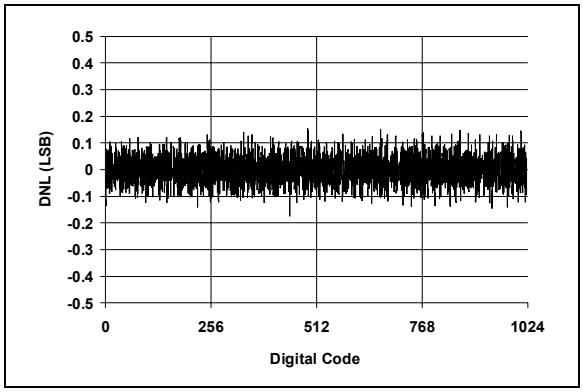


FIGURE 2-16: *DNL vs. Code (Representative Part, V_{DD} = 2.7V).*

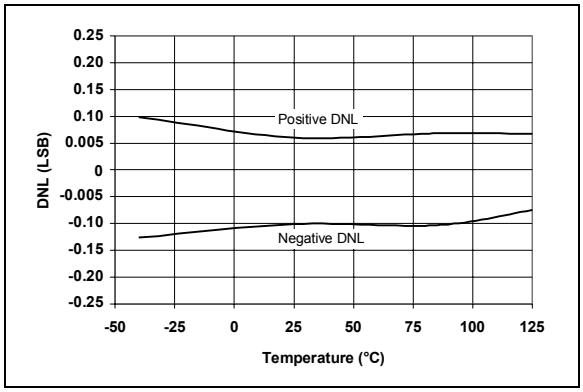


FIGURE 2-14: *DNL vs. Temperature.*

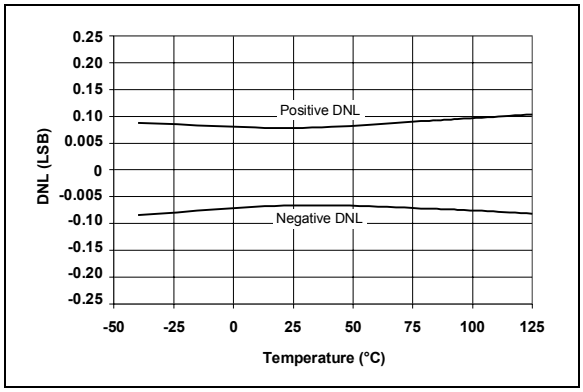


FIGURE 2-17: *DNL vs. Temperature (V_{DD} = 2.7V).*

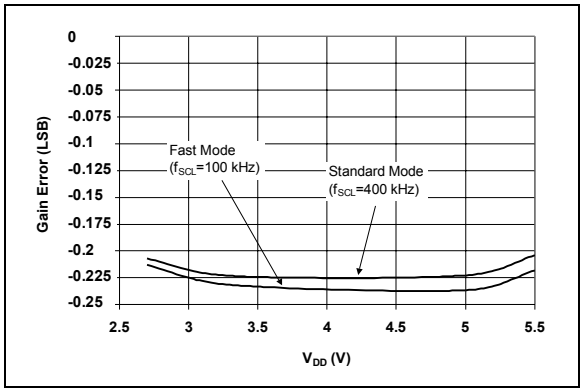


FIGURE 2-15: *Gain Error vs. V_{DD}.*

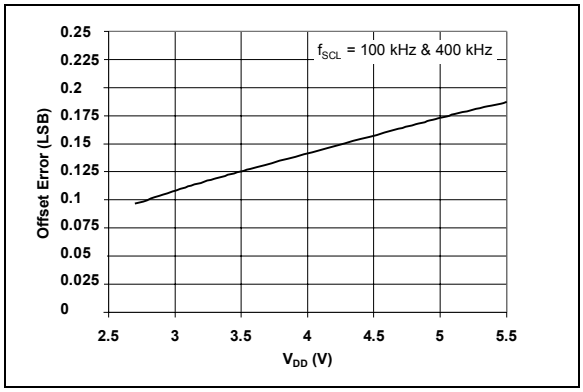


FIGURE 2-18: *Offset Error vs. V_{DD}.*

Note: Unless otherwise indicated, V_{DD} = 5V, V_{SS} = 0V, I^2C Fast Mode Timing (SCL = 400 kHz), Continuous Conversion Mode (f_{SAMP} = 22.3 ksps), T_A = +25°C.

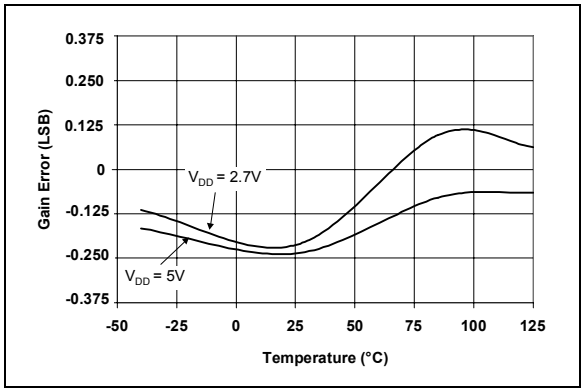


FIGURE 2-19: *Gain Error vs. Temperature.*

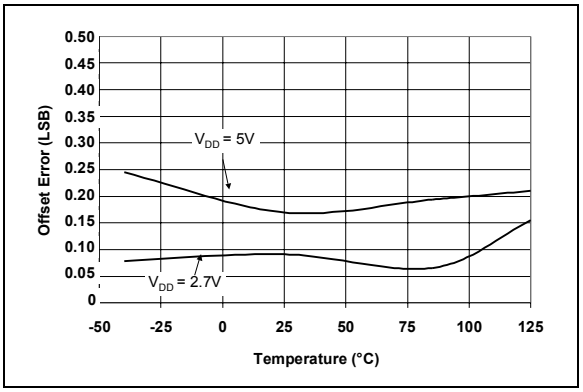


FIGURE 2-22: *Offset Error vs. Temperature.*

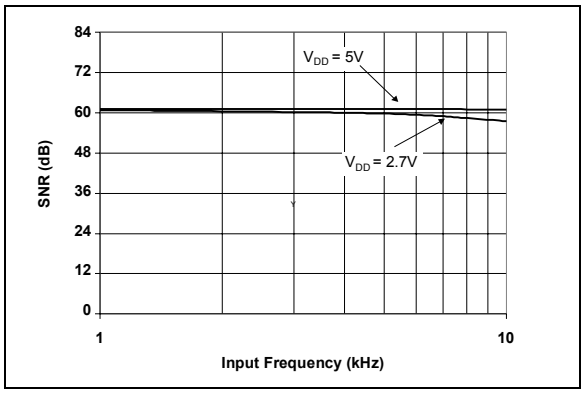


FIGURE 2-20: *SNR vs. Input Frequency.*

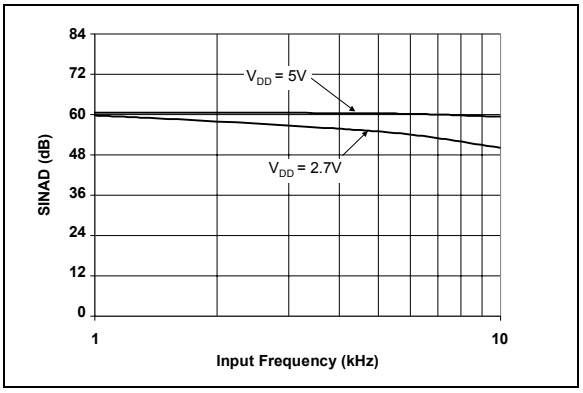


FIGURE 2-23: *SINAD vs. Input Frequency.*

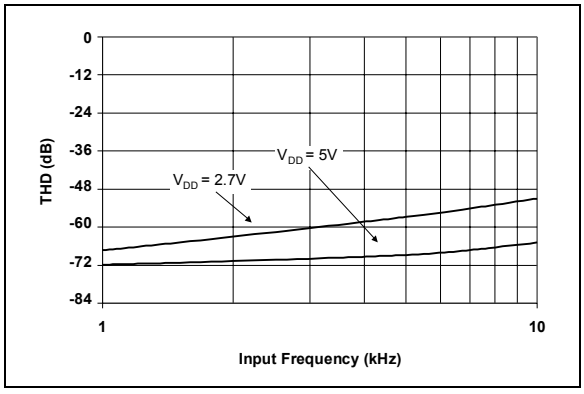


FIGURE 2-21: *THD vs. Input Frequency.*

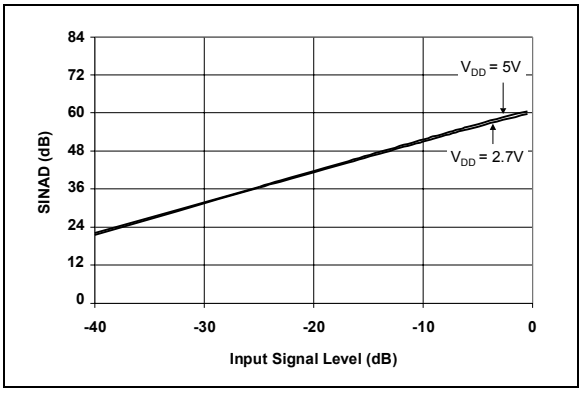


FIGURE 2-24: *SINAD vs. Input Signal Level.*

Note: Unless otherwise indicated, V_{DD} = 5V, V_{SS} = 0V, I^2C Fast Mode Timing (SCL = 400 kHz), Continuous Conversion Mode (f_{SAMP} = 22.3 ksps), T_A = +25°C.

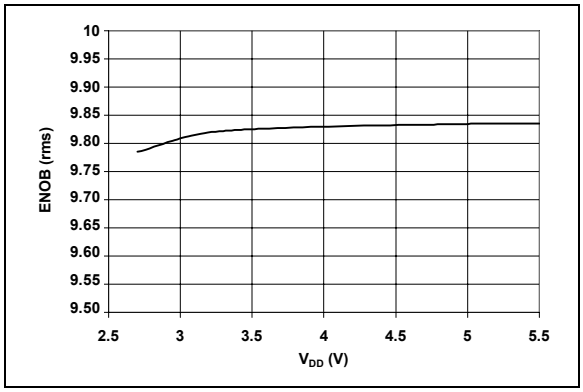


FIGURE 2-25: *ENOB vs. V_{DD}.*

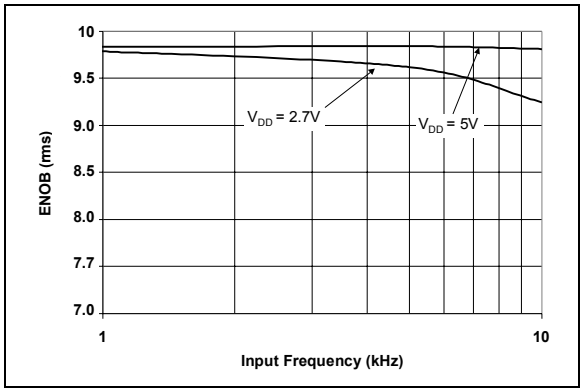


FIGURE 2-28: *ENOB vs. Input Frequency.*

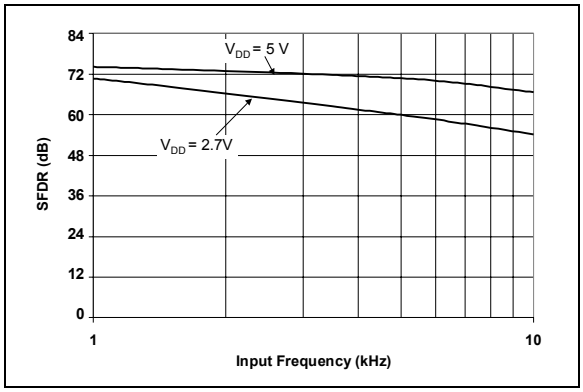


FIGURE 2-26: *SFDR vs. Input Frequency.*

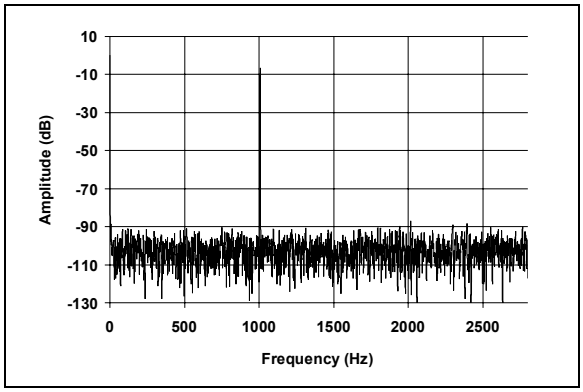


FIGURE 2-29: *Spectrum Using I^2C Standard Mode (Representative Part, 1 kHz Input Frequency).*

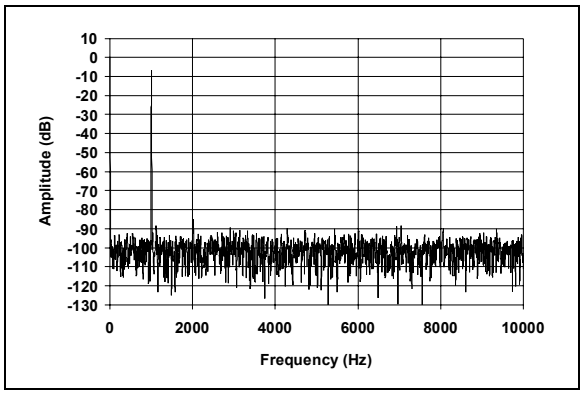


FIGURE 2-27: *Spectrum Using I^2C Fast Mode (Representative Part, 1 kHz Input Frequency).*

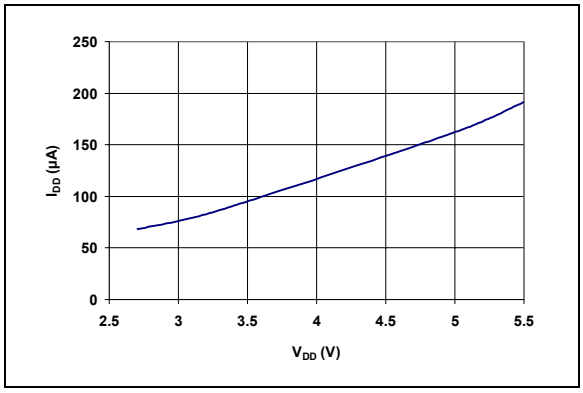


FIGURE 2-30: *I_{DD} (Conversion) vs. V_{DD}.*

Note: Unless otherwise indicated, V_{DD} = 5V, V_{SS} = 0V, I^2C Fast Mode Timing (SCL = 400 kHz), Continuous Conversion Mode (f_{SAMP} = 22.3 ksps), T_A = +25°C.

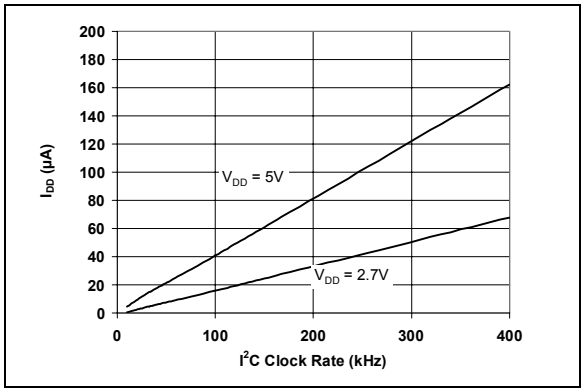


FIGURE 2-31: *I_{DD} (Conversion) vs. Clock Rate.*

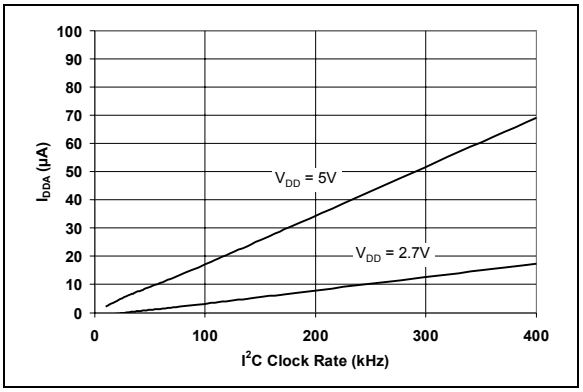


FIGURE 2-34: *I_{DDA} (Active Bus) vs. Clock Rate.*

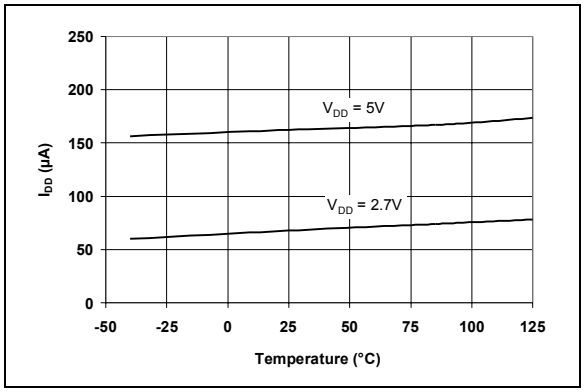


FIGURE 2-32: *I_{DD} (Conversion) vs. Temperature.*

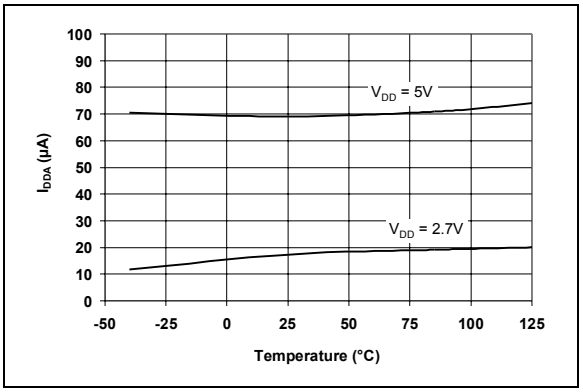


FIGURE 2-35: *I_{DDA} (Active Bus) vs. Temperature.*

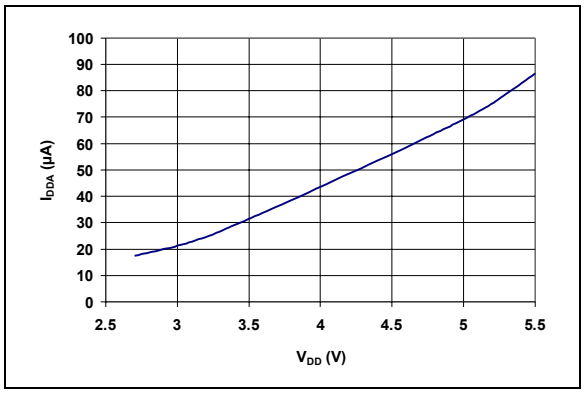


FIGURE 2-33: *I_{DDA} (Active Bus) vs. V_{DD}.*

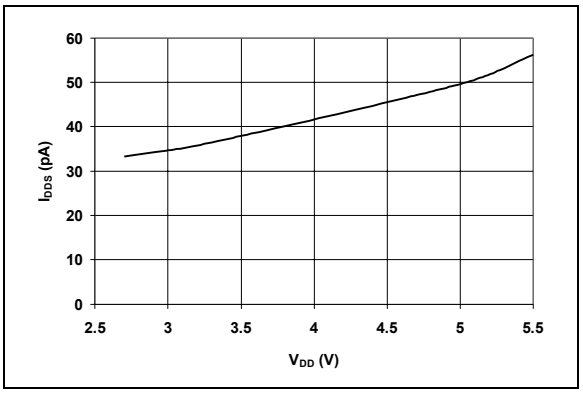


FIGURE 2-36: *I_{DDS} (Standby) vs. V_{DD}.*

Note: Unless otherwise indicated, V_{DD} = 5V, V_{SS} = 0V, I^2C Fast Mode Timing (SCL = 400 kHz), Continuous Conversion Mode (f_{SAMP} = 22.3 ksps), T_A = +25°C.

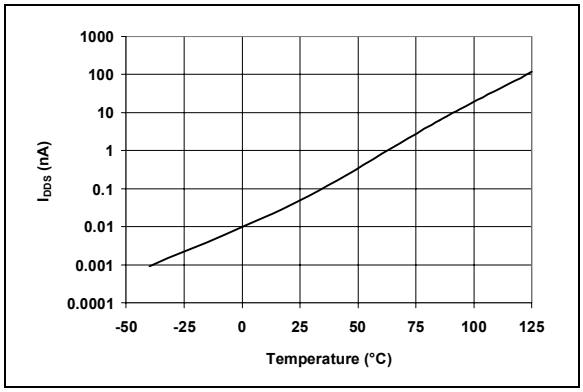


FIGURE 2-37: *I_{DDS} (Standby) vs. Temperature.*

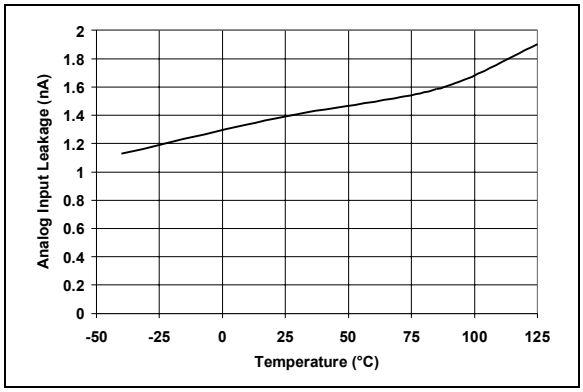


FIGURE 2-38: *Analog Input Leakage vs. Temperature.*

2.1 Test Circuit

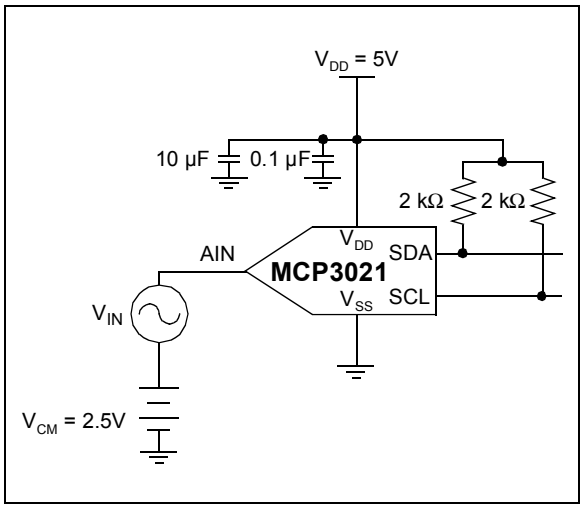


FIGURE 2-39: *Typical Test Configuration.*

3.0 PIN FUNCTIONS

TABLE 3-1: PIN FUNCTION TABLE

Name	Function
V_{DD}	+2.7V to 5.5V Power Supply
V_{SS}	Ground
AIN	Analog Input
SDA	Serial Data In/Out
SCL	Serial Clock In

3.1 V_{DD} and V_{SS}

The V_{DD} pin, with respect to V_{SS}, provides power to the device, as well as a voltage reference for the conversion process. Refer to Section 6.4, “Device Power and Layout Considerations”, for tips on power and grounding.

3.2 Analog Input (AIN)

AIN is the input pin to the sample and hold circuitry of the Successive Approximation Register (SAR) converter. Care should be taken in driving this pin. Refer to Section 6.1, “Driving the Analog Input”. For proper conversions, the voltage on this pin can vary from V_{SS} to V_{DD}.

3.3 Serial Data (SDA)

This is a bidirectional pin used to transfer addresses and data into and out of the device. It is an open-drain terminal, therefore, the SDA bus requires a pull-up resistor to V_{DD} (typically 10 kΩ for 100 kHz and 2 kΩ for 400 kHz SCL clock speeds (refer to Section 6.2, “Connecting to the I^2C Bus”).

For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions (refer to Section 5.1, “I^2C Bus Characteristics”).

3.4 Serial Clock (SCL)

SCL is an input pin used to synchronize the data transfer to and from the device on the SDA pin and is an open-drain terminal. Therefore, the SCL bus requires a pull-up resistor to V_{DD} (typically, 10 kΩ for 100 kHz and 2 kΩ for 400 kHz SCL clock speeds. Refer to Section 6.2, “Connecting to the I^2C Bus”).

For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions (refer to Section 6.1, “Driving the Analog Input”).

4.0 DEVICE OPERATION

The MCP3021 employs a classic SAR architecture. This architecture uses an internal sample and hold capacitor to store the analog input while the conversion is taking place. At the end of the acquisition time, the input switch of the converter opens and the device uses the collected charge on the internal sample and hold capacitor to produce a serial 10-bit digital output code. The acquisition time and conversion is self-timed using an internal clock. After each conversion, the results are stored in a 10-bit register that can be read at any time.

Communication with the device is accomplished with a 2-wire I^2C interface. Maximum sample rates of 22.3 ksps are possible with the MCP3021 in a continuous conversion mode and an SCL clock rate of 400 kHz.

4.1 Digital Output Code

The digital output code produced by the MCP3021 is a function of the input signal and power supply voltage (V_{DD}). As the V_{DD} level is reduced, the LSB size is reduced accordingly. The theoretical LSB size is shown below.

EQUATION

$$LSB\ SIZE = \frac{V_{DD}}{1024}$$

V_{DD} = Supply voltage

The output code of the MCP3021 is transmitted serially with MSB first, the format of the code being straight binary.

4.2 Conversion Time (t_{CONV})

The conversion time is the time required to obtain the digital result once the analog input is disconnected from the holding capacitor. With the MCP3021, the specified conversion time is typically 8.96 µs. This time is dependent on the internal oscillator and independent of SCL.

4.3 Acquisition Time (t_{ACQ})

The acquisition time is the amount of time the sample cap array is acquiring charge.

The acquisition time is, typically, 1.12 µs. This time is dependent on the internal oscillator and independent of SCL.

4.4 Sample Rate

Sample rate is the inverse of the maximum amount of time that is required from the point of acquisition of the first conversion to the point of acquisition of the second conversion.

The sample rate can be measured either by single or continuous conversions. A single conversion includes a Start Bit, Address Byte, Two Data Bytes and a Stop bit. This sample rate is measured from one Start Bit to the next Start Bit.

For continuous conversions (requested by the Master by issuing an acknowledge after a conversion), the maximum sample rate is measured from conversion to conversion, or a total of 18 clocks (two data bytes and two Acknowledge bits). Refer to Section 5-2, “Device Addressing”.

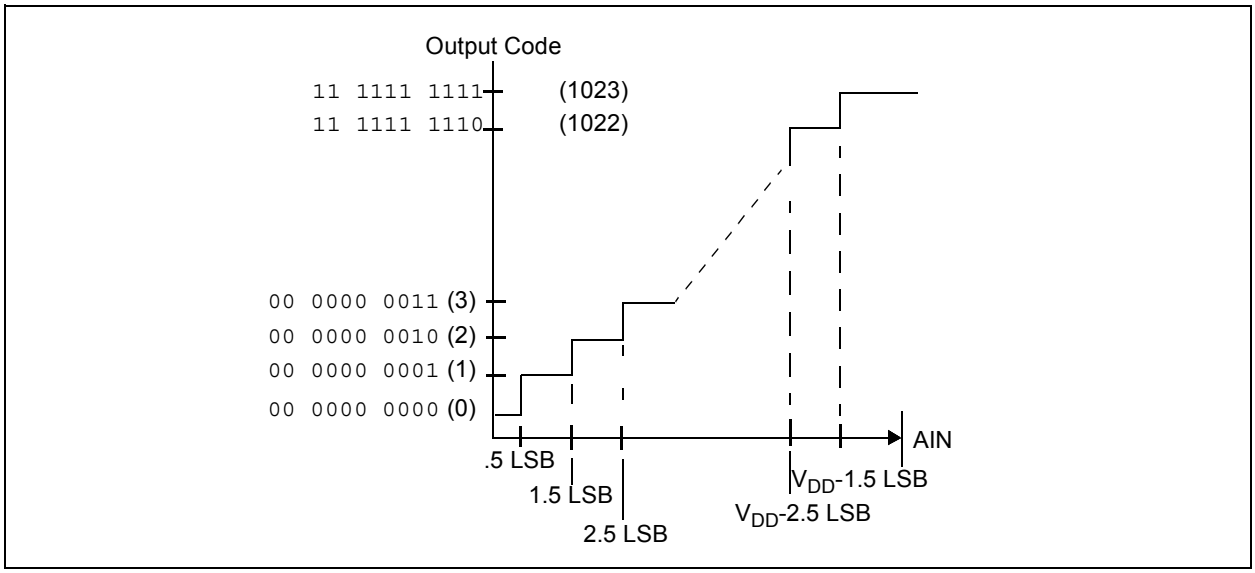


FIGURE 4-1: *Transfer Function.*

4.5 Differential Non-Linearity (DNL)

In the ideal ADC transfer function, each code has a uniform width. That is, the difference in analog input voltage is constant from one code transition point to the next. DNL specifies the deviation of any code in the transfer function from an ideal code width of 1 LSB. The DNL is determined by subtracting the locations of successive code transition points after compensating for any gain and offset errors. A positive DNL implies that a code is longer than the ideal code width, while a negative DNL implies that a code is shorter than the ideal width.

4.6 Integral Non-Linearity (INL)

INL is a result of cumulative DNL errors and specifies how much the overall transfer function deviates from a linear response. The method of measurement used in the MCP3021 ADC to determine INL is the “end-point” method.

4.7 Offset Error

Offset error is defined as a deviation of the code transition points that are present across all output codes. This has the effect of shifting the entire A/D transfer function. The offset error is measured by finding the difference between the actual location of the first code transition and the desired location of the first transition. The ideal location of the first code transition is located at 1/2 LSB above V_{SS}.

4.8 Gain Error

The gain error determines the amount of deviation from the ideal slope of the ADC transfer function. Before the gain error is determined, the offset error is measured and subtracted from the conversion result. The gain error can then be determined by finding the location of the last code transition and comparing that location to the ideal location. The ideal location of the last code transition is 1.5 LSBs below full-scale or V_{DD}.

4.9 Conversion Current (I_{DD})

The average amount of current over the time required to perform a 10-bit conversion.

4.10 Active Bus Current (I_{DDA})

The average amount of current over the time required to monitor the I^2C bus. Any current the device consumes while it is not being addressed is referred to as Active Bus current.

4.11 Standby Current (I_{DDS})

The average amount of current required while no conversion is occurring and while no data is being output (i.e., SCL and SDA lines are quiet).

4.12 I^2C Standard Mode Timing

I^2C specification where the frequency of SCL is 100 kHz.

4.13 I^2C Fast Mode Timing

I^2C specification where the frequency of SCL is 400 kHz.

5.0 SERIAL COMMUNICATIONS

5.1 I^2C Bus Characteristics

The following bus protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (refer to Figure 5-1).

5.1.1 BUS NOT BUSY (A)

Both data and clock lines remain high.

5.1.2 START DATA TRANSFER (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a START condition. All commands must be preceded by a START condition.

5.1.3 STOP DATA TRANSFER (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a STOP condition. All operations must be ended with a STOP condition.

5.1.4 DATA VALID (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between the START and STOP conditions is determined by the master device and is unlimited.

5.1.5 ACKNOWLEDGE

Each receiving device, when addressed, is obliged to generate an acknowledge bit after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge-related clock pulse. Setup and hold times must be taken into account. During reads, a master device must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave (NAK). In this case, the slave (MCP3021) will release the bus to allow the master device to generate the STOP condition.

The MCP3021 supports a bidirectional 2-wire bus and data transmission protocol. The device that sends data onto the bus is the transmitter and the device receiving data is the receiver. The bus has to be controlled by a master device that generates the serial clock (SCL), controls the bus access and generates the START and STOP conditions, while the MCP3021 works as a slave device. Both master and slave devices can operate as either transmitter or receiver, but the master device determines which mode is activated.

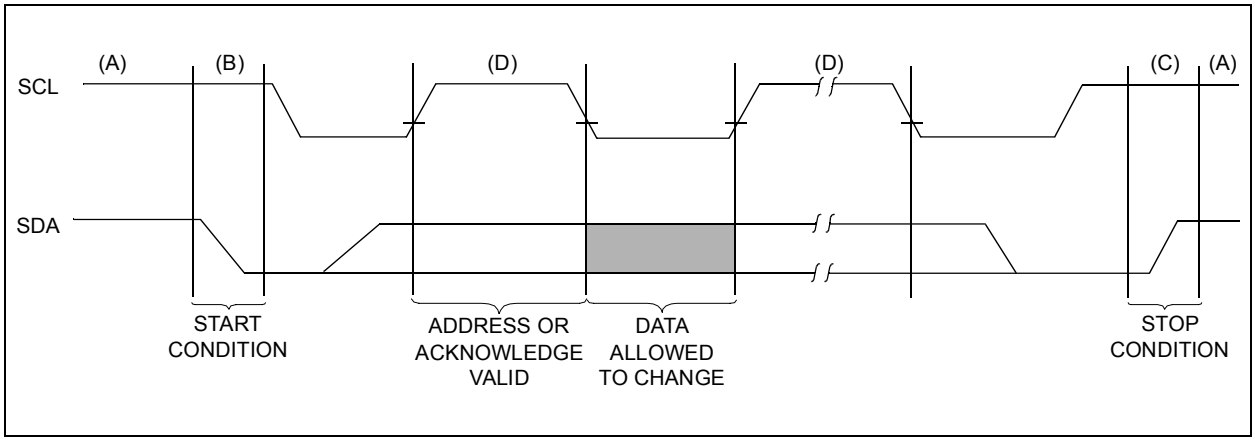


FIGURE 5-1: *Data Transfer Sequence on the Serial Bus.*

5.2 Device Addressing

The address byte is the first byte received following the START condition from the master device. The first part of the control byte consists of a 4-bit device code, which is set to 1001 for the MCP3021. The device code is followed by three address bits: A2, A1 and A0. The default address bits are 101 (contact the Microchip factory for additional address bit options).The address bits allow up to eight MCP3021 devices on the same bus and are used to determine which device is accessed.

The eighth bit of the slave address determines if the master device wants to read conversion data or write to the MCP3021. When set to a '1', a read operation is selected. When set to a '0', a write operation is selected. There are no writable registers on the MCP3021, therefore, this bit must be set to a '1' to initiate a conversion.

The MCP3021 is a slave device that is compatible with the 2-wire I^2C serial interface protocol. A hardware connection diagram is shown in Figure 6-2. Communication is initiated by the microcontroller (master device), which sends a START bit followed by the address byte.

On completion of the conversion(s) performed by the MCP3021, the microcontroller must send a STOP bit to stop the communication.

The last bit in the device address byte is the R/$\overline{W}$ bit. When this bit is a logic '1', a conversion will be executed. Setting this bit to logic '0' will also result in an "acknowledge" (ACK) from the MCP3021, with the device then releasing the bus. This can be used for device polling (refer to Section 6.3, "Device Polling").

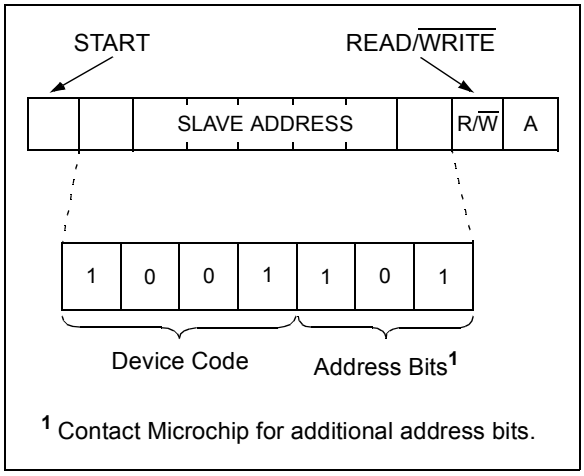


FIGURE 5-2: *Device Addressing.*

5.3 Executing a Conversion

This section will describe the details of communicating with the MCP3021 device. Initiating the sample and hold acquisition, reading the conversion data and executing multiple conversions will be discussed.

5.3.1 INITIATING THE SAMPLE AND HOLD

The acquisition and conversion of the input signal begins with the falling edge of the R/$\overline{W}$ bit of the address byte. At this point, the internal clock initiates the sample, hold and conversion cycle, all of which are internal to the ADC.

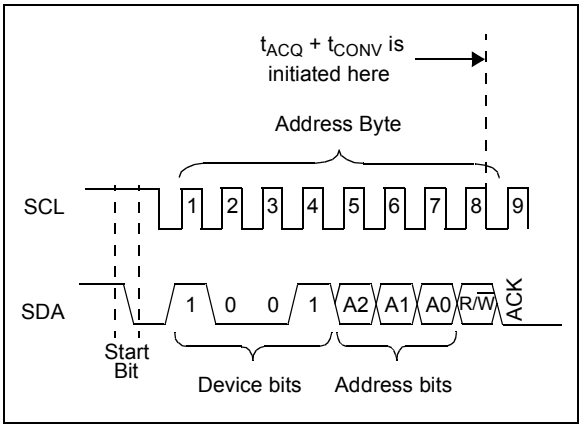


FIGURE 5-3: *Initiating the Conversion, Address Byte.*

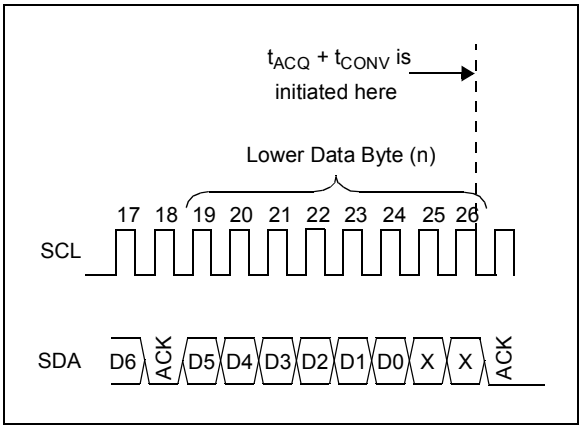


FIGURE 5-4: *Initiating the Conversion, Continuous Conversions.*

The input signal will initially be sampled with the first falling edge of the clock following the transmission of a logic-high R/$\overline{W}$ bit. Additionally, with the rising edge of the SCL, the ADC will transmit an acknowledge bit (ACK = 0). The master must release the data bus during this clock pulse to allow the MCP3021 to pull the line low (refer to Figure 5-3).

For consecutive samples, sampling begins on the last bit of the lower data byte. Refer to Figure 5-6 for timing diagram.

5.3.2 READING THE CONVERSION DATA

After the MCP3021 acknowledges the address byte, the device will transmit four '0' bits followed by the upper four data bits of the conversion. The master device will then acknowledge this byte with an ACK = low. With the following six clock pulses, the MCP3021 will transmit the lower six data bits from the conversion. The last two bits are "don't cares", and do not contain valid data. The master then sends an ACK = high, indicating to the MCP3021 that no more data is requested. The master can then send a stop bit to end the transmission.

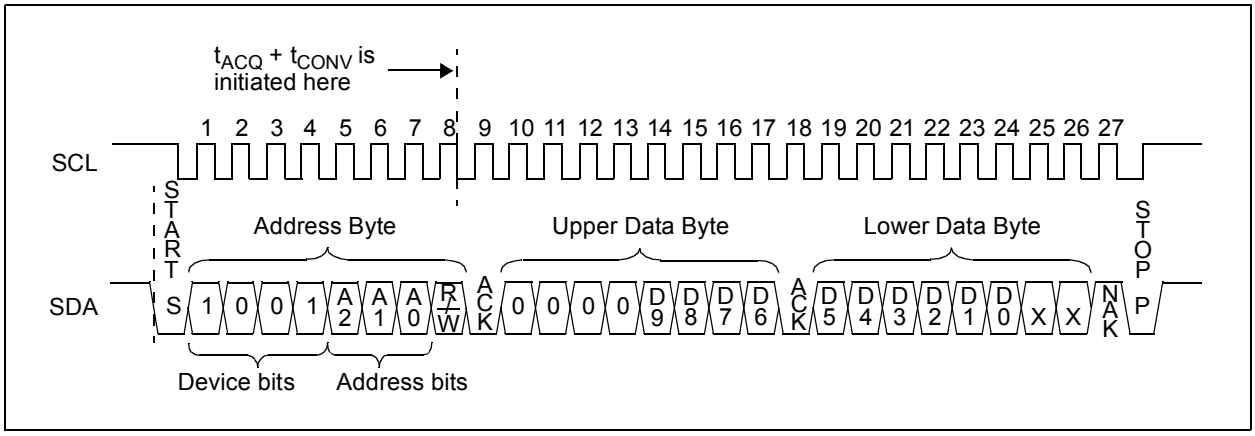


FIGURE 5-5: *Executing a Conversion.*

5.3.3 CONSECUTIVE CONVERSIONS

For consecutive samples, sampling begins on the falling edge of the last bit of the lower data byte. See Figure 5-6 for timing.

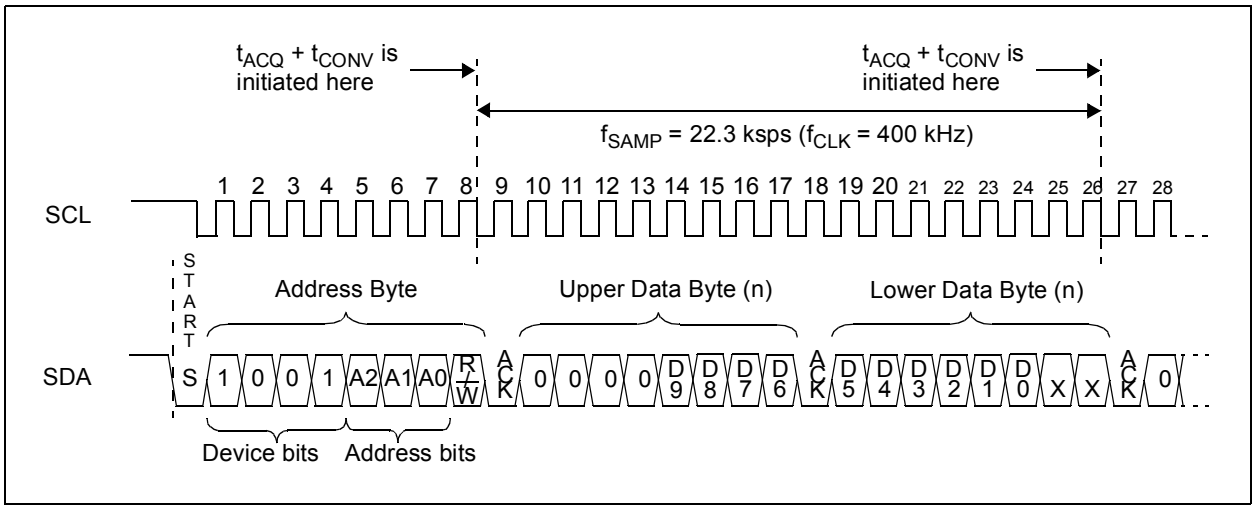


FIGURE 5-6: *Continuous Conversion.*

6.0 APPLICATIONS INFORMATION

6.1 Driving the Analog Input

The MCP3021 has a single-ended analog input (AIN). For proper conversion results, the voltage at the AIN pin must be kept between V_{SS} and V_{DD}. If the converter has no offset error, gain error, INL or DNL errors and the voltage level of AIN is equal to or less than V_{SS} + 1/2 LSB, the resultant code will be `000h`. Additionally, if the voltage at AIN is equal to or greater than V_{DD} - 1.5 LSB, the output code will be `1FFh`.

The analog input model is shown in Figure 6-1. In this diagram, the source impedance (R_{SS}) adds to the internal sampling switch (R_S) impedance, directly affecting the time required to charge the capacitor (C_{SAMPLE}). Consequently, a larger source impedance increases the offset error, gain error and integral linearity errors of the conversion. Ideally, the impedance of the signal source should be near zero. This is achievable with an operational amplifier such as the MCP6022, which has a closed-loop output impedance of tens of ohms.

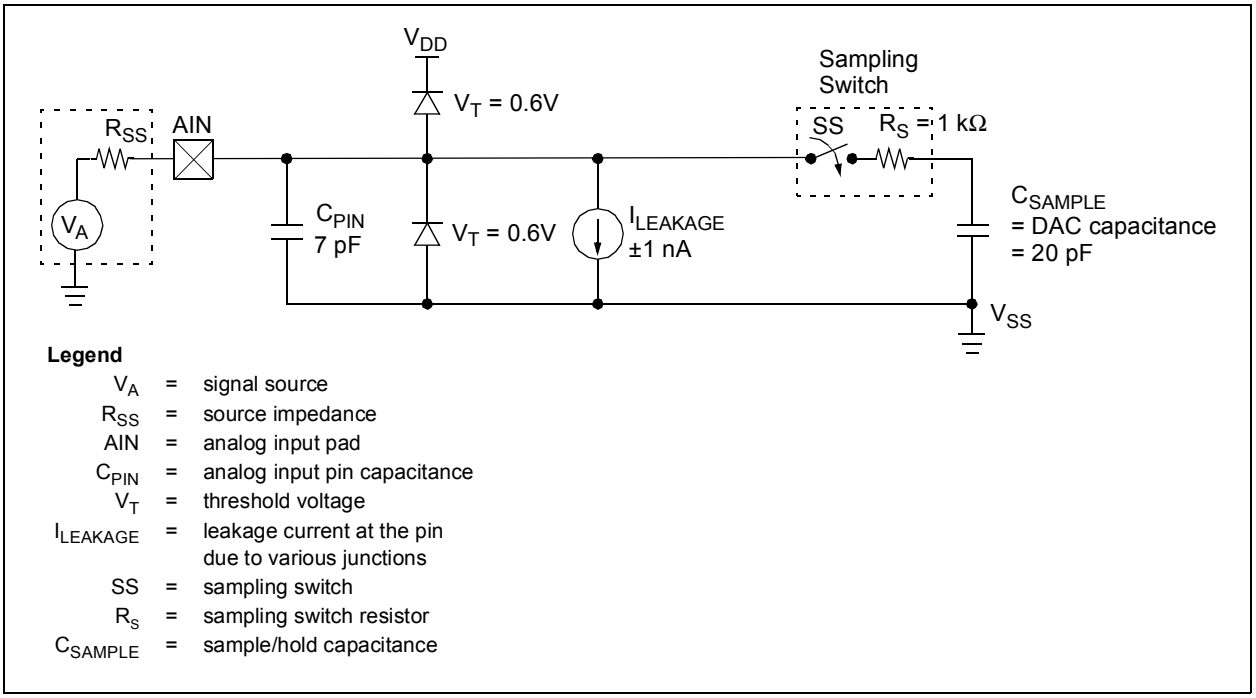


FIGURE 6-1: *Analog Input Model, AIN.*

6.2 Connecting to the I^2C Bus

The I^2C bus is an open collector bus, requiring pull-up resistors connected to the SDA and SCL lines. This configuration is shown in Figure 6-2.

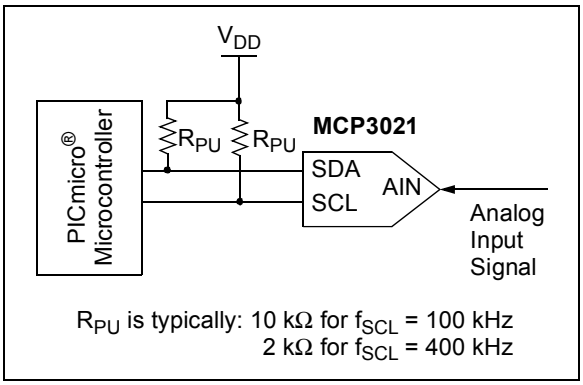


FIGURE 6-2: *Pull-up Resistors on I^2C Bus.*

The number of devices connected to the bus is limited only by the maximum bus capacitance of 400 pF. A possible configuration using multiple devices is shown in Figure 6-3.

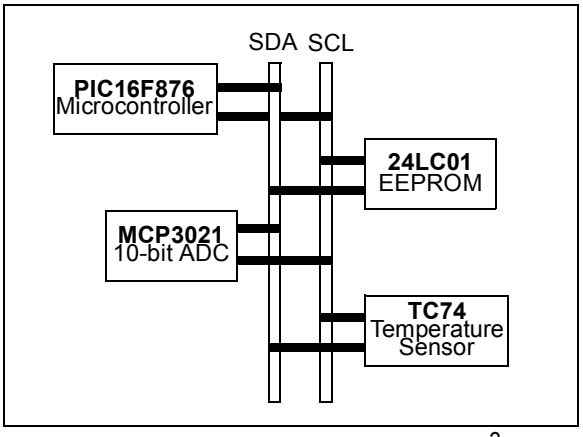


FIGURE 6-3: *Multiple Devices on I^2C Bus.*

6.3 Device Polling

In some instances, it may be necessary to test for MCP3021 presence on the I^2C bus without performing a conversion, described in Figure 6-4. Here we are setting the R/$\overline{W}$ bit in the address byte to a zero. The MCP3021 will then acknowledge by pulling SDA low during the ACK clock and then release the bus back to the I^2C master. A stop or repeated start bit can then be issued from the master and I^2C communication can continue.

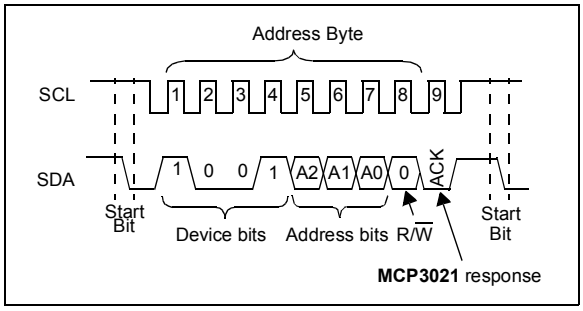


FIGURE 6-4: *Device Polling.*

6.4 Device Power and Layout Considerations

6.4.1 POWERING THE MCP3021

V_{DD} supplies the power to the device as well as the reference voltage. A bypass capacitor value of 0.1 µF is recommended. Adding a 10 µF capacitor in parallel is recommended to attenuate higher frequency noise present in some systems.

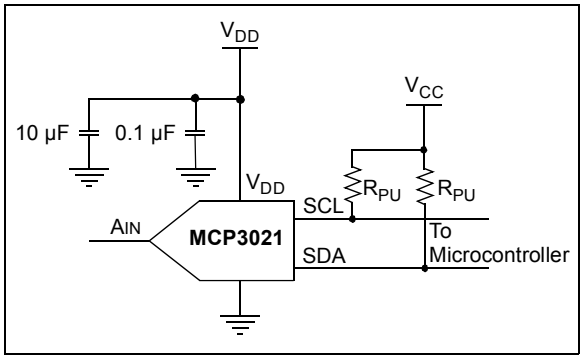


FIGURE 6-5: *Powering the MCP3021.*

6.4.2 LAYOUT CONSIDERATIONS

When laying out a printed circuit board for use with analog components, care should be taken to reduce noise wherever possible. A bypass capacitor from V_{DD} to ground should always be used with this device and should be placed as close as possible to the device pin. A bypass capacitor value of 0.1 µF is recommended.

Digital and analog traces should be separated as much as possible on the board, with no traces running underneath the device or the bypass capacitor. Extra precautions should be taken to keep traces with high frequency signals (such as clock lines) as far as possible from analog traces.

The MCP3021 should be connected entirely to the analog ground place, as well as the analog power trace. The pull-up resistors can be placed close to the microcontroller and tied to the digital power or V_{CC}.

Use of an analog ground plane is recommended in order to keep the ground potential the same for all devices on the board. Providing V_{DD} connections to devices in a "star" configuration can also reduce noise by eliminating current return paths and associated errors (Figure 6-6). For more information on layout tips when using the MCP3021 or other ADC devices, refer to AN688, *"Layout Tips for 12-Bit A/D Converter Applications"*.

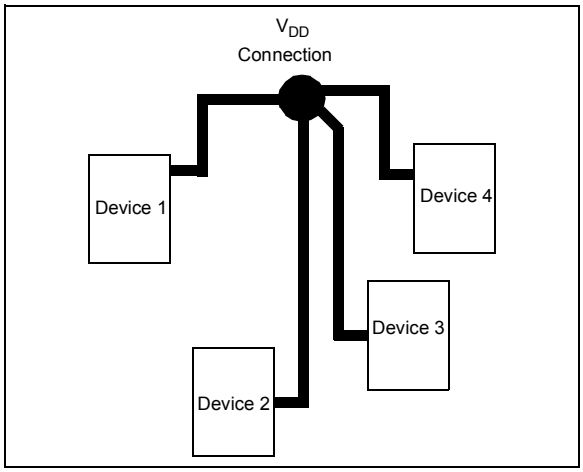


FIGURE 6-6: *V_{DD} traces arranged in a 'Star' configuration in order to reduce errors caused by current return paths.*

6.4.3 USING A REFERENCE FOR SUPPLY

The MCP3021 uses V_{DD} as power and also as a reference. In some applications, it may be necessary to use a stable reference to achieve the required accuracy. Figure 6-7 shows an example using the MCP1541 as a 4.096V 2% reference.

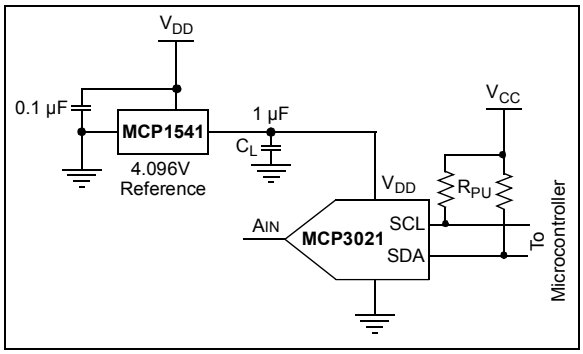
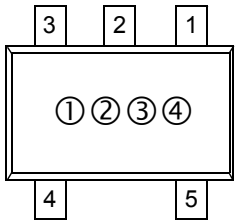


FIGURE 6-7: *Stable Power and Reference Configuration.*

7.0 PACKAGING INFORMATION

7.1 Package Marking Information

5-Pin SOT-23A (EIAJ SC-74) Device



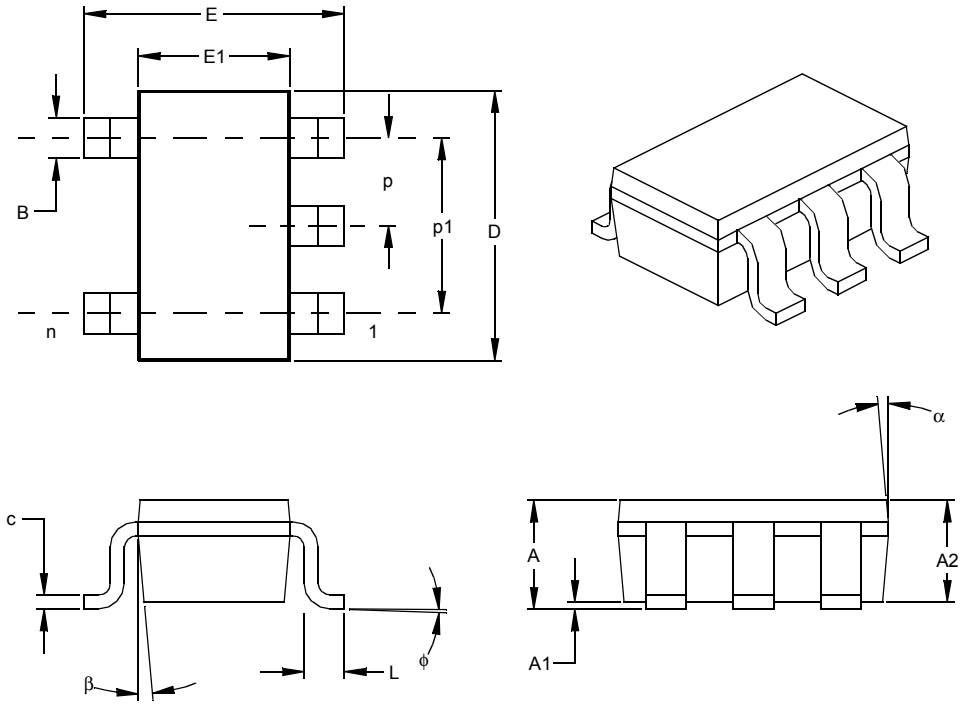
Part Number	Address Option	SOT-23
MCP3021A0T-E/OT	000	GP
MCP3021A1T-E/OT	001	GS
MCP3021A2T-E/OT	010	GK
MCP3021A3T-E/OT	011	GL
MCP3021A4T-E/OT	100	GM
MCP3021A5T-E/OT	101	GJ *
MCP3021A6T-E/OT	110	GQ
MCP3021A7T-E/OT	111	GR

* Default option. Contact Microchip Factory for other address options.

Legend:	1	Part Number code + temperature range
	2	Part Number code + temperature range
	3	Year and work week
	4	Lot ID
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.	

***** Standard device marking consists of Microchip part number, year code, week code, and traceability code.

5-Lead Plastic Small Outline Transistor (OT) (SOT23)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		5			5	
Pitch	p		.038			0.95	
Outside lead pitch (basic)	p1		.075			1.90	
Overall Height	A	.035	.046	.057	0.90	1.18	1.45
Molded Package Thickness	A2	.035	.043	.051	0.90	1.10	1.30
Standoff §	A1	.000	.003	.006	0.00	0.08	0.15
Overall Width	E	.102	.110	.118	2.60	2.80	3.00
Molded Package Width	E1	.059	.064	.069	1.50	1.63	1.75
Overall Length	D	.110	.116	.122	2.80	2.95	3.10
Foot Length	L	.014	.018	.022	0.35	0.45	0.55
Foot Angle	ϕ	0	5	10	0	5	10
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.014	.017	.020	0.35	0.43	0.50
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MO-178
Drawing No. C04-091

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XX	X	/XX
Device	Address Options	Temperature Range	Package

Device: MCP3021T: 10-Bit 2-Wire Serial A/D Converter (Tape and Reel)

Temperature Range: E = -40°C to +125°C

Address Options:

XX		A2	A1	A0
A0	=	0	0	0
A1	=	0	0	1
A2	=	0	1	0
A3	=	0	1	1
A4	=	1	0	0
A5 *	=	1	0	1
A6	=	1	1	0
A7	=	1	1	1

* Default option. Contact Microchip factory for other address options

Package: OT = SOT-23, 5-lead (Tape and Reel)

Examples:

a) MCP3021A0T-E/OT: Extended, A0 Address, Tape and Reel

b) MCP3021A1T-E/OT: Extended, A1 Address, Tape and Reel

c) MCP3021A2T-E/OT: Extended, A2 Address, Tape and Reel

d) MCP3021A3T-E/OT: Extended, A3 Address, Tape and Reel

e) MCP3021A4T-E/OT: Extended, A4 Address, Tape and Reel

f) MCP3021A5T-E/OT: Extended, A5 Address, Tape and Reel

g) MCP3021A6T-E/OT: Extended, A6 Address, Tape and Reel

h) MCP3021A7T-IE/OT: Extended, A7 Address, Tape and Reel

Sales and Support

Data Sheets
Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

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NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200 Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: http://www.microchip.com

Atlanta
3780 Mansell Road, Suite 130
Alpharetta, GA 30022
Tel: 770-640-0034 Fax: 770-640-0307

Boston
2 Lan Drive, Suite 120
Westford, MA 01886
Tel: 978-692-3848 Fax: 978-692-3821

Chicago
333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071 Fax: 630-285-0075

Dallas
4570 Westgrove Drive, Suite 160
Addison, TX 75001
Tel: 972-818-7423 Fax: 972-818-2924

Detroit
Tri-Atria Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250 Fax: 248-538-2260

Kokomo
2767 S. Albright Road
Kokomo, IN 46902
Tel: 765-864-8360 Fax: 765-864-8387

Los Angeles
18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888 Fax: 949-263-1338

Phoenix
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7966 Fax: 480-792-4338

San Jose
Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

Toronto
6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699 Fax: 905-673-6509

ASIA/PACIFIC

Australia
Microchip Technology Australia Pty Ltd
Marketing Support Division
Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

China - Beijing
Microchip Technology Consulting (Shanghai) Co., Ltd., Beijing Liaison Office
Unit 915
Bei Hai Wan Tai Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100 Fax: 86-10-85282104

China - Chengdu
Microchip Technology Consulting (Shanghai) Co., Ltd., Chengdu Liaison Office
Rm. 2401-2402, 24th Floor,
Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-86766200 Fax: 86-28-86766599

China - Fuzhou
Microchip Technology Consulting (Shanghai) Co., Ltd., Fuzhou Liaison Office
Unit 28F, World Trade Plaza
No. 71 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7503506 Fax: 86-591-7503521

China - Hong Kong SAR
Microchip Technology Hongkong Ltd.
Unit 901-6, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200 Fax: 852-2401-3431

China - Shanghai
Microchip Technology Consulting (Shanghai) Co., Ltd.
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

China - Shenzhen
Microchip Technology Consulting (Shanghai) Co., Ltd., Shenzhen Liaison Office
Rm. 1812, 18/F, Building A, United Plaza
No. 5022 Binhe Road, Futian District
Shenzhen 518033, China
Tel: 86-755-82901380 Fax: 86-755-8295-1393

China - Qingdao
Rm. B505A, Fullhope Plaza,
No. 12 Hong Kong Central Rd.
Qingdao 266071, China
Tel: 86-532-5027355 Fax: 86-532-5027205

India
Microchip Technology Inc.
India Liaison Office
Marketing Support Division
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaugnessey Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan
Microchip Technology Japan K.K.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471- 6166 Fax: 81-45-471-6122

Korea
Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-882
Tel: 82-2-554-7200 Fax: 82-2-558-5934

Singapore
Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-6334-8870 Fax: 65-6334-8850

Taiwan
Microchip Technology (Barbados) Inc.,
Taiwan Branch
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Austria
Microchip Technology Austria GmbH
Durisolstrasse 2
A-4600 Wels
Austria
Tel: 43-7242-2244-399
Fax: 43-7242-2244-393

Denmark
Microchip Technology Nordic ApS
Regus Business Centre
Lautrup hoj 1-3
Ballerup DK-2750 Denmark
Tel: 45-4420-9895 Fax: 45-4420-9910

France
Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - ler Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany
Microchip Technology GmbH
Steinheilstrasse 10
D-85737 Ismaning, Germany
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy
Microchip Technology SRL
Via Quasimodo, 12
20025 Legnano (MI)
Milan, Italy
Tel: 39-0331-742611 Fax: 39-0331-466781

United Kingdom
Microchip Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44-118-921-5869 Fax: 44-118-921-5820

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