93AA86A/B/C, 93LC86A/B/C, 93C86A/B/C

16K Microwire® Compatible Serial EEPROM

Device Selection Table

Part Number	Vcc Range	ORG Pin	Word Size	Temp Ranges	Packages
93AA86A	1.8-5.5	No	8-bit	I	OT
93AA86B	1.8-5-5	No	16-bit	I	OT
93LC86A	2.5-5.5	No	8-bit	I, E	OT
93LC86B	2.5-5.5	No	16-bit	I, E	OT
93C86A	4.5-5.5	No	8-bit	I, E	OT
93C86B	4.5-5.5	No	16-bit	I, E	OT
93AA86C	1.8-5.5	Yes	8 or 16-bit	I	P, SN, ST, MS
93LC86C	2.5-5.5	Yes	8 or 16-bit	I, E	P, SN, ST, MS
93C86C	4.5-5.5	Yes	8 or 16-bit	I, E	P, SN, ST, MS

Features

- Low-power CMOS technology
- ORG pin to select word size for ‘86C’ version
- 2048 x 8-bit organization ‘A’ devices (no ORG)
- 1024 x 16-bit organization ‘B’ devices (no ORG)
- Program Enable pin to write-protect the entire array
- Self-timed ERASE/WRITE cycles (including auto-erase)
- Automatic ERAL before WRAL
- Power on/off data protection circuitry
- Industry standard 3-wire serial I/O
- Device STATUS signal (READY/$\overline{\text{BUSY}}$)
- Sequential READ function
- 1,000,000 E/W cycles
- Data retention > 200 years
- Temperature ranges supported:
  - Industrial (I) -40°C to +85°C
  - Automotive (E) -40°C to +125°C

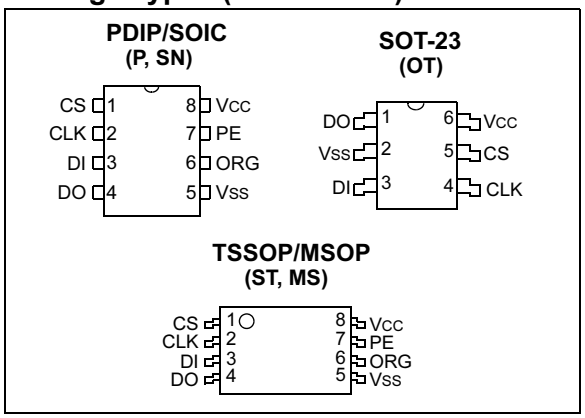
Pin Function Table

Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
Vss	Ground
PE	Program Enable
ORG	Memory Configuration
Vcc	Power Supply

Description

The Microchip Technology Inc. 93XX86A/B/C devices are 16K bit low-voltage serial Electrically Erasable PROMs (EEPROM). Word-selectable devices such as the 93XX86C are dependent upon external logic levels driving the ORG pin to set word size. For dedicated 8-bit communication, the 93XX86A devices are available, while the 93XX86B devices provide dedicated 16-bit communication. A Program Enable (PE) pin allows the user to write-protect the entire memory array. Advanced CMOS technology makes these devices ideal for low-power, nonvolatile memory applications. The entire 93XX Series is available in standard packages including 8-lead PDIP and SOIC, and advanced packaging including 8-lead MSOP, 6-lead SOT-23, and 8-lead TSSOP. Pb-free (Pure Matte Sn) finish is also available.

Package Types (not to scale)



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

V_{CC} 7.0V

All inputs and outputs w.r.t. V_{SS} ..... -0.6V to V_{CC} +1.0V

Storage temperature ..... -65°C to +150°C

Ambient temperature with power applied ..... -40°C to +125°C

ESD protection on all pins ..... ≥ 4 kV

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

All parameters apply over the specified ranges unless otherwise noted.			V_{CC} = range by device (see Table on Page 1) Industrial (I): T_{AMB} = -40°C to +85°C Automotive (E): T_{AMB} = -40°C to +125°C				
Param. No.	**Symbol**	**Parameter**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
D1	V_{IH1} V_{IH2}	High-level input voltage	2.0 0.7 V_{CC}	— —	V_{CC} +1 V_{CC} +1	V V	V_{CC} ≥ 2.7V V_{CC} < 2.7V
D2	V_{IL1} V_{IL2}	Low-level input voltage	-0.3 -0.3	— —	0.8 0.2 V_{CC}	V V	V_{CC} ≥ 2.7V V_{CC} < 2.7V
D3	Vol1 Vol2	Low-level output voltage	— —	— —	0.4 0.2	V V	I_{OL} = 2.1 mA, V_{CC} = 4.5V I_{OL} = 100 μA, V_{CC} = 2.5V
D4	V_{OH1} V_{OH2}	High-level output voltage	2.4 V_{CC} - 0.2	— —	— —	V V	I_{OH} = -400 μA, V_{CC} = 4.5V I_{OH} = -100 μA, V_{CC} = 2.5V
D5	I_{LI}	Input leakage current	—	—	±10	μA	V_{IN} = V_{SS} to V_{CC}
D6	I_{LO}	Output leakage current	—	—	±10	μA	V_{OUT} = V_{SS} to V_{CC}
D7	C_{IN}, C_{OUT}	Pin capacitance (all inputs/ outputs)	—	—	7	pF	V_{IN}/V_{OUT} = 0V **(Note 1)** T_{AMB} = 25°C, F_{CLK} = 1 MHz
D8	I_{CC} write	Write current	— —	— 500	3 —	mA μA	F_{CLK} = 3 MHz, V_{CC} = 5.5V F_{CLK} = 2 MHz, V_{CC} = 2.5V
D9	I_{CC} read	Read current	— — —	— — 100	1 500 —	mA μA μA	F_{CLK} = 3 MHz, V_{CC} = 5.5V F_{CLK} = 2 MHz, V_{CC} = 3.0V F_{CLK} = 2 MHz, V_{CC} = 2.5V
D10	I_{CCS}	Standby current	— —	— —	1 5	μA μA	I – Temp E – Temp CLK = Cs = 0V ORG = DI = V_{SS} or V_{CC} **(Note 2) (Note 3)**
D11	V_{POR}	V_{CC} voltage detect 93AA86A/B/C, 93LC86A/B/C 93C86A/B/C	— —	1.5V 3.8V	— —	V V	**(Note 1)**

Note 1: This parameter is periodically sampled and not 100% tested.

2: ORG pin not available on ‘A’ or ‘B’ versions.

3: READY/$\overline{BUSY}$ status must be cleared from DO, see **Section 3.4 “Data Out (DO)”**.

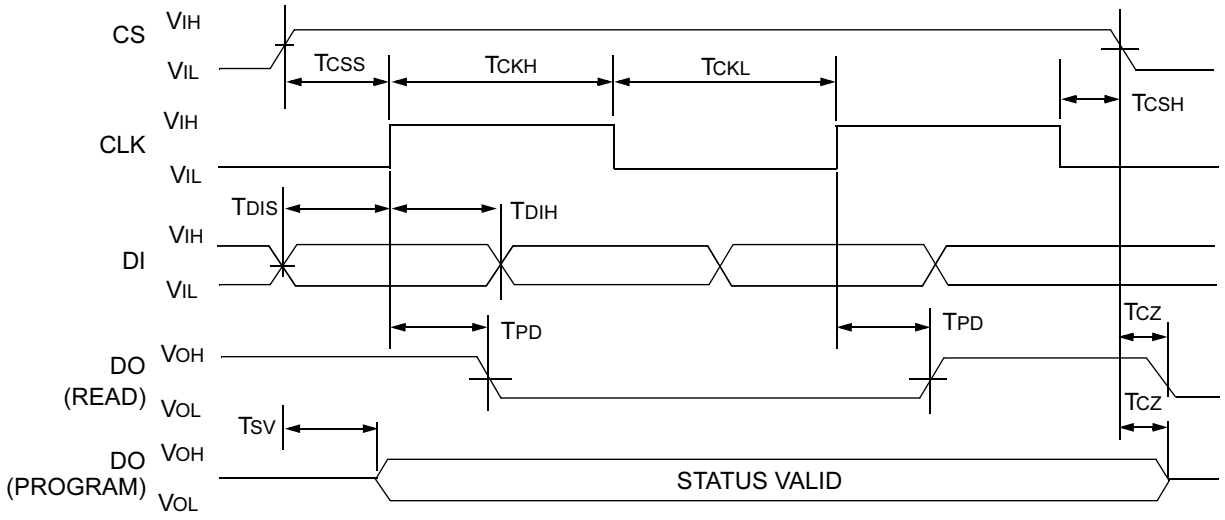
AC CHARACTERISTICS

All parameters apply over the specified ranges unless otherwise noted.			VCC = range by device (see Table on Page 1) Industrial (I): TAMB = -40°C to +85°C Automotive (E): TAMB = -40°C to +125°C			
Param. No.	**Symbol**	**Parameter**	**Min**	**Max**	**Units**	**Conditions**
A1	FCLK	Clock frequency	—	3 2 1	MHz MHz MHz	4.5V ≤ VCC < 5.5V 2.5V ≤ VCC < 4.5V 1.8V ≤ VCC < 2.5V
A2	TCKH	Clock high time	200 250 450	—	ns ns ns	4.5V ≤ VCC < 5.5V 2.5V ≤ VCC < 4.5V 1.8V ≤ VCC < 2.5V
A3	TCKL	Clock low time	100 200 450	—	ns ns ns	4.5V ≤ VCC < 5.5V 2.5V ≤ VCC < 4.5V 1.8V ≤ VCC < 2.5V
A4	TCSS	Chip select setup time	50 100 250	—	ns ns ns	4.5V ≤ VCC < 5.5V 2.5V ≤ VCC < 4.5V 1.8V ≤ VCC < 2.5V
A5	TCSH	Chip select hold time	0	—	ns	1.8V ≤ VCC < 5.5V
A6	TCSL	Chip select low time	250	—	ns	1.8V ≤ VCC < 5.5V
A7	TDIS	Data input setup time	50 100 250	—	ns ns ns	4.5V ≤ VCC < 5.5V 2.5V ≤ VCC < 4.5V 1.8V ≤ VCC < 2.5V
A8	TDIH	Data input hold time	50 100 250	—	ns ns ns	4.5V ≤ VCC < 5.5V 2.5V ≤ VCC < 4.5V 1.8V ≤ VCC < 2.5V
A9	TPD	Data output delay time	—	100 250 400	ns ns ns	4.5V ≤ VCC < 5.5V, CL = 100 pF 2.5V ≤ VCC < 4.5V, CL = 100 pF 1.8V ≤ VCC < 2.5V, CL = 100 pF
A10	TCZ	Data output disable time	—	100 200	ns ns	4.5V ≤ VCC < 5.5V, **(Note 1)** 1.8V ≤ VCC < 4.5V, **(Note 1)**
A11	TSV	Status valid time	—	200 300 500	ns ns ns	4.5V ≤ VCC < 5.5V, CL = 100 pF 2.5V ≤ VCC < 4.5V, CL = 100 pF 1.8V ≤ VCC < 2.5V, CL = 100 pF
A12	TWC	Program cycle time	—	6	ms	ERASE/WRITE mode (AA and LC versions)
A13	TWC		—	2	ms	ERASE/WRITE mode (93C versions)
A14	TEC		—	6	ms	ERAL mode, 4.5V ≤ VCC ≤ 5.5V
A15	TWL		—	15	ms	WRAL mode, 4.5V ≤ VCC ≤ 5.5V
A16	—	Endurance	1M	—	cycles	25°C, VCC = 5.0V, **(Note 2)**

Note 1: This parameter is periodically sampled and not 100% tested.

2: This application is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which may be obtained on www.microchip.com.

FIGURE 1-1: SYNCHRONOUS DATA TIMING



Note: TSV is relative to CS.

TABLE 1-1: INSTRUCTION SET FOR X 16 ORGANIZATION (93XX86B OR 93XX86C WITH ORG = 1)

Instruction	SB	Opcode	Address										Data In	Data Out	Req. CLK Cycles
READ	1	10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	D15 – D0	29
EWEN	1	00	1	1	X	X	X	X	X	X	X	X	—	HIGH-Z	13
ERASE	1	11	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	(RDY/$\overline{\text{BSY}}$)	13
ERAL	1	00	1	0	X	X	X	X	X	X	X	X	—	(RDY/$\overline{\text{BSY}}$)	13
WRITE	1	01	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	D15 – D0	(RDY/$\overline{\text{BSY}}$)	29
WRAL	1	00	0	1	X	X	X	X	X	X	X	X	D15 – D0	(RDY/$\overline{\text{BSY}}$)	29
EWDS	1	00	0	0	X	X	X	X	X	X	X	X	—	HIGH-Z	13

TABLE 1-2: INSTRUCTION SET FOR X 8 ORGANIZATION (93XX86A OR 93XX86C WITH ORG = 0)

Instruction	SB	Opcode	Address											Data In	Data Out	Req. CLK Cycles
READ	1	10	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	D7 – D0	22
EWEN	1	00	1	1	X	X	X	X	X	X	X	X	X	—	HIGH-Z	14
ERASE	1	11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	—	(RDY/$\overline{\text{BSY}}$)	14
ERAL	1	00	1	0	X	X	X	X	X	X	X	X	X	—	(RDY/$\overline{\text{BSY}}$)	14
WRITE	1	01	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	D7 – D0	(RDY/$\overline{\text{BSY}}$)	22
WRAL	1	00	0	1	X	X	X	X	X	X	X	X	X	D7 – D0	(RDY/$\overline{\text{BSY}}$)	22
EWDS	1	00	0	0	X	X	X	X	X	X	X	X	X	—	HIGH-Z	14

2.0 FUNCTIONAL DESCRIPTION

When the ORG* pin is connected to VCC, the (x16) organization is selected. When it is connected to ground, the (x8) organization is selected. Instructions, addresses and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normally held in a HIGH-Z state except when reading data from the device, or when checking the READY/BUSY status during a programming operation. The READY/BUSY status can be verified during an Erase/Write operation by polling the DO pin; DO low indicates that programming is still in progress, while DO high indicates the device is ready. DO will enter the HIGH-Z state on the falling edge of CS.

2.1 START Condition

The START bit is detected by the device if CS and DI are both high with respect to the positive edge of CLK for the first time.

Before a START condition is detected, CS, CLK, and DI may change in any combination (except to that of a START condition), without resulting in any device operation (READ, WRITE, ERASE, EWEN, EWDS, ERAL, or WRAL). As soon as CS is high, the device is no longer in Standby mode.

An instruction following a START condition will only be executed if the required opcode, address and data bits for any particular instruction are clocked in.

2.2 Data In/Data Out (DI/DO)

It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a “bus conflict” to occur during the “dummy zero” that precedes the read operation, if A0 is a logic high level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A0. The higher the current sourcing capability of A0, the higher the voltage at the Data Out pin. In order to limit this current, a resistor should be connected between DI and DO.

2.3 Data Protection

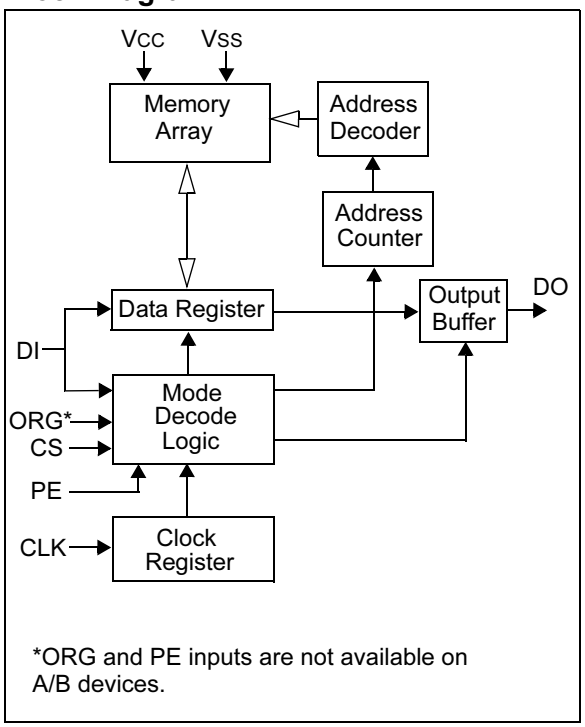
All modes of operation are inhibited when VCC is below a typical voltage of 1.5V for ‘93AA’ and ‘93LC’ devices or 3.8V for ‘93C’ devices.

The EWEN and EWDS commands give additional protection against accidentally programming during normal operation.

Note: For added protection, an EWDS command should be performed after every write operation.

After power-up, the device is automatically in the EWDS mode. Therefore, an EWEN instruction must be performed before the initial ERASE or WRITE instruction can be executed.

Block Diagram



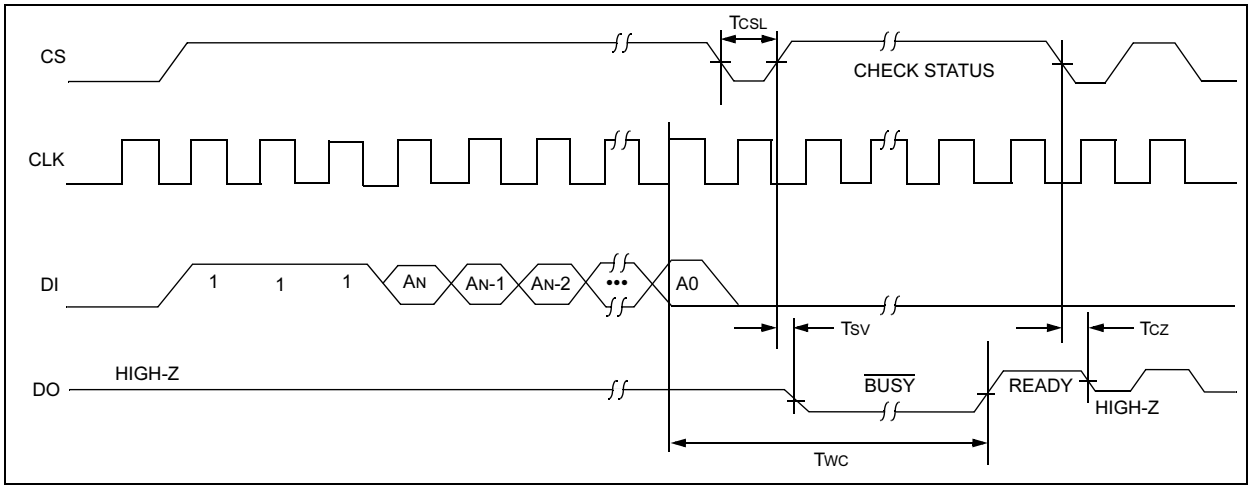
2.4 ERASE

The ERASE instruction forces all data bits of the specified address to the logical “1” state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle, except on ‘93C’ devices where the rising edge of CLK before the last address bit initiates the write cycle.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (T_{CSL}). DO at logical “0” indicates that programming is still in progress. DO at logical “1” indicates that the register at the specified address has been erased and the device is ready for another instruction.

Note: Issuing a START bit and then taking CS low will clear the READY/$\overline{\text{BUSY}}$ status from DO.

FIGURE 2-1: ERASE TIMING



2.5 ERASE ALL (ERAL)

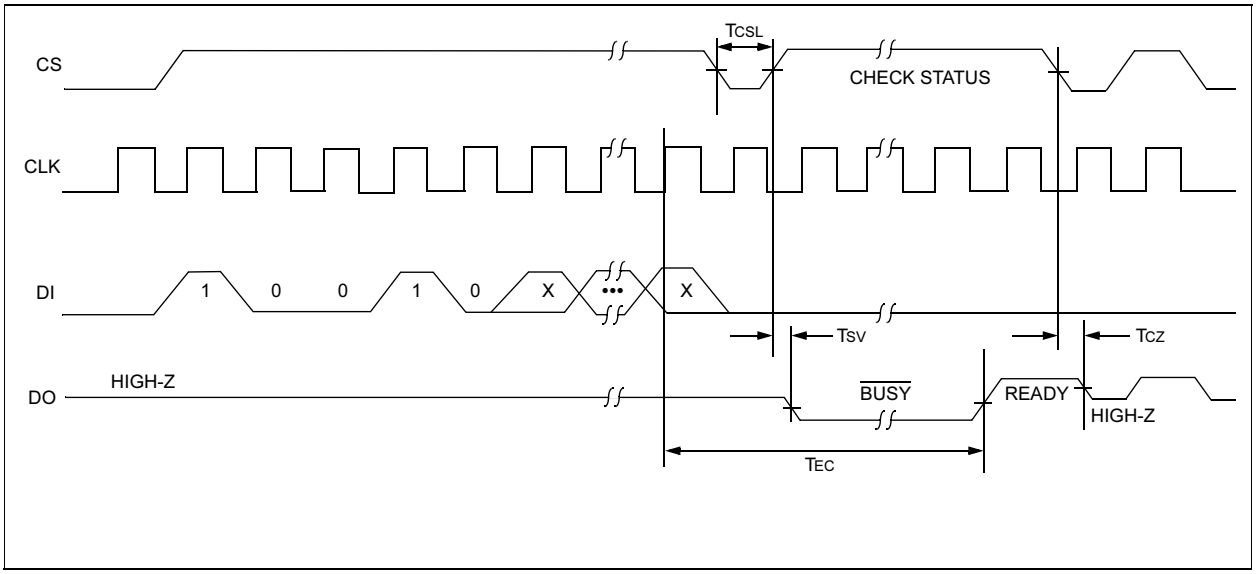
The Erase All (ERAL) instruction will erase the entire memory array to the logical “1” state. The ERAL cycle is identical to the ERASE cycle, except for the different opcode. The ERAL cycle is completely self-timed and commences at the falling edge of the CS, except on ‘93C’ devices where the rising edge of CLK before the last data bit initiates the write cycle. Clocking of the CLK pin is not necessary after the device has entered the ERAL cycle.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device, if CS is brought high after a minimum of 250 ns low (T_{CSL}).

Note: Issuing a START bit and then taking CS low will clear the READY/$\overline{\text{BUSY}}$ status from DO.

V_{CC} must be ≥ 4.5V for proper operation of ERAL.

FIGURE 2-2: ERAL TIMING



2.6 ERASE/WRITE DISABLE And ENABLE (EWDS/EWEN)

The 93XX86A/B/C powers up in the ERASE/WRITE Disable (EWDS) state. All programming modes must be preceded by an ERASE/WRITE Enable (EWEN) instruction. Once the EWEN instruction is executed, programming remains enabled until an EWDS instruction is executed or VCC is removed from the device. To protect against accidental data disturbance, the EWDS instruction can be used to disable all ERASE/WRITE functions and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

FIGURE 2-3: EWDS TIMING

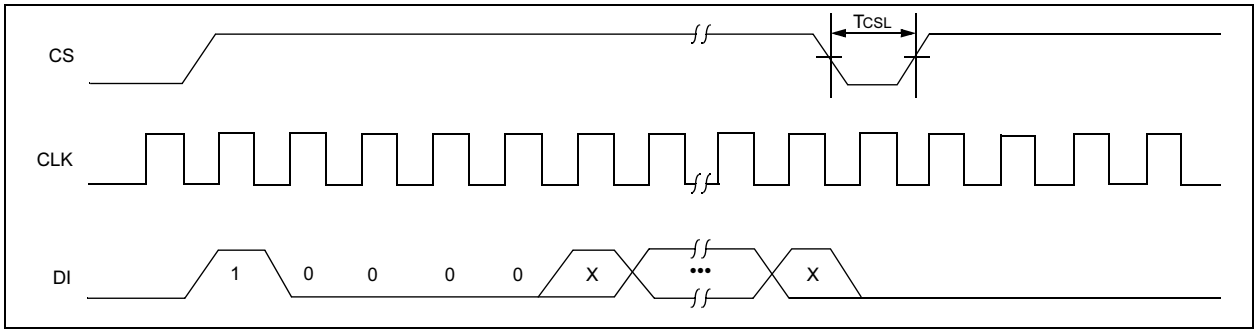
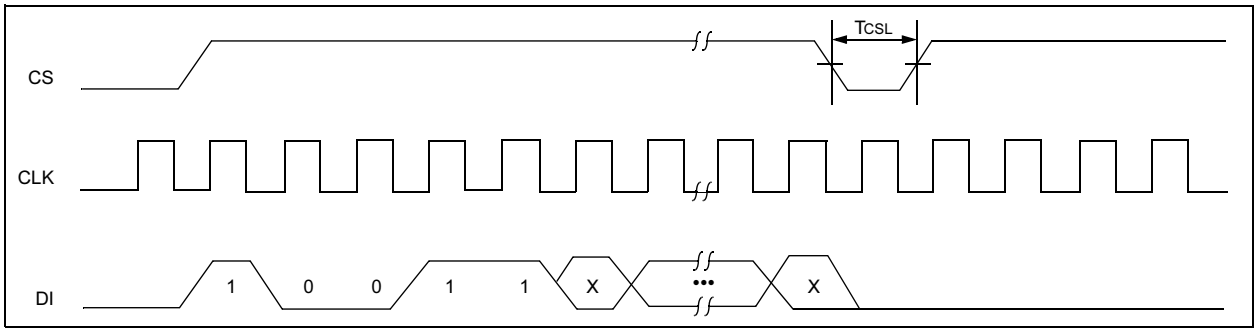


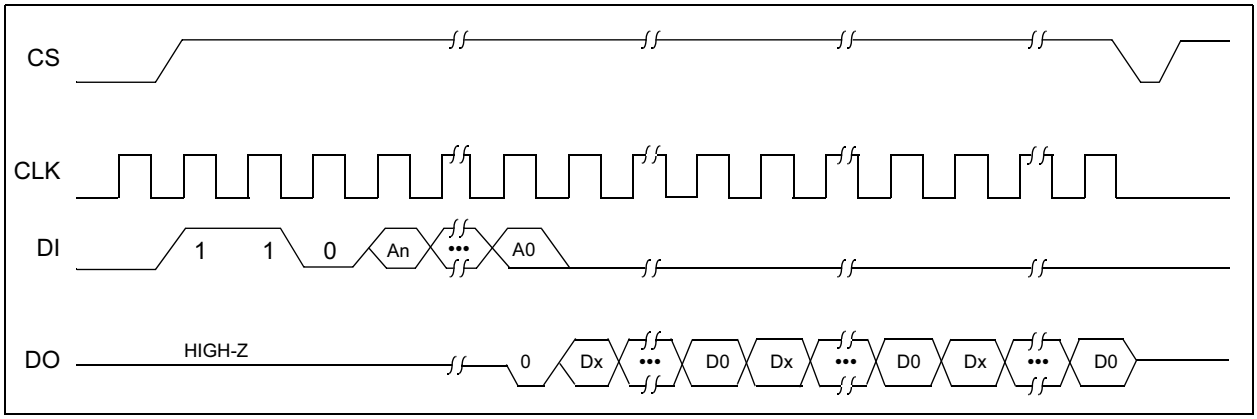
FIGURE 2-4: EWEN TIMING



2.7 READ

The READ instruction outputs the serial data of the addressed memory location on the DO pin. A dummy zero bit precedes the 8-bit (If ORG pin is low or A-Version devices) or 16-bit (If ORG pin is high or B-version devices) output string. The output data bits will toggle on the rising edge of the CLK and are stable after the specified time delay (TPD). Sequential read is possible when CS is held high. The memory data will automatically cycle to the next register and output sequentially.

FIGURE 2-5: READ TIMING



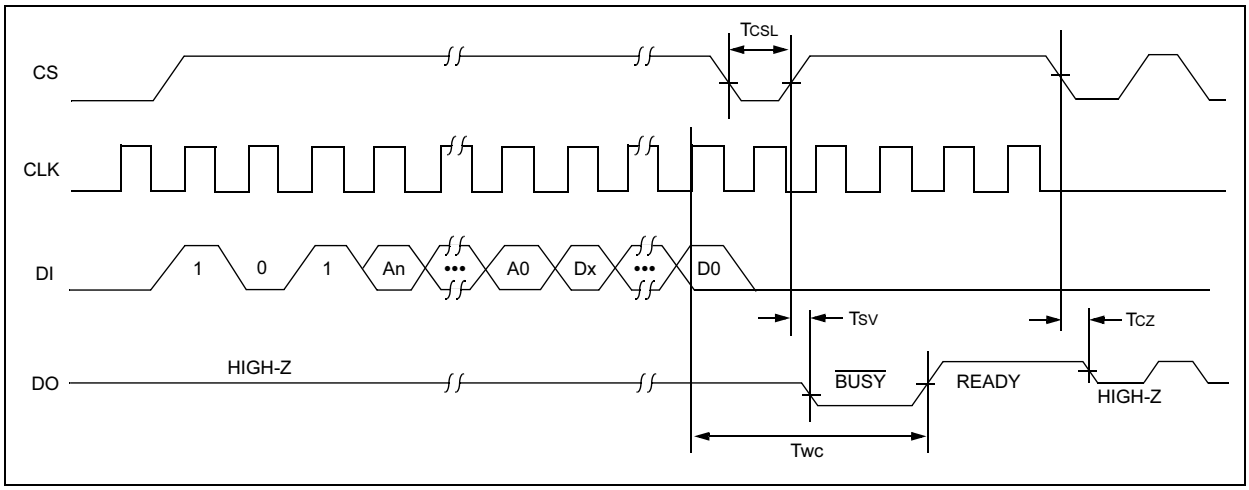
2.8 WRITE

The `WRITE` instruction is followed by 8 bits (If ORG is low or A-version devices) or 16 bits (If ORG pin is high or B-version devices) of data which are written into the specified address. For 93AA86A/B/C and 93LC86A/B/C devices, after the last data bit is clocked into DI, the falling edge of CS initiates the self-timed auto-erase and programming cycle. For 93C86A/B/C devices, the self-timed auto-erase and programming cycle is initiated by the rising edge of CLK on the last data bit.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device, if CS is brought high after a minimum of 250 ns low (T_{CSL}). DO at logical “0” indicates that programming is still in progress. DO at logical “1” indicates that the register at the specified address has been written with the data specified and the device is ready for another instruction.

Note: Issuing a START bit and then taking CS low will clear the READY/$\overline{\text{BUSY}}$ status from DO.

FIGURE 2-6: WRITE TIMING



2.9 WRITE ALL (WRAL)

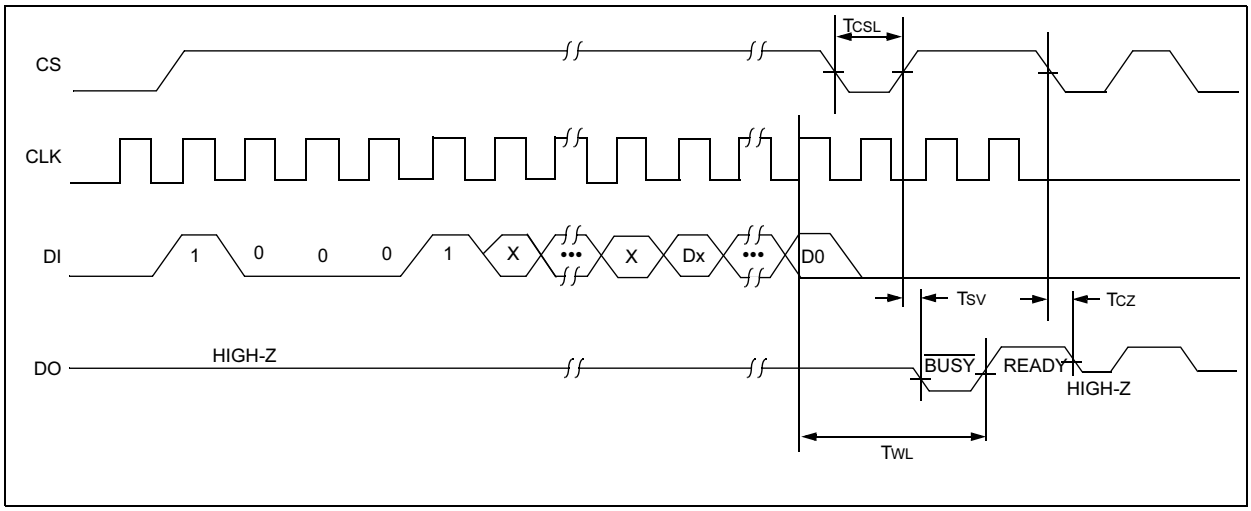
The Write All (WRAL) instruction will write the entire memory array with the data specified in the command. For 93AA86A/B/C and 93LC86A/B/C devices, after the last data bit is clocked into DI, the falling edge of CS initiates the self-timed auto-erase and programming cycle. For 93C86A/B/C devices, the self-timed auto-erase and programming cycle is initiated by the rising edge of CLK on the last data bit. Clocking of the CLK pin is not necessary after the device has entered the WRAL cycle. The WRAL command does include an automatic ERAL cycle for the device. Therefore, the WRAL instruction does not require an ERAL instruction but the chip must be in the EWEN status.

The DO pin indicates the READY/$\overline{\text{BUSY}}$ status of the device if CS is brought high after a minimum of 250 ns low (T_{CSL}).

Note: Issuing a START bit and then taking CS low will clear the READY/$\overline{\text{BUSY}}$ status from DO.

V_{CC} must be ≥ 4.5V for proper operation of WRAL.

FIGURE 2-7: WRAL TIMING



3.0 PIN DESCRIPTIONS

TABLE 3-1: PIN DESCRIPTIONS

Name	SOIC/PDIP/ MSOP/TSSOP	SOT-23	Function
CS	1	5	Chip Select
CLK	2	4	Serial Clock
DI	3	3	Data In
DO	4	1	Data Out
VSS	5	2	Ground
ORG	6	N/A	Organization / 93XX86C
PE	7	N/A	Program Enable
VCC	8	6	Power Supply

3.1 Chip Select (CS)

A high level selects the device; a low level deselects the device and forces it into Standby mode. However, a programming cycle which is already in progress will be completed, regardless of the Chip Select (CS) input signal. If CS is brought low during a program cycle, the device will go into Standby mode as soon as the programming cycle is completed.

CS must be low for 250 ns minimum (TCSL) between consecutive instructions. If CS is low, the internal control logic is held in a RESET status.

3.2 Serial Clock (CLK)

The Serial Clock is used to synchronize the communication between a master device and the 93XX series device. Opcodes, address and data bits are clocked in on the positive edge of CLK. Data bits are also clocked out on the positive edge of CLK.

CLK can be stopped anywhere in the transmission sequence (at high or low level) and can be continued anytime with respect to clock high time (TCKH) and clock low time (TCKL). This gives the controlling master freedom in preparing opcode, address and data.

CLK is a “Don't Care” if CS is low (device deselected). If CS is high, but the START condition has not been detected (DI = 0), any number of clock cycles can be received by the device without changing its status (i.e., waiting for a START condition).

CLK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycle.

After detection of a START condition the specified number of clock cycles (respectively low-to-high transitions of CLK) must be provided. These clock cycles are required to clock in all required opcode, address and data bits before an instruction is executed. CLK and DI then become don't care inputs waiting for a new START condition to be detected.

3.3 Data In (DI)

Data In (DI) is used to clock in a START bit, opcode, address and data synchronously with the CLK input.

3.4 Data Out (DO)

Data Out (DO) is used in the Read mode to output data synchronously with the CLK input (TPD after the positive edge of CLK).

This pin also provides READY/$\overline{\text{BUSY}}$ status information during ERASE and WRITE cycles. READY/$\overline{\text{BUSY}}$ status information is available on the DO pin if CS is brought high after being low for minimum chip select low time (TCSL) and an erase or write operation has been initiated.

The status signal is not available on DO, if CS is held low during the entire ERASE or WRITE cycle. In this case, DO is in the HIGH-Z mode. If status is checked after the ERASE/WRITE cycle, the data line will be high to indicate the device is ready.

Note: Issuing a START bit and then taking CS low will clear the READY/$\overline{\text{BUSY}}$ status from DO.

3.5 Organization (ORG)

When the ORG pin is connected to VCC or Logic HI, the (x16) memory organization is selected. When the ORG pin is tied to VSS or Logic LO, the (x8) memory organization is selected. For proper operation, ORG must be tied to a valid logic level.

93XX86A devices are always x8 organization and 93XX86B devices are always x16 organization.

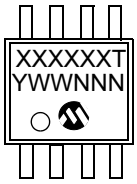
3.6 Program Enable (PE)

This pin allows the user to enable or disable the ability to write data to the memory array. If the PE pin is tied to VCC, the device can be programmed. If the PE pin is tied to VSS, programming will be inhibited. PE is not available on 93XX86A or 93XX86B. On those devices, programming is always enabled. This pin cannot be floated, it must be tied to VCC or VSS.

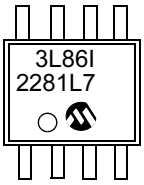
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

8-Lead MSOP (150 mil)

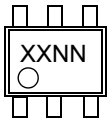


Example:

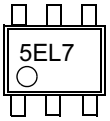


MSOP 1st Line Marking Codes		
Device	std mark	Pb-free mark
93AA86C	3A86CT	GA86CT
93LC86C	3L86CT	GL86CT
93C86C	3C86CT	GC86CT
T = blank for commercial, “I” for Industrial, “E” for Extended.		

6-Lead SOT-23

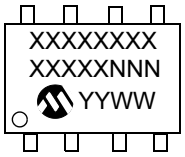


Example:

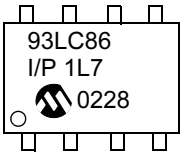


SOT23 Marking Codes		
Device	I-temp	E-temp
93AA86A	5BNN	–
93AA86B	5LNN	–
93LC86A	5ENN	5FNN
93LC86B	5PNN	5RNN
93C86A	5HNN	5JNN
93C86B	5TNN	5UNN
Pb-free topside mark is same; Pb-free noted only on carton label.		

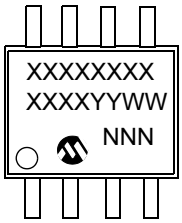
8-Lead PDIP



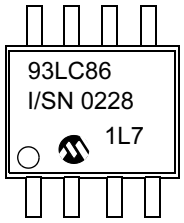
Example:



8-Lead SOIC

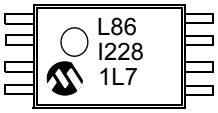


Example:



8-Lead TSSOP

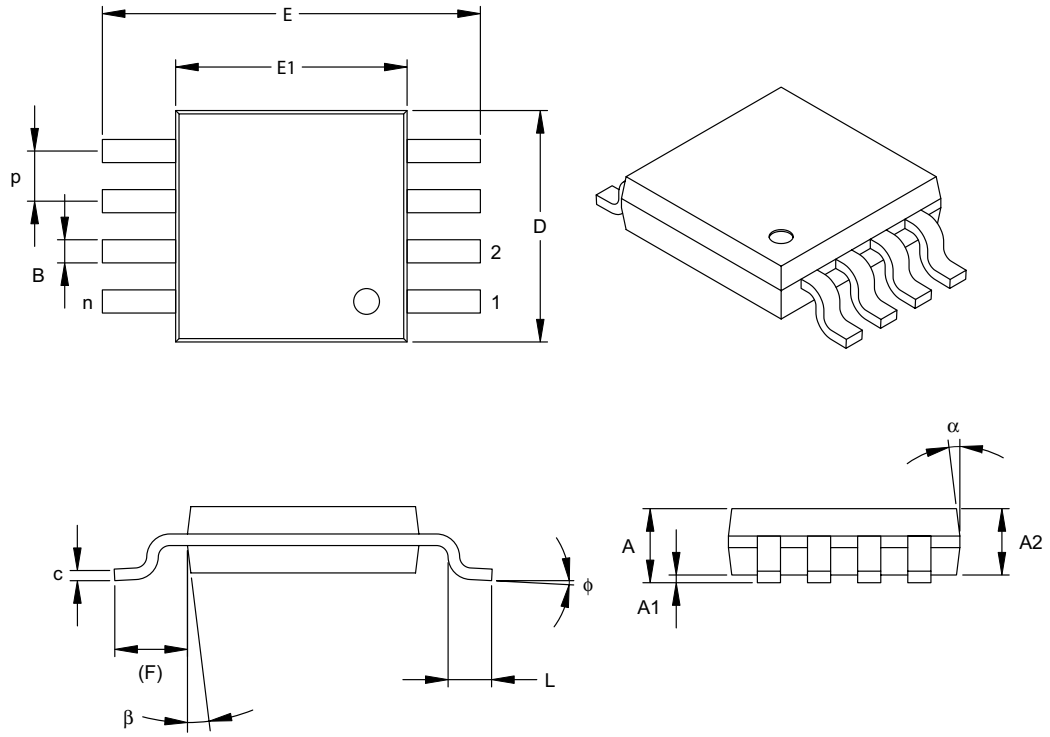
Example:



TSSOP 1st Line Marking Codes		
Device	std mark	Pb-free mark
93AA86C	A86C	GAEC
93LC86C	L86C	GLEC
93C86C	C86C	GCEC
Temperature grade is marked on line 2.		

Legend:	XX...X	Part number
	T	Temperature
	Blank	Commercial
	I	Industrial
	E	Extended
	YY	Year code (last 2 digits of calendar year) except TSSOP and MSOP which use only the last 1 digit
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
Note:	Custom marking available.	

8-Lead Plastic Micro Small Outline Package (MS) (MSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026 BSC			0.65 BSC	
Overall Height	A	-	-	.043	-	-	1.10
Molded Package Thickness	A2	.030	.033	.037	0.75	0.85	0.95
Standoff	A1	.000	-	.006	0.00	-	0.15
Overall Width	E		.193 TYP.			4.90 BSC	
Molded Package Width	E1		.118 BSC			3.00 BSC	
Overall Length	D		.118 BSC			3.00 BSC	
Foot Length	L	.016	.024	.031	0.40	0.60	0.80
Footprint (Reference)	F		.037 REF			0.95 REF	
Foot Angle	φ	0°	-	8°	0°	-	8°
Lead Thickness	c	.003	.006	.009	0.08	-	0.23
Lead Width	B	.009	.012	.016	0.22	-	0.40
Mold Draft Angle Top	α	5°	-	15°	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°	5°	-	15°

*Controlling Parameter

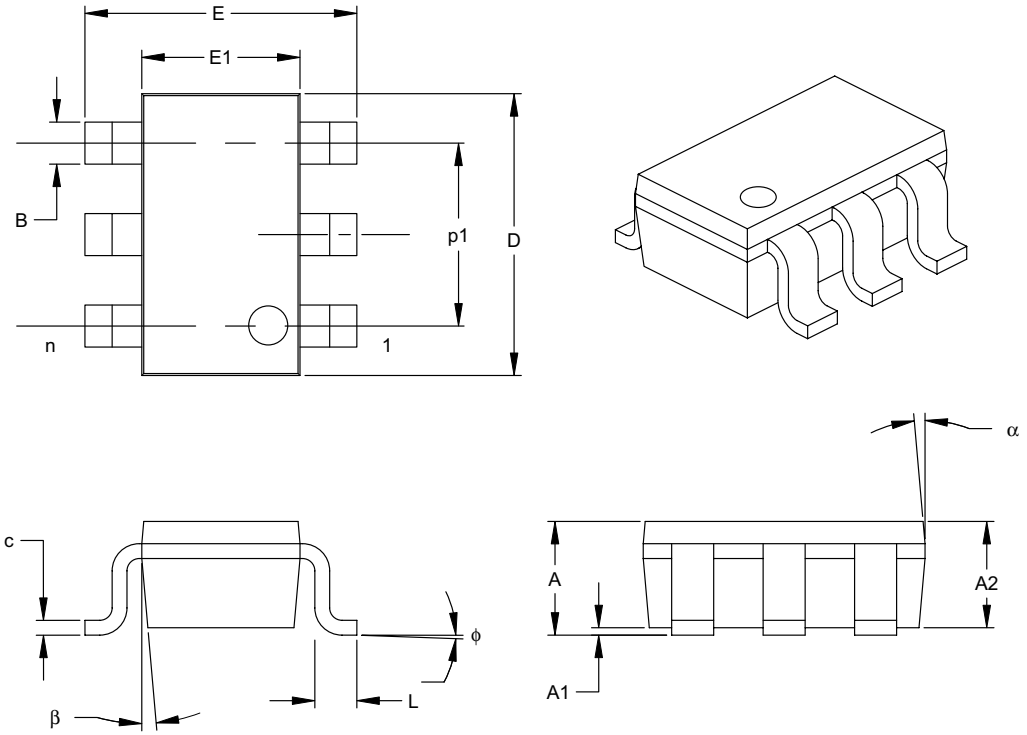
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-187

Drawing No. C04-111

6-Lead Plastic Small Outline Transistor (CH) (SOT-23)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		6			6	
Pitch	p		.038			0.95	
Outside lead pitch (basic)	p1		.075			1.90	
Overall Height	A	.035	.046	.057	0.90	1.18	1.45
Molded Package Thickness	A2	.035	.043	.051	0.90	1.10	1.30
Standoff	A1	.000	.003	.006	0.00	0.08	0.15
Overall Width	E	.102	.110	.118	2.60	2.80	3.00
Molded Package Width	E1	.059	.064	.069	1.50	1.63	1.75
Overall Length	D	.110	.116	.122	2.80	2.95	3.10
Foot Length	L	.014	.018	.022	0.35	0.45	0.55
Foot Angle	ϕ	0	5	10	0	5	10
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.014	.017	.020	0.35	0.43	0.50
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

*Controlling Parameter

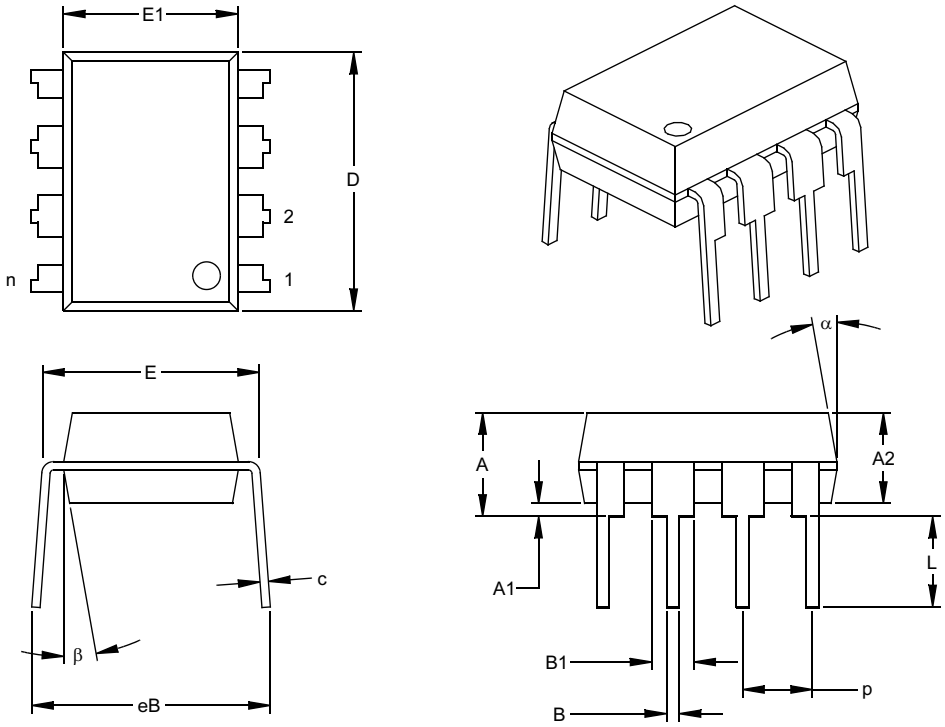
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

JEITA (formerly EIAJ) equivalent: SC-74A

Drawing No. C04-120

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

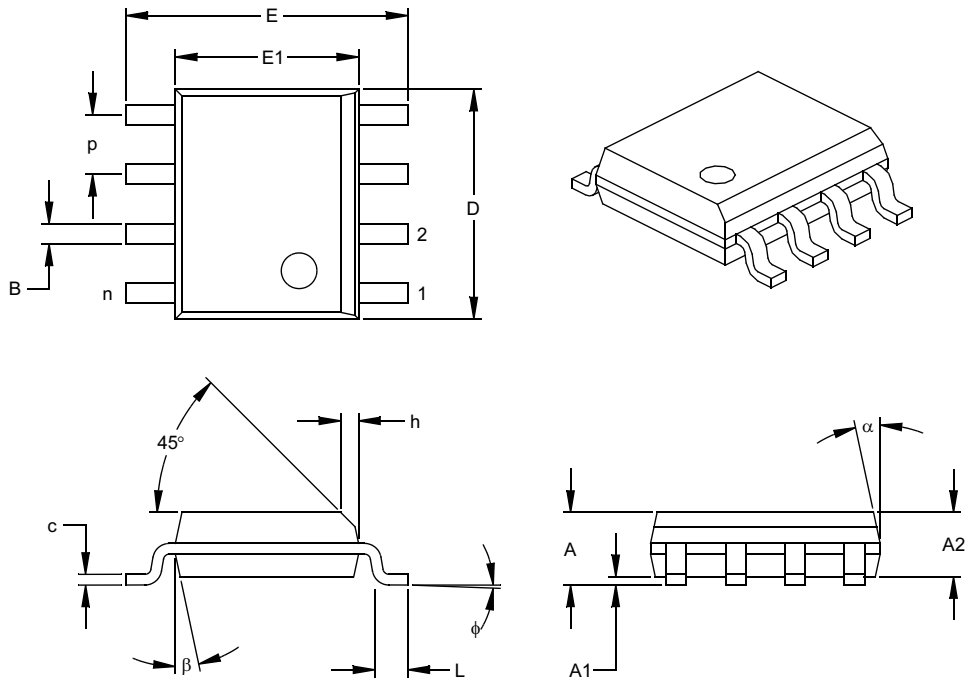


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)

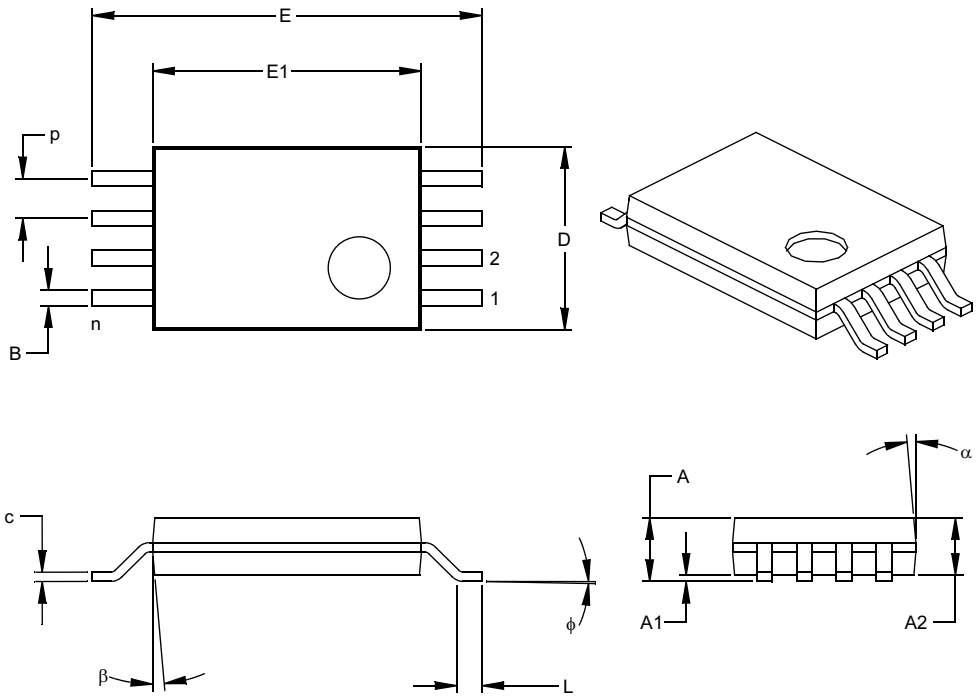


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005” (0.127mm) per side.
JEDEC Equivalent: MO-153
Drawing No. C04-086

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_____

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_____

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To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	X	/XX	X
Device	Tape & Reel	Temperature Range	Package	Lead Finish

Device	93AA86A:	16K 1.8V Microwire Serial EEPROM (x8)	
	93AA86B:	16K 1.8V Microwire Serial EEPROM (x16)	
	93AA86C:	16K 1.8V Microwire Serial EEPROM w/ORG	
	93LC86A:	16K 2.5V Microwire Serial EEPROM (x8)	
	93LC86B:	16K 2.5V Microwire Serial EEPROM (x16)	
	93LC86C:	16K 2.5V Microwire Serial EEPROM w/ORG	
	93C86A:	16K 5.0V Microwire Serial EEPROM (x8)	
	93C86B:	16K 5.0V Microwire Serial EEPROM (x16)	
	93C86C:	16K 5.0V Microwire Serial EEPROM w/ORG	
Tape & Reel:	Blank	=	Standard packaging
	T	=	Tape & Reel
Temperature Range	I	=	-40°C to +85°C
	E	=	-40°C to +125°C
Package	MS	=	Plastic MSOP (Micro Small outline, 8-lead)
	OT	=	SOT-23, 6-lead (Tape & Reel only)
	P	=	Plastic DIP (300 mil body), 8-lead
	SN	=	Plastic SOIC (150 mil body), 8-lead
	ST	=	TSSOP, 8-lead
Lead Finish:	Blank	=	Standard 63% / 37% SnPb
	G	=	Pb-free (Matte Tin - Pure Sn)

Examples:

a) 93AA86C-I/MS: 16K, 2048x8 or 1024x16 Serial EEPROM, MSOP package, 1.8V
b) 93AA86AT-I/OT: 16K, 2048x8 Serial EEPROM, SOT-23 package, tape and reel, 1.8V
c) 93AA86CT-I/MS: 16K, 2048x8 or 1024x16 Serial EEPROM, MSOP package, tape and reel, 1.8V

a) 93LC86C-I/MS: 16K, 2048x8, 1024x16 Serial EEPROM, MSOP package, 2.5V
b) 93LC86BT-I/OT: 16K, 1024x16 Serial EEPROM, SOT-23 package, tape and reel, 2.5V
c) 93LC86CT-I/SNG: 16K, 2048x8 or 1024x16 Serial EEPROM, SOIC package, Industrial temperature, tape and reel, Pb-free finish, 2.5V

a) 93C86C-I/MS: 16K, 2048x8 or 1024x16 Serial EEPROM, MSOP package, 5.0V
b) 93C86AT-I/OT: 16K, 2048x8 Serial EEPROM, SOT-23 package, tape and reel, 5.0V

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