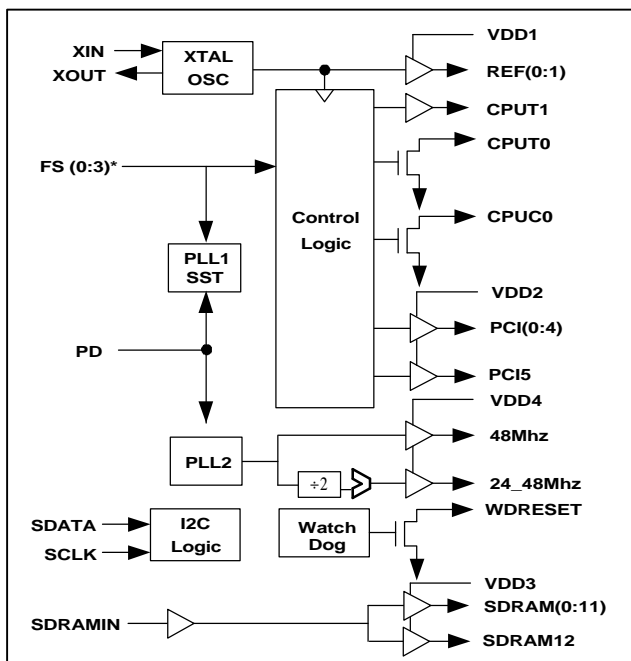


**Motherboard Clock Generator for AMD - K7**

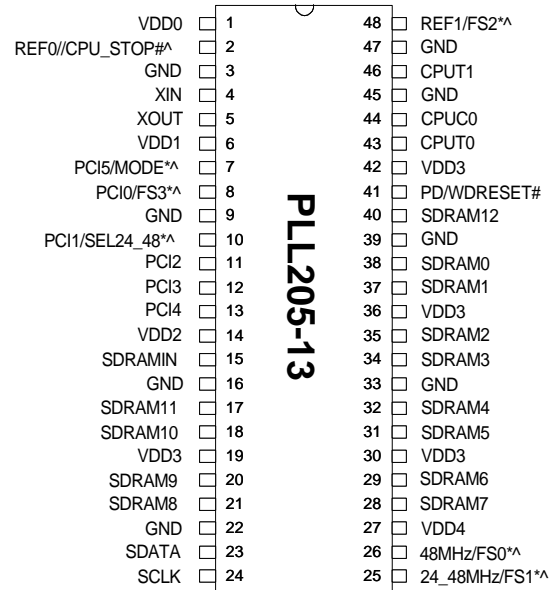
**FEATURES**

- Generates all clock frequencies for VIA K7 chip sets requiring multiple CPU clocks and high speed SDRAM buffers.
- Support one pair of differential CPU clocks, one 3.3V push-pull CPU, 6 PCI and 13 high-speed SDRAM buffers for 3-DIMM applications.
- One 24\_48MHz clock and one 48MHz clock.
- Two 14.318MHz reference clocks.
- Power management control to stop CPU, and Power down Mode from I2C programming.
- Support 2-wire I2C serial bus interface with built-in Vendor ID, Device ID and Revision ID.
- Single byte micro-step linear Frequency Programming via I2C with Glitch free smooth switching.
- Enhanced CPU and SDRAM output Drive selected by I2C.
- Built-in programmable watchdog timer up to 63 seconds with 1-second interval. It will generate a LOW reset output when timer expired.
- Spread Spectrum  $\pm 0.25\%$  center spread, 0 to -0.5% down spread.
- Available in 300 mil 48 pin SSOP.

**BLOCK DIAGRAM**



**PIN CONFIGURATION**



Note: ^: Pull up, #: Active Low  
\*: Bi-directional latched at power-up

**I/O MODE CONFIGURATION**

MODE (Pin 7)	PIN 2
1 (OUTPUT)	REF0
0 (INPUT)	CPU_STOP

**POWER GROUP**

- VDD0: PLL CORE
- VDD1: REF(0:1), XIN, XOUT
- VDD2: PCI(0:5)
- VDD3: SDRAM(0:12)
- VDD4: 48MHz, 24\_48MHz

**KEY SPECIFICATIONS**

- CPU Cycle to Cycle jitter: 250ps.
- PCI to PCI output skew: 500ps.
- CPU to CPU output skew:  $\pm 175$ ps
- SDRAM to SDRAM output skew: 250ps.
- CPU to PCI skew (CPU leads): 0 ~ 3 ns.

**Motherboard Clock Generator for AMD - K7**

**PIN DESCRIPTIONS**

Name	Number	Type	Description
VDD0	1	P	Power supply for PLL CORE.
VDD1	6	P	Power supply for REF0, REF1, and crystal oscillator.
VDD2	14	P	Power supply for PCI (0:5).
VDD3	19,30,36,42	P	Power supply for SDRAM (0:12).
VDD4	27	P	Power supply for 24_48MHz and 48MHz.
GND	3,9,16,22, 33,39,45,47	P	Ground.
XIN	4	I	14.318MHz crystal input that has internal loads cap (36pF) and feedback resistor from XOUT.
XOUT	5	O	14.318MHz crystal output. It has internal load cap (36pF).
REF0//CPU_STOP	2	B	Multiplexed pin controlled by MODE signal. When CPU_STOP is low, it will halt CPUT (0:1), CPUC0 and SDRAM (0:11) outputs. In output mode, this pin will generate buffered reference clock output.
PCI5/MODE	7	B	At power-up, MODE function will be activated. When MODE is Low, Pin 2 is input for CPU_STOP. When high, Pin 2 is output for REF0. After input data latched, this pin will generate PCI bus clock.
PCI0/FS3	8	B	At power-up, this pin is input pin and will determine CPU clock frequency. After input sampling, this pin will generate output clocks. FS3 has internal pull up (high by default).
PCI1/SEL24_48	10	B	At power-up, this pin will select 24MHz (when high) or 48MHz (when low) for pin25 output. After input sampling, this pin is PCI output. It has internal pull up resistor.
PCI(2:4)	11,12,13	O	PCI clock outputs.
SDRAMIN	15	I	Buffer input pin: The signal provided to this input pin is buffered to 13 SDRAM outputs.
SDRAM(0:11)	17,18,20,21, 28,29,31,32, 34,35,37,38	O	SDRAM clock outputs, Fan-out Buffer outputs from SDRAMIN pin.
SDATA	23	B	Serial data inputs for serial interface port.
SCLK	24	I	
24_48MHz/FS1, 24MHz/FS0	25,26	B	At power-up, these pins are input pins and will determine the CPU clock frequency. FS0, FS1 have internal pull up (high by default).
SDRAM12	40	O	When CPU_STOP is low, this pin is still free running. When the power down is low, this SDRAM will be stopped.
PD/WDRESET	41	B	Power Down Control input. When low, Power Down will disable all clock outputs including internal VCO and crystal clock. The enable of the watchdog timer masks the PD action.
CPUT0	43	O	True clock of differential pair open-drain CPU output.
CPUC0	44	O	Complementary clocks of differential pair open-drain CPU outputs.
CPUT1	46	O	True clock of push-pull CPU output.
REF1/FS2	48	B	Buffered reference clock output after input data latched during power-up.

**Motherboard Clock Generator for AMD - K7**

**POWER MANAGEMENT**

CPU_STOP	CPUC0	CPUT (0:1)	SDRAM (0:11)	SDRAM12	CRYSTAL	VCO
0	Stopped Low	Stopped Low	Stopped Low	Running	Running	Running
1	Running	Running	Running	Running	Running	Running

**FREQUENCY (MHz) SELECTION TABLE**

I2C Byte0 Bit2	FS3	FS2	FS1	FS0	CPU	PCI	Spread Spectrum Modulation
0 default	0	0	0	0	124.0	41.3	±0.25%
	0	0	0	1	75.0	37.5	±0.25%
	0	0	1	0	83.3	41.7	±0.25%
	0	0	1	1	66.8	33.4	±0.25%
	0	1	0	0	103.0	34.3	±0.25%
	0	1	0	1	112.0	37.3	±0.25%
	0	1	1	0	133.3	44.4	±0.25%
	0	1	1	1	100.0	33.3	±0.25%
	1	0	0	0	120.0	40.0	±0.25%
	1	0	0	1	115.0	38.3	±0.25%
	1	0	1	0	110.0	36.7	±0.25%
	1	0	1	1	105.0	35.0	±0.25%
	1	1	0	0	140.0	35.0	±0.25%
	1	1	0	1	150.0	37.5	±0.25%
	1	1	1	0	124.0	31.0	±0.25%
1	1	1	1	133.3	33.3	±0.25%	
1	0	0	0	0	90.0	30.0	±0.25%
	0	0	0	1	92.5	30.8	±0.25%
	0	0	1	0	95.0	31.7	±0.25%
	0	0	1	1	97.5	32.5	±0.25%
	0	1	0	0	101.5	33.8	±0.25%
	0	1	0	1	127.0	42.3	±0.25%
	0	1	1	0	136.5	34.1	±0.25%
	0	1	1	1	100.0	33.3	0 to -0.5%
	1	0	0	0	120.0	40.0	0 to -0.5%
	1	0	0	1	117.5	39.2	±0.25%
	1	0	1	0	122.0	40.7	±0.25%
	1	0	1	1	107.5	35.8	±0.25%
	1	1	0	0	145.0	36.3	±0.25%
	1	1	0	1	155.0	38.7	±0.25%
	1	1	1	0	130.0	32.5	±0.25%
1	1	1	1	133.3	33.3	0 to -0.5%	

**Motherboard Clock Generator for AMD - K7**

**I2C BUS CONFIGURATION SETTING**

Address Assignment	A6	A5	A4	A3	A2	A1	A0	R/W
	1	1	0	1	0	0	1	-
Slave Receiver/Transmitter	Provides both slave write and readback functionality							
Data Transfer Rate	Standard mode at 100kbts/s							
Serial Bits Reading	The serial bits will be read or sent by the clock driver in the following order Byte 0 Bits 7, 6, 5, 4, 3, 2, 1, 0 Byte 1 Bits 7, 6, 5, 4, 3, 2, 1, 0 - Byte N Bits 7, 6, 5, 4, 3, 2, 1, 0							
Data Protocol	This serial protocol is designed to allow both blocks write and read from the controller. The bytes must be accessed in sequential order from lowest to highest byte. Each byte transferred must be followed by 1 acknowledge bit. A byte transferred without acknowledged bit will terminate the transfer. The write or read block both begins with the master sending a slave address and a write condition (0xD2) or a read condition (0xD3). Following the acknowledge of this address byte, in <b>Write Mode:</b> the <b>Command Byte</b> and <b>Byte Count Byte</b> must be sent by the master but ignored by the slave, in <b>Read Mode:</b> the <b>Byte Count Byte</b> will be read by the master then all other <b>Data Byte</b> . <b>Byte Count Byte</b> default at power-up is = (0x09).							

**I2C CONTROL REGISTERS**

**1. BYTE 0: Functional and Frequency Select Clock Register (1=Enable, 0=Disable)**

Bit	Pin#	Default	Description
Bit 7	8	0	FS3 ( see Frequency selection Table )
Bit 6	48	1	FS2 ( see Frequency selection Table )
Bit 5	25	0	FS1 ( see Frequency selection Table )
Bit 4	26	0	FS0 ( see Frequency selection Table )
Bit 3	-	0	Frequency selection control bit 1=Via I2C, 0=Via External jumper
Bit 2	-	0	FS4 ( see Frequency selection Table )
Bit 1	-	1	0=Normal 1=Spread Spectrum enable
Bit 0	-	0	0=Normal 1=Tristate Mode for all outputs

**Motherboard Clock Generator for AMD - K7**

**2. BYTE 1: CPU Clock Register (1=Enable, 0=Disable)**

Bit	Pin#	Default	Description
Bit 7	-	1	Reserved
Bit 6	17,18,20,21, 28,29,31,32, 34,35,37,38	1	High Strength SDRAM Select ( 1=Normal, 0= Enhanced by 25% )
Bit 5	46	1	Enhanced CPUT1 Drive Select ( 1=Normal, 0=Enhanced by 25% )
Bit 4	43,44	1	Enhanced CPUT0, CPUC0 Drive Select ( 1=Normal, 0=Enhanced by 25% )
Bit 3	40	1	SDRAM12 ( Active/Inactive )
Bit 2	-	1	Reserved
Bit 1	43,44	1	CPUT0, CPUC0 ( Active/Inactive )
Bit 0	46	1	CPUT1 ( Active/Inactive )

**3. BYTE 2: PCI Clock Register (1=Enable, 0=Disable)**

Bit	Pin#	Default	Description
Bit 7	-	1	Reserved
Bit 6	7	1	PCI5 ( Active/Inactive )
Bit 5	-	1	Reserved
Bit 4	13	1	PCI4 ( Active/Inactive )
Bit 3	12	1	PCI3 ( Active/Inactive )
Bit 2	11	1	PCI2 ( Active/Inactive )
Bit 1	10	1	PCI1 ( Active/Inactive )
Bit 0	8	1	PCI0 ( Active/Inactive )

**4. BYTE 3: SDRAM Clock Register (1=Enable, 0=Disable)**

Bit	Pin#	Default	Description
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	26	1	48MHz ( Active/Inactive )
Bit 4	25	1	24_48MHz ( Active/Inactive )
Bit 3	17	1	SDRAM11 ( Active/Inactive )
Bit 2	18	1	SDRAM10 ( Active/Inactive )
Bit 1	20	1	SDRAM9 ( Active/Inactive )
Bit 0	21	1	SDRAM8 ( Active/Inactive )

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**5. BYTE 4: SDRAM Clock Register (1=Enable, 0=Disable)**

Bit	Pin#	Default	Description
Bit 7	28	1	SDRAM7 ( Active/Inactive )
Bit 6	29	1	SDRAM6 ( Active/Inactive )
Bit 5	31	1	SDRAM5 ( Active/Inactive )
Bit 4	32	1	SDRAM4 ( Active/Inactive )
Bit 3	34	1	SDRAM3 ( Active/Inactive )
Bit 2	35	1	SDRAM2 ( Active/Inactive )
Bit 1	37	1	SDRAM1 ( Active/Inactive )
Bit 0	38	1	SDRAM0 ( Active/Inactive )

**6. BYTE 5: Peripheral Clock Register (1=Enable, 0=Disable)**

Bit	Pin#	Default	Description
Bit 7	-	X	Inverted Power-up latched FS3 value (Read only)
Bit 6	-	X	Inverted Power-up latched FS2 value (Read only)
Bit 5	-	X	Inverted Power-up latched FS1 value (Read only)
Bit 4	-	X	Inverted Power-up latched FS0 value (Read only)
Bit 3	-	1	Reserved
Bit 2	-	X	Inverted Power-up latched SEL24_48MHz value (Read only)
Bit 1	48	1	REF1 ( Active/Inactive )
Bit 0	2	1	REF0 ( Active/Inactive )

**7. BYTE 6: Fall-Back Frequency / Revision / Vendor ID Register (1=Enable, 0=Disable)**

Bit	Pin#	Default	Description
Bit 7	-	0	WDT Fall-back Frequency selection for FS4
Bit 6	-	0	WDT Fall-back Frequency selection for FS3
Bit 5	-	0	WDT Fall-back Frequency selection for FS2
Bit 4	-	0	WDT Fall-back Frequency selection for FS1
Bit 3	-	0	WDT Fall-back Frequency selection for FS0
Bit 2	-	0	Vendor ID Bit 2*
Bit 1	-	1	Vendor ID Bit 1*
Bit 0	-	1	Vendor ID Bit 0*

Note: \*: Default value at power-up

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**8. BYTE 7: Linear Programming (M) Register (1=Enable, 0=Disable)**

Bit	Pin#	Default	Description
Bit 7	-	0*	Linear programming sign bit ( 0 is + , 1 is - )
Bit 6	-	0*	Linear programming magnitude bit 6 (MSB)
Bit 5	-	0*	Linear programming magnitude bit 5
Bit 4	-	0*	Linear programming magnitude bit 4
Bit 3	-	0*	Linear programming magnitude bit 3
Bit 2	-	0*	Linear programming magnitude bit 2
Bit 1	-	0*	Linear programming magnitude bit 1
Bit 0	-	0*	Linear programming magnitude bit 0 (LSB)

**Note:** This register will be initialized to 0 following WATCHDOG RESET.

**9. BYTE 8: WATCHDOG TIMER / Device ID Register (1=Enable, 0=Disable)**

Bit	Pin#	Default	Description	
Bit 7	-	0	Watchdog Timer Enable Bit. 1=Enable, 0=Disable	
Bit 6	-	0	Device ID Bit 6*	
Bit 5	-	0	Watchdog Time Interval Bit 5 (MSB)	Device ID Bit 5*
Bit 4	-	0	Watchdog Time Interval Bit 4	Device ID Bit 4*
Bit 3	-	0	Watchdog Time Interval Bit 3	Device ID Bit 3*
Bit 2	-	0	Watchdog Time Interval Bit 2	Device ID Bit 2*
Bit 1	-	1	Watchdog Time Interval Bit 1	Device ID Bit 1*
Bit 0	-	1	Watchdog Time Interval Bit 0 (LSB)	Device ID Bit 0*

**Note:** \*: Default value at power-up

**Motherboard Clock Generator for AMD - K7**

**PROGRAMMING OF CPU FREQUENCY**

To simplify traditional loop counter setting, the PLL205-13 device incorporates SMART-BYTE technology with a single byte programming via I2C to better optimize clock jitter and spread spectrum performance. Detail of PLL205-13's dual mode frequency programming method is described below:

**1. ROM-table Frequency Programming:**

The pre-defined 32 frequencies found in Frequency table can be accessed either through 5 external jumpers or by setting internal I2C register in BYTE0.

**2. Micro-step Linear Frequency Programming:**

CPU Frequency can be programmed via I2C in fine and linear positive or negative stepping around selected CPU frequency in Frequency table. The highest step is either +127 or -127. Other bus frequencies will be changed proportionally with the rate that CPU frequency change. The formula is as follow:

$$F_{CPU} = F_{CPU.ROM-Table} \pm \alpha (=0.22) * M$$

- Where:
1. M is magnitude factor defined in I2C Byte 7.bit(0:6)
  2.  $\pm$  (sign bit) of M is defined in I2C Byte7.bit 7
  3.  $\alpha$  is a constant  
 $\alpha = 0.22$

**FREQUENCY PROGRAMMING EXAMPLE:**

**1. Procedures to program target CPU frequency to 139.0 Mhz:**

- A. Locate the closest CPU frequency from Frequency-ROM table: 136.5
- B.  $\alpha = 0.22$
- C. Solve M (Linear Magnitude factor) in integer:

$$\begin{aligned} M &= (F_{CPU} - F_{CPU-ROMTABLE}) / \alpha \\ &= (139 - 136.5) / 0.22 \\ &= 11 \end{aligned}$$

- D. Program I2C register:

7	6	5	4	3	2	1	0	Setting of I2C.BYTE0
0	1	1	0	1	1	0	0	

FS3	FS2	FS1	FS0	CTR	FS4	Setting of M = +11 in I2C.BYTE7	
7	6	5	4	3	2		1
0	0	0	0	1	0	1	1
Sign	M6	M5	M4	M3	M2	M1	M0

$$\begin{aligned} F_{CPU} &= 136.5 + (0.22) * 11 = 138.92 \quad ( \% \text{ of frequency increased} = 1.8 \% ) \\ F_{PCI} &= 34.1 * (1+1.8\%) = 34.7 \end{aligned}$$



**Motherboard Clock Generator for AMD - K7**

**BUILT-IN WATCHDOG TIMER (WDT)**

Watchdog timer is used to perform safe recovery if frequency switching causes system to enter into Hang-up state within a reasonable period of time (or Watchdog time interval). While disabled, the watchdog time interval can be programmed between 0 and 63 seconds with increment of 1 second by setting the value of I2C.Byte8.Bit(5:0). Once Enabled, WDT has to be disabled within a period that is shorter than the programmed watchdog interval; otherwise WDT will generate a 500ms low watchdog reset pulse to provoke a system reset. After system restarts, the PLL205-13 will start from predefined Fall-back Frequency (the value of I2C Byte6,bits(7:3)). If system for any reason fails again at Fall-back Frequency, the internal hardware will then generate a watchdog reset to restart the system from the value of external hardware jumper setting to ensure a safe recovery.

**Example usage:**

1. System power-up at CPU= 66.8MHz where external jumpers are used.
- 2A. Switch to target CPU=100.0MHz frequency with following I2C register setting:

7 6 5 4 3 2 1 0	0	0	1	1	1	0	0	0	FSEL	Setting in I2C.BYTE0	
	FS3	FS2	FS1	FS0	CTR	FS4					
7 6 5 4 3 2 1 0	0	0	0	0	0	0	0	0	M =0	Setting in I2C.BYTE7	
	Sign	M6	M5	M4	M3	M2	M1	M0			
7 6 5 4 3 2 1 0	1	0	0	0	1	1	1	1	WD-Timer = 15s	Setting in I2C.BYTE8	
	ENB	T5	T4	T3	T2	T1	T0				
7 6 5 4 3 2 1 0	0	0	0	1	1	0	0	0	FBSEL	Setting in I2C.BYTE6	
	FB4	FB3	FB2	FB1	FB0						

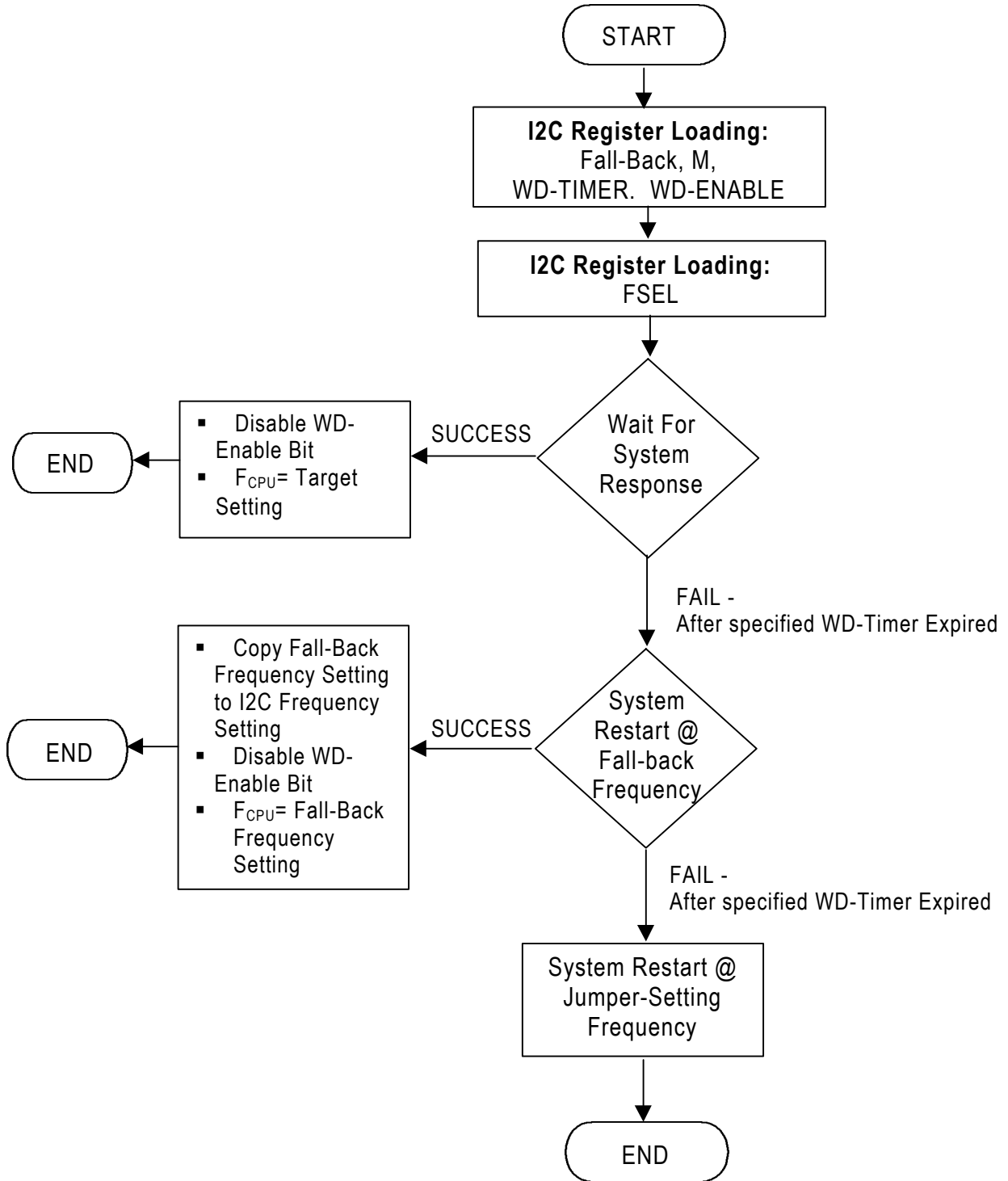
The fall-back frequency is set to the same location as that of FSEL since frequency switching between different timing groups will cause system to hang up. After WD timer expired or 15 seconds, the system will restart properly at target 100.0MHz if CPU is capable; otherwise WDT will perform another reset action to restart the system from 66.8 Mhz

- 2B. Switch to target CPU=78Mhz within the same timing Group

The fall-back frequency is recommended to set at the most safe and comfortable level to ensure a successful reboot such as 70 or 75.3 if system is unable to switch to 78Mhz.

**Motherboard Clock Generator for AMD - K7**

**WDT OPERATIONAL FLOW CHART**



**Motherboard Clock Generator for AMD - K7**

**ELECTRICAL SPECIFICATIONS**

**1. Absolute Maximum Ratings**

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	$V_{DD}$	$V_{SS}-0.5$	7	V
Input Voltage, dc	$V_I$	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Output Voltage, dc	$V_O$	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Storage Temperature	$T_S$	-65	150	°C
Ambient Operating Temperature	$T_A$	0	70	°C
Junction Temperature	$T_J$		115	°C
ESD Voltage			2	KV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

**2. AC/DC Electrical Specifications**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input High Voltage	$V_{IH}$		2.0		$V_{DD}+0.3$	V
Input Low Voltage	$V_{IL}$		$V_{SS}-0.3$		0.8	V
Input High Current	$I_{IH}$	$V_{IN} = V_{DD}$			5	$\mu A$
Input Low Current	$I_{IL1}$	Logic inputs without internal pull-up on SCLK, $V_{IN} = 0V$	-5			$\mu A$
Input Low Current	$I_{IL2}$	Logic inputs with internal pull-up resistors, $V_{IN} = 0V$	-200			$\mu A$
Power Down	PD				600	$\mu A$
Pull-up resistor	$R_{pu}$	Pin 2,7,8,10,25,26,48		120		kohm
Operating Supply Current	$I_{DD}$	$C_L=0$ pF @ 66MHz			180	mA
		$C_L=0$ pF @ 100MHz				
		$C_L=0$ pF @ 133MHz				
Input frequency	$F_I$	$V_{DD} = 3.3V$	12	14.318	16	MHz
Input Capacitance	$C_{IN}$	Logic Inputs			5	pF
	$C_{INX}$	XIN & XOUT pins	27		45	pF

**Motherboard Clock Generator for AMD - K7**
**2. Output Buffer Electrical Specifications**

 Unless otherwise stated, all power supplies = 3.3V±5%, and ambient temperature range T<sub>A</sub>= 0°C to 70°C

PARAMETERS	SYMBOL	OUTPUTS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Rise time	T <sub>OR</sub>	CPUT1	Measured @ 0.3V ~ 1.2V, C <sub>L</sub> =20pf, 3.3V±5%			2	ns
		CPU (Open Drain)	Measured @ 0.3V ~ 1.2V, C <sub>L</sub> =20pf, 3.3V±5%			0.9	
		REF(0:1)	Measured @ 0.4V ~ 2.4V, C <sub>L</sub> =20pf, 3.3V±5%			4	
		PCI(0:5)	Measured @ 0.4V ~ 2.4V, C <sub>L</sub> =30pf, 3.3V±5%			2	
		24_48MHz, 48MHz	Measured @ 0.4V ~ 2.4V, C <sub>L</sub> =20pf, 3.3V±5%			4	
Output Fall time	T <sub>OF</sub>	CPUT1	Measured @ 0.3V ~ 1.2V, C <sub>L</sub> =20pf, 3.3V±5%			2	ns
		CPU (Open Drain)	Measured @ 1.2V ~ 0.3V, C <sub>L</sub> =20pf, 3.3V±5%			0.9	
		REF(0:1)	Measured @ 2.4V ~ 0.4V, C <sub>L</sub> =20pf, 3.3V±5%			4	
		PCI(0:5)	Measured @ 2.4V ~ 0.4V, C <sub>L</sub> =30pf, 3.3V±5%			2	
		24_48MHz, 48MHz	Measured @ 2.4V ~ 0.4V, C <sub>L</sub> =20pf, 3.3V±5%			4	
Duty Cycle	D <sub>T</sub>	REF(0:1),CPU, PCI(0:5)	V <sub>T</sub> = 50%	45		55	%
		24_48MHz, 48MHz	V <sub>T</sub> = 1.5V				
Clock Skew	T <sub>SKEW</sub>	CPUT1 to CPUT0	V <sub>T</sub> = 50%			200	ps
		PCI to PCI				200	
		CPU to PCI		0		3	ns
		CPU to AGP		-500		500	
Output Impedance	Z <sub>0</sub>	CPUT1	V <sub>O</sub> = V <sub>X</sub>		30		Ohm
		CPU			50		
		PCI(0:5)	V <sub>DD</sub> =3.3V±5%		30		
		REF(0:1)			40		
		REF1			40		
		24_48MHz, 48MHz			40		

**Motherboard Clock Generator for AMD - K7**

**2. Output Buffer Electrical Specifications, continued**

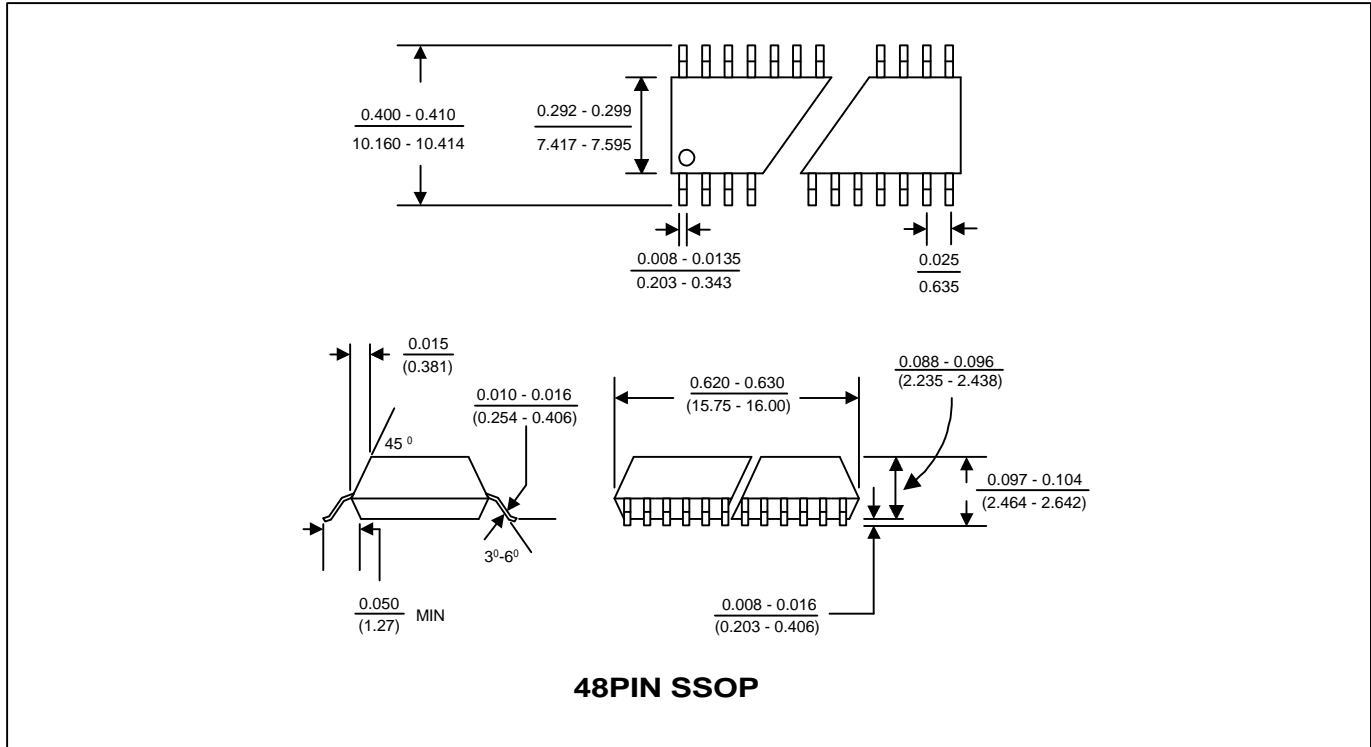
Unless otherwise stated, all power supplies = 3.3V±5%, and ambient temperature range T<sub>A</sub>= 0°C to 70°C

PARAMETERS	SYMBOL	OUTPUTS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output High Current	I <sub>OH</sub>	CPUT1	V <sub>OH</sub> = 2.0V			-40	mA
		CPU				-40	
		REF(0:1)				-34	
		PCI(0:5)				-34	
		24_48MHz				-34	
		48MHz				-34	
		SDRAM				-55	
Output Low Current	I <sub>OL</sub>	CPUT1	V <sub>OL</sub> = 0.4V	20			mA
		CPU		20			
		REF(0:1)	V <sub>OL</sub> = 0.8V	25			
		PCI(0:5)		25			
		24_48MHz		25			
		48MHz		25			
		SDRAM		43			
Jitter, One Sigma	J <sub>sigma</sub>	REF,48MHz,24MHz	V <sub>T</sub> = 1.5V			0.5	ns
Jitter, Absolute	J <sub>Abs</sub>	CPU	V <sub>T</sub> = 50%	-250		250	ps
		REF,48MHz,24MHz	V <sub>T</sub> = 1.5V	-1		1	ns
Jitter (cycle to cycle)	J <sub>cyc-cyc</sub>	CPU	V <sub>T</sub> = V <sub>X</sub>			250	ps
		PCI	Measured @ 1.5V			250	
AC Differential Voltage	V <sub>DIF</sub>	CPU (Open Drain)		0.4		V <sub>pullup</sub> +0.6	V
DC Differential Voltage	V <sub>DIF</sub>			0.2		V <sub>pullup</sub> +0.6	V
Differential Crossover Voltage	V <sub>X</sub>				550		1100

Note: V<sub>pullup</sub> = 1.5V (external); V<sub>DIF</sub> specifies the minimum input differential voltages (V<sub>TR</sub>-V<sub>CP</sub>) required for switching, where V<sub>TR</sub> is the true input level and V<sub>CP</sub> is the complement input level.

**Motherboard Clock Generator for AMD - K7**

**PACKAGE INFORMATION**



**ORDERING INFORMATION**

**For part ordering, please contact our Sales Department:**

47745 Fremont Blvd., Fremont, CA 94538, USA

Tel: (510) 492-0990 Fax: (510) 492-0991

**PART NUMBER**

The order number for this device is a combination of the following:  
Device number, Package type and Operating temperature range

**PLL205-13 X C**

PART NUMBER

TEMPERATURATURE  
C=COMMERCIAL  
M=MILITARY  
I=INDUSTRIAL  
PACKAGE TYPE  
X=SSOP

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