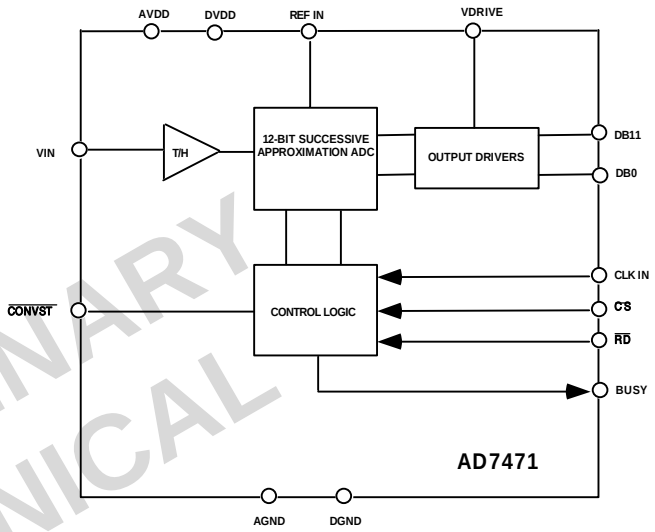
1.4us, 642µW Micropower 12-Bit Parallel ADC

Preliminary Technical Data — AD7471

FEATURES

Specified for V_{DD} of 2.7 V to 5.25 V
600KSPS for AD7471 (12-Bit)
Low Power:
500µW max per cycle for 100KSPS @ 3V Supplies
1.065mW max per cycle for 100KSPS @ 5V Supplies
Input Bandwidth = 50KHz
70dB typ SNR at 10kHz Input Frequency
Flexible Power/Throughput Rate Management
No Pipeline Delays
High Speed Parallel Interface
Sleep Mode: 50nA typ.
24-Pin SOIC and TSSOP Packages

FUNCTIONAL BLOCK DIAGRAM



AD7471 is a 12 Bit part with DB0 to DB11 as outputs

PRELIMINARY TECHNICAL DATA

GENERAL DESCRIPTION

The AD7471 is a 12-bit high speed, low power, successive-approximation ADC. The part operates from a single 2.7 V to 5.25 V power supply and feature throughput rates up to 600KSPS. The part contains a low-noise track/hold amplifier which can handle input frequencies up to 50KHz.

The conversion process and data acquisition are controlled using standard control inputs allowing easy interfacing to microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{\text{CONVST}}$ and conversion is also initiated at this point. The BUSY goes high at the start of conversion and goes low 1.4us later to indicate that the conversion is complete. There are no pipelined delays associated with the part. The conversion result is accessed via standard $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals over a high speed parallel interface.

The AD7471 uses advanced design techniques to achieve extremely low power dissipation at a 100KHz throughput rate. With 3V supplies and 100KSPS throughput rate, the parts consume just 167µA. With 5V supplies and 100KSPS, the current consumption is 213µA. The part also offers flexible power/throughput rate management.

It is also possible to operate the parts in an auto shutdown mode, where the part powers up to do a conversion and automatically enters shutdown mode at the end of conversion. Using this method allows very low power dissipation numbers at lower throughput rates.

The analog input range for the part is 0 to REF IN. The +2.5V reference is applied externally to the REF IN pin. The conversion rate is determined by the externally-applied clock.

PRODUCT HIGHLIGHTS

1. 100KHz Throughput with very Low Power Consumption.
2. Flexible Power/Throughput Rate Management
   The conversion rate is determined by an externally-applied clock allowing the power to be reduced as the conversion rate is reduced. The part also features an autoshutdown mode to maximize power efficiency at lower throughput rates.
3. No Pipeline Delay.
   The part features a standard successive-approximation ADC with accurate control of the sampling instant via a $\overline{\text{CONVST}}$ input and once off conversion control.

REV. PrB 8/99

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Analog Devices, Inc., 1998

AD7471–SPECIFICATIONS[1] (V_{DD} = +2.7 V to +5.25 V, REF IN = 2.5 V, $f_{CLK\ IN}$ = 10 MHz unless otherwise noted; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	A Version[1]		Units	Test Conditions/Comments
DYNAMIC PERFORMANCE	**5V**	**3V**		
Signal to Noise + Distortion (SINAD)	68	68	dB min	f_{IN} =10kHz Sine Wave, f_S = 100Ksps
Signal to Noise Ratio (SNR)	68	68	dB min	f_{IN} =10kHz Sine Wave, f_S = 100Ksps
Total Harmonic Distortion (THD)	-83	-78	db typ	f_{IN} =10kHz Sine Wave, f_S = 100Ksps
	–75	-75	dB max	f_{IN} =10kHz Sine Wave, f_S = 100Ksps
Peak Harmonic or Spurious Noise	-86	-86	db typ	f_{IN} =10kHz Sine Wave, f_S = 100Ksps
(SFDR)	–76	-76	dB max	f_{IN} =10kHz Sine Wave, f_S = 100Ksps
Intermodulation Distortion (IMD)				
Second Order Terms	–86	-86	dB typ	f_{IN} =10kHz Sine Wave, f_S = 100Ksps
Third Order Terms	–86	-86	dB typ	f_{IN} =10kHz Sine Wave, f_S = 100Ksps
Aperture Delay	5	5	ns typ	
Aperture Jitter	15	15	ns typ	
Full Power Bandwidth	20	20	MHz max	
DC ACCURACY				
Resolution	12	12	Bits	
Integral Nonlinearity	±1	±1	LSB max	
Differential Nonlinearity	±0.9	±0.9	LSB max	Guaranteed No Missed Codes to 12 Bits.
Offset Error	±10	±10	LSB max	
Gain Error	±2	±2	LSB max	
ANALOG INPUT				
Input Voltage Ranges	0 to REF IN	0 to REF IN	Volts	
dc Leakage Current	±1	±1	µA max	
Input Capacitance	33	33	pF typ	
REFERENCE INPUT				
REF IN Input Voltage Range	2.5	2.5	V	+/-1% for Specified Performance
dc Leakage Current	±1	±1	µA max	
Input Capacitance	10/20	10/20	pF typ	Track/Hold Mode
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.4	0.4	V max	
Input Current, I_{IN}	±1	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[3]	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	V_{DRIVE} -0.2	V_{DRIVE} -0.2	V min	I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} =200mA
Floating-State Leakage Current	±10	±10	µA max	V_{DD} = 2.7 V to 5.25 V
Floating-State Output Capacitance	10	10	pF max	
Output Coding	Straight(Natural) Binary			
CONVERSION RATE				
Conversion Time	14	14	CLK IN Cycles max	
Track/Hold Acquisition Time	250	250	ns max	
Throughput Rate	600	tbd	KSPS max	Conversion Time + Acquisition Time. CLK IN at 10MHz @ 5V

PRELIMINARY TECHNICAL DATA

AD7471–SPECIFICATIONS[1] (V_{DD} = +2.7 V to +5.25 V, REF IN = 2.5 V, $f_{CLK\ IN}$ = 10 MHz unless otherwise noted; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	A Version	Units	Test Conditions/Comments
POWER REQUIREMENTS			
V_{DD}	+2.7/+5.25	V min/max	
I_{DD}[4]			Digital I/Ps = 0V or DV_{DD}
Normal Mode	0.23	mA max	V_{DD} = 4.75V to 5.25V. f_S=100KSPS
Quiescent Current	0.12	mA max	V_{DD} = 4.75V to 5.25V
Normal Mode	0.18	mA max	V_{DD} = 2.7V to 3.3V. f_S=100KSPS
Quiescent Current	0.12	mA max	V_{DD} = 2.7V to 3.3V
Shutdown Mode	1	uA max	CLK IN =0V or DV_{DD}
Power Dissipation[4]			Digital I/Ps = 0V or DV_{DD}
Normal Mode	0.677	mW max	V_{DD} = 5V. f_S=100KSPS
	0.385	mW max	V_{DD} = 3V f_S=100KSPS
Shutdown Mode	5	uW max	V_{DD} = 5 V. CLK IN =0V or DV_{DD}
	3	uW max	V_{DD} = 3 V. CLK IN =0V or DV_{DD}

NOTES
[1]Temperature ranges as follows: A Versions: –40°C to +85°C.
[2]SNR calculation includes distortion and noise components.
[3] Sample tested @ +25°C to ensure compliance.
[4] See POWER VERSUS THROUGHPUT RATE section.

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

TIMING SPECIFICATIONS[1] (V_{DD} = +2.7 V to +5.25 V, REF IN = 2.5 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX} AD7471	Units	Description
f_{CLK}[2]	1	kHz min	
	10	MHz max	
$t_{CONVERT}$	1.4	us max	t_{CLK}= $1/f_{CLK\ IN}$
t_{WAKEUP}	1	us max	Wakeup Time
t_{acq}	250	ns min	Acquisition Time
t_1	10	ns min	$\overline{CONVST}$ Pulse Width
t_2[3]	10	ns max	$\overline{CONVST}$ to BUSY Delay, V_{DD} = 5 V
	30	ns max	$\overline{CONVST}$ to BUSY Delay, V_{DD} = 3 V
t_3	0	ns max	BUSY to $\overline{CS}$ Setup Time
t_4[4]	0	ns max	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_5	20	ns min	$\overline{RD}$ Pulse Width
t_6[4]	15	ns min	Data Access Time After Falling Edge of $\overline{RD}$
t_7[5]	8	ns max	Bus Relinquish Time After Rising Edge of $\overline{RD}$
t_8	0	ns max	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_9	100	ns min	Quite Time

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 Volts. See Figure 2.

[2]Mark/Space ratio for the CLK input is 40/60 to 60/40.

[3]t_2 is 35 ns max @ 125°C.

[4]Measured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.8 V or 2.0 V.

[5]t_7 is derived form the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_7, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

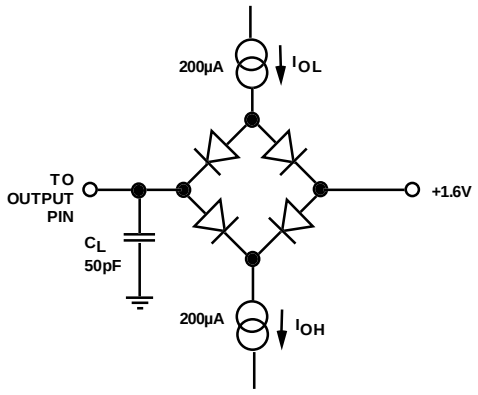
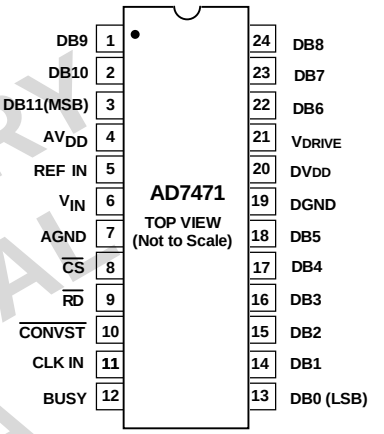


Figure 1. Load Circuit for Digital Output Timing Specifications

ABSOLUTE MAXIMUM RATINGS[1]
(T_A = +25°C unless otherwise noted)

AV_{DD} to AGND/DGND .....-0.3V to +7V
DV_{DD} to AGND/DGND .....-0.3V to +7V
V_{DRIVE} to AGND/DGND .....-0.3V to +7V
AV_{DD} to DV_{DD} ..... -0.3V to +0.3V
V_{DRIVE} to DV_{DD} ..... -0.3V to DV_{DD}+0.3V
AGND TO DGND .....-0.3V to +0.3V
Analog Input Voltage to AGND ...-0.3V to AVDD+0.3V
Digital Input Voltage to DGND ..-0.3V to DVDD+0.3V
REF IN to AGND .....-0.3V to AVDD+0.3V
Input Current to Any Pin Except Supplies[2] .....±10mA
Operating Temperature Range
Commercial (A Version) .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature ..... +150°C
SOIC, TSSOP Package Dissipation ..... +450mW
θ_{JA} Thermal Impedance ..... 75°C/W (SOIC)
..... 115°C/W(TSSOP)
θ_{JC} Thermal Impedance ..... 25°C/W (SOIC)
..... 35°C/W (TSSOP)
Lead Temperature, Soldering
Vapor Phase (60 secs) ..... +215°C
Infared (15 secs) ..... +220°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100 mA will not cause SCR latch up.



AD7471 PIN CONFIGURATION

PRELIMINARY TECHNICAL DATA

ORDERING GUIDE

Model	Range	Resolution (Bits)	Package Option[1]	Branding
AD7471AR	-40°C to +85°C	12	R-24	
AD7471ARU	-40°C to +85°C	12	RU-24	
EVAL-AD7471CB[2]	Evaluation Board			
EVAL-CONTROL BOARD[3]	Controller Board			

NOTES
[1]R = SOIC; RU = TSSOP.
[2]This can be used as a stand-alone evaluation board or in conjunction with the EVAL-CONTROL BOARD for evaluation/ demonstration purposes.
[3]This board is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators.

CAUTION
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the XX0000 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTION

Pin Mnemonic	Function
$\overline{CS}$	Chip Select. Active low logic input used in conjunction with $\overline{RD}$ to access the conversion result. The conversion result is placed on the data bus following the falling edge of both $\overline{CS}$ and $\overline{RD}$. $\overline{CS}$ and $\overline{RD}$ are both connected to the same AND gate on the input so the signals are interchangeable. $\overline{CS}$ can be hardwired permanently low.
$\overline{RD}$	Read Input. Logic Input used in conjunction with $\overline{CS}$ to access the conversion result. The conversion result is placed on the data bus following the falling edge of both $\overline{CS}$ and $\overline{RD}$. $\overline{CS}$ and $\overline{RD}$ are both connected to same AND gate on the input so the signals are interchangeable. $\overline{CS}$ and $\overline{RD}$ can be hardwired permanently low in which case, the data bus is always active and the result of the new conversion is clocked out slightly before to the BUSY line going low.
$\overline{CONVST}$	Conversion Start Input. Logic Input used to initiate conversion. The input track/hold amplifier goes from track mode to hold mode on the falling edge of $\overline{CONVST}$ and the conversion process is initiated at this point. The conversion input can be as narrow as 10 ns. If the $\overline{CONVST}$ input is kept low for the duration of conversion and is still low at the end of conversion, the part will automatically enter sleep mode. If the part enters this sleep mode, the next rising edge of $\overline{CONVST}$ wakes up the part. Wake-up time for the part is typically 1 µs.
CLK IN	Master Clock Input. The clock source for the conversion process is applied to this pin. Conversion time for the AD7471 takes 14 clock cycles. The frequency of this master clock input, therefore, determines the conversion time and achievable throughput rate. While the ADC is not converting, the Clock-In pad is in three-state and thus no clock is going through the part. The frequency range for this clock input is from 1KHz to 10MHz.
BUSY	BUSY Output. Logic Output indicating the status of the conversion process. The BUSY signal goes high after the falling edge of $\overline{CONVST}$ and stays high for the duration of conversion. Once conversion is complete and the conversion result is in the output register, the BUSY line returns low. The track/hold returns to track mode just prior to the falling edge of BUSY and the acquisition time for the part begins when BUSY goes low. If the $\overline{CONVST}$ input is still low when BUSY goes low, the part automatically enters its sleep mode on the falling edge of BUSY.
REF IN	Reference Input. An external reference must be applied to this input. The voltage range for the external reference is 2.5 V ±1% for specified performance.
AV_{DD}	Analog Supply Voltage, +2.7 V to +5.25 V. This is the only supply voltage for all analog circuitry on the AD7471. The AV_{DD} and DV_{DD} voltages should ideally be at the same potential and must not be more than 0.3 V apart even on a transient basis. This supply should be decoupled to AGND.
DV_{DD}	Digital Supply Voltage, +2.7 V to +5.25 V. This is the supply voltage for all digital circuitry on the AD7471 apart from the output drivers. The DV_{DD} and AV_{DD} voltages should ideally be at the same potential and must not be more than 0.3 V apart even on a transient basis. This supply should be decoupled to DGND.
AGND	Analog Ground. Ground reference point for all analog circuitry on the AD7471. All analog input signals and any external reference signal should be referred to this AGND voltage. The AGND and DGND voltages should ideally be at the same potential and must not be more than 0.3 V apart even on a transient basis.
DGND	Digital Ground. This is the ground reference point for all digital circuitry on the AD7471. The DGND and AGND voltages should ideally be at the same potential and must not be more than 0.3 V apart even on a transient basis.
V_{IN}	Analog Input. Single-ended analog input channel. The input range is 0 V to REFIN. The analog input presents a high dc input impedance.
V_{DRIVE}	Supply Voltage for the Output Drivers, +2.7 V to +5.25 V. This voltage determines the output high voltage for the data output pins. It allows the AV_{DD} and DV_{DD} to operate at 5 V (and maximize the dynamic performance of the ADC) while the digital outputs can interface to 3 V logic.
DB0–DB11	Data Bit 0 to Data Bit 11. Parallel digital outputs that provide the conversion result for the part. These are three-state outputs that are controlled by $\overline{CS}$ and $\overline{RD}$. The output high voltage level for these outputs is determined by the V_{DRIVE} input.

PRELIMINARY TECHNICAL DATA

TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1/2 LSB below the first code transition, and full scale, a point 1/2 LSB above the last code transition.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
This is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, i.e., AGND + 1 LSB.

Gain Error
The last transition should occur at the analog value 1 1/2 LSB below the nominal full scale. The first transition is a 1/2 LSB above the low end of the scale (zero in the case of AD7471). The gain error is the deviation of the actual difference between the first and last code transitions from the ideal difference between the first and last code transitions with offset errors removed.

Track/Hold Acquisition Time
The track/hold amplifier returns into track mode after the end of conversion. Track/Hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±1 LSB, after the end of conversion.

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$\textit{Signal to (Noise + Distortion)} = (6.02\ N + 1.76)\ dB$$

Thus for a 12-bit converter, this is 74 dB and for a 10-bit converter is 62 dB.

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7471 it is defined as:

$$THD\ (dB) = 20\ \log \frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2)}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation distortion terms are those for which neither m nor n is equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7471 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

Aperture Delay
In a sample/hold, the time required after the hold command for the switch to open fully is the aperture delay. The sample is, in effect, delayed by this interval, and the hold command would have to be advanced by this amount for precise timing.

Aperture Jitter
Aperture jitter is the range of variation in the aperture delay. In other words, it is the uncertainty about when the sample is taken. Jitter is the result of noise which modulates the phase of the hold command. This specification establishes the ultimate timing error, hence the maximum sampling frequency for a given resolution. This error will increase as the input dV/dt increases.

PRELIMINARY TECHNICAL DATA

CIRCUIT DESCRIPTION

CONVERTER OPERATION

The AD7471 is a 12-bit successive approximation analog-to-digital converter based around a capacitive DAC. The AD7471 can convert analog input signals in the range 0 V to V_{REF}. Figure 2 shows a very simplified schematic of the ADC. The Control Logic, SAR and the Capacitive DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition.

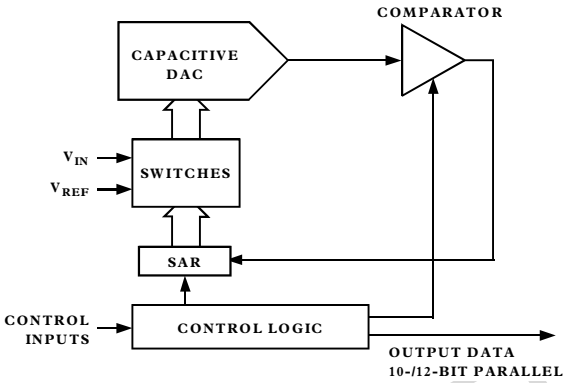


Figure 2. Simplified Block Diagram of AD7471

Figure 3 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in Position A. The comparator is held in a balanced condition and the sampling capacitor acquires the signal on V_{IN}.

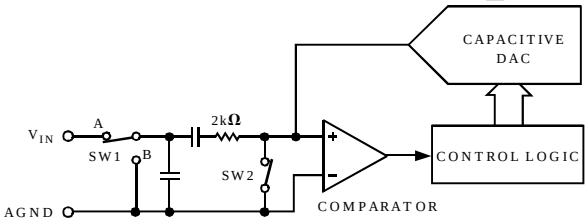


Figure 3. ADC Acquisition Phase

Figure 4 shows the ADC during conversion. When conversion starts SW2 will open and SW1 will move to position B, causing the comparator to become unbalanced. The ADC then runs through its successive approximation routine and brings the comparator back into a balanced condition. When the comparator is rebalanced, the conversion result is available in the SAR register.

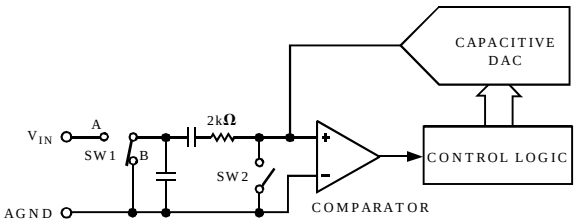


Figure 4. ADC Conversion Phase

TYPICAL CONNECTION DIAGRAM

Figure 5 shows a typical connection diagram for the AD7471. Conversion is initiated by a falling edge on $\overline{CONVST}$. Once $\overline{CONVST}$ goes low the BUSY signal goes high, and at the end of conversion the falling edge of BUSY is used to activate an Interrupt Service Routine. The $\overline{CS}$ and $\overline{RD}$ lines are then activated in parallel to read the 12-data bits. The recommended REF IN voltage is 2.5 V providing an analog input range of 0 V to 2.5 V, making the AD7471 a unipolar A/D. It is recommended to perform a dummy conversion after power-up as the first conversion result could be incorrect. This also ensures that the part is in the correct mode of operation. The $\overline{CONVST}$ pin should not be floating when power is applied as a rising edge on $\overline{CONVST}$ might not wake up the part.

In Figure 5 the V_{DRIVE} pin is tied to DV_{DD}, which results in logic output voltage values being either 0 V or DV_{DD}. The voltage applied to V_{DRIVE} controls the voltage value of the output logic signals. For example, if DV_{DD} is supplied by a 5 V supply and V_{DRIVE} by a 3 V supply, the logic output voltage levels would be either 0 V or 3 V. This feature allows the AD7471 to interface to 3 V parts while still enabling the A/D to process signals at 5 V supply.

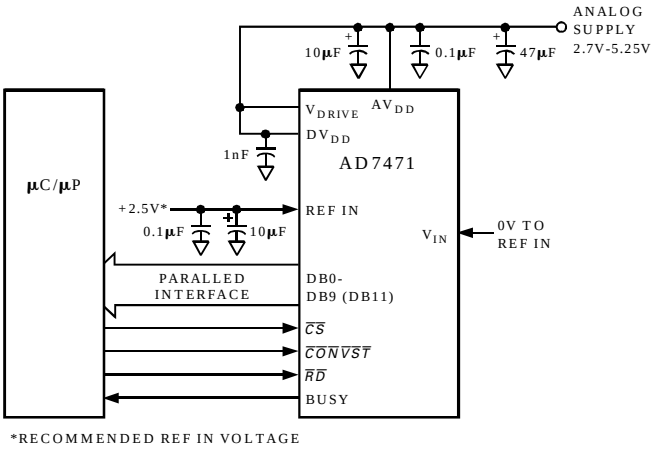


Figure 5. Typical Connection Diagram

PRELIMINARY TECHNICAL DATA

ADC TRANSFER FUNCTION

The output coding of the AD7471 is straight binary. The designed code transitions occur at successive integer LSB values (i.e., 1 LSB, 2 LSB, etc.). The LSB size is = (REF IN)/4096. The ideal transfer characteristic for the AD7471 is shown in Figure 6.

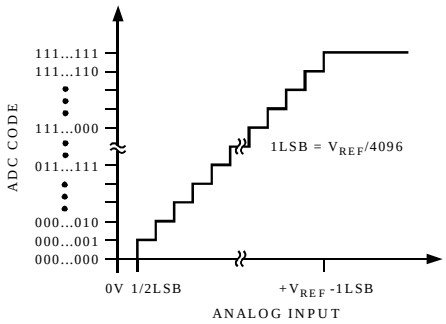


Figure 6. Transfer Characteristic for 12 Bits

AC ACQUISITION TIME

In ac applications it is recommended to always buffer analog input signals. The source impedance of the drive circuitry must be kept as low as possible to minimize the acquisition time of the ADC. Large values of impedance at the VIN pin of the ADC will cause the THD to degrade at high input frequencies.

INPUT BUFFERS	AD7471 DYNAMIC PERFORMANCE SPECIFICATIONS SNR 50kHz	THD 50kHz	TYPICAL AMPLIFIER CURRENT CONSUMPTION
AD8047	70	78	5.8mA
AD8051	68.6	78	4.4mA

Figure 7. Recommended Input Buffers

Reference Input

The following references are best suited for use with the AD7471.

ADR291
AD780
AD192

For optimum performance, a 2.5 V reference is recommended. The part can function with a reference up to 3 V and down to 2 V, but the performance deteriorates.

DC Acquisition Time

The ADC starts a new acquisition phase at the end of a conversion and ends it on the falling edge of the $\overline{\text{CONVST}}$ signal. At the end of conversion there is a settling time associated with the sampling circuit. This settling time lasts approximately 250 ns. The analog signal on V_{IN} is also being acquired during this settling time; therefore, the minimum acquisition time needed is approximately 250 ns.

Figure 8 shows the equivalent charging circuit for the sampling capacitor when the ADC is in its acquisition phase. R3 represents the source impedance of a buffer amplifier or resistive network, R1 is an internal switch resistance, R2 is for bandwidth control and C1 is the sampling capacitor. C2 is back-plate capacitance and switch parasitic capacitance.

During the acquisition phase the sampling capacitor must be charged to within 1 LSB of its final value.

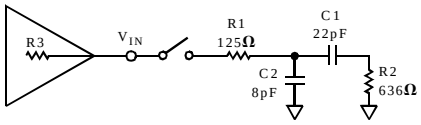


Figure 8. Equivalent Sampling Circuit

ANALOG INPUT

Figure 9 shows the equivalent circuit of the analog input structure of the AD7471. The two diodes, D1 and D2, provide ESD protection for the analog inputs. The capacitor C3 is typically about 4 pF and can be primarily attributed to pin capacitance. The resistor R1 is an internal switch resistance. This resistor is typically about 125r. The capacitor C1 is the sampling capacitor while R2 is used for bandwidth control.

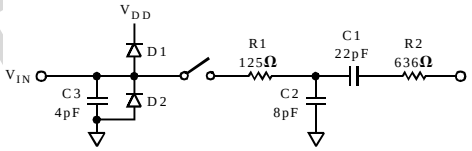


Figure 9. Equivalent Analog Input Circuit

CLOCK SOURCES

The max CLK specification for the AD7471 is 10 MHz. This frequency is a standard off-the-shelf oscillator frequency. Many manufacturers produce oscillator modules at this frequency or close to this frequency. Of course any clock source can be used, not just crystal oscillators.

PRELIMINARY TECHNICAL DATA

PARALLEL INTERFACE

The parallel interface of the AD7471 is 12-bits wide. The output data buffers are activated when both $\overline{CS}$ and $\overline{RD}$ are logic low. At this point the contents of the data register are placed onto the data bus. Figure 10 shows the timing diagram for the parallel port.

Figure 11 shows the timing diagram for the parallel port when $\overline{CS}$ and $\overline{RD}$ are tied permanently low. In this setup, once the BUSY line goes from high to low the conversion process is completed. The data is available on the output bus slightly before the falling edge of BUSY.

It is important to point out that data bus cannot change state while the A/D is doing a conversion as this would have a detrimental effect on the conversion in progress. The data out lines will go three-state again when either the $\overline{RD}$ or $\overline{CS}$ line goes high. Thus the $\overline{CS}$ can be tied low permanently, leaving the $\overline{RD}$ line to control conversion result access. Please reference the V_{DRIVE} section for output voltage levels.

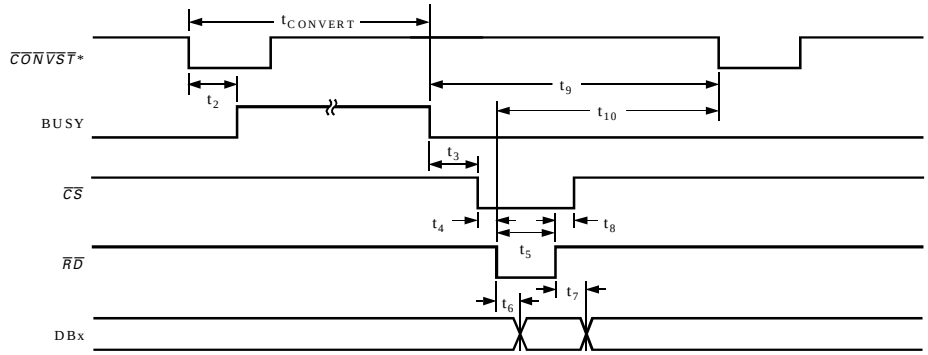


Figure 10. Parallel Port Timing

PRELIMINARY TECHNICAL DATA

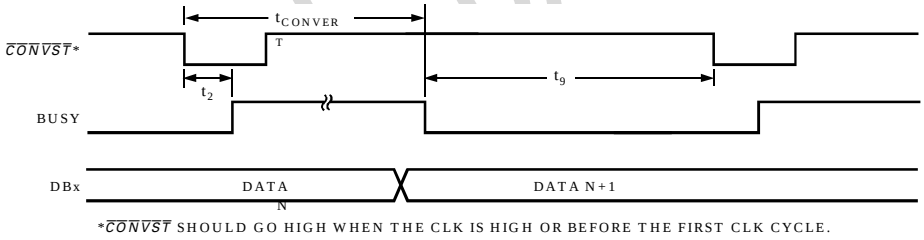


Figure 11. Parallel Port Timing with $\overline{CS}$ and $\overline{RD}$ Tied Low

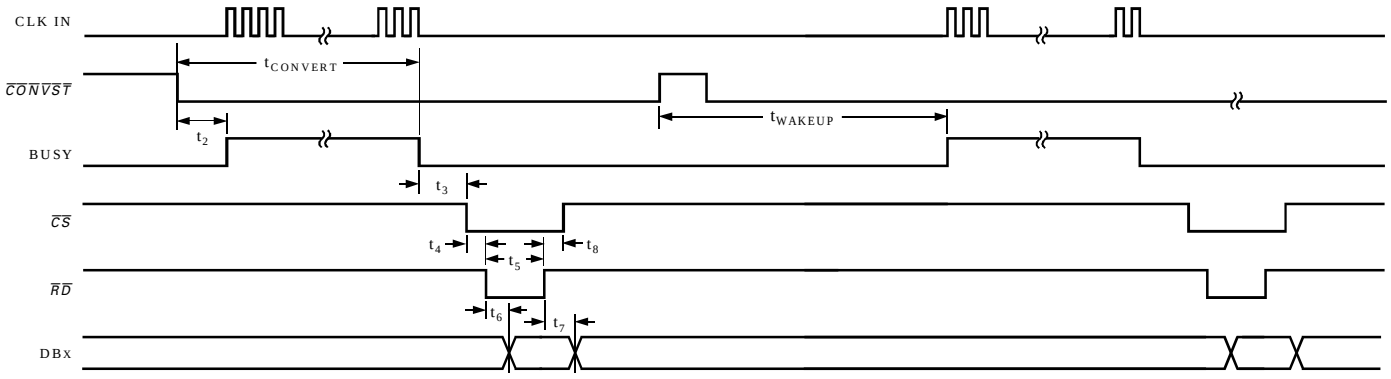


Figure 12. Wake-Up Timing Diagram (Burst Clock)

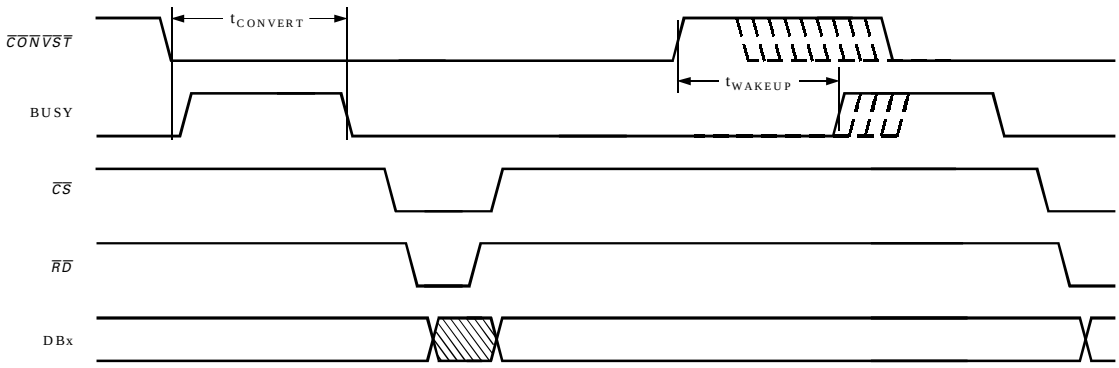


Figure 13. Mode 2 Operation

PRELIMINARY TECHNICAL DATA

OPERATING MODES

The AD7471 has two possible modes of operation depending on the state of the $\overline{CONVST}$ pulse at the end of a conversion, Mode 1 and Mode 2. There is a continuous clock on the CLK IN pin.

Mode 1 (High Speed Sampling)

In this mode of operation the $\overline{CONVST}$ pulse is brought high before the end of conversion i.e., before the BUSY goes low (see Figure 10). If the $\overline{CONVST}$ pin is brought from high to low while BUSY is high, the conversion is restarted. When operating in this mode a new conversion should not be initiated until 250 ns after BUSY goes low. This acquisition time allows the track/hold circuit to accurately acquire the input signal. As mentioned earlier, a read should not be done during a conversion. This mode facilitates the fastest throughput times for the AD7471.

Mode 2 (Sleep Mode)

Figure 13 shows AD7471 in Mode 2 operation where the ADC goes into sleep mode after conversion. The $\overline{CONVST}$ line is brought low to initiate a conversion and remains low until after the end of conversion. If $\overline{CONVST}$ goes high and low again while BUSY is high, the conversion is restarted. Once the BUSY line goes from a high to a low, the $\overline{CONVST}$ line has its status checked and, if low, the part enters sleep mode.

The device wakes up again on the rising edge of the $\overline{CONVST}$ signal. There is a wake-up time of typically 1 µs after the rising edge of $\overline{CONVST}$ before the BUSY line can go high to indicate start of conversion. BUSY will only go high once $\overline{CONVST}$ goes low. The $\overline{CONVST}$ line can go from a high to a low during this wake-up time, but the conversion will still not be initiated until after the 1 µs wake-up time. Superior power performance can be achieved in this mode of operation by waking up the AD7471 only to carry out a conversion.

Burst Mode

Burst mode on the AD7471 is a subsection of Mode 1 and Mode 2, the clock is noncontinuous. Figure 12 shows how the ADC works in burst mode for Mode 2. The clock needs only to be switched on during conversion, maximum of 14 clock cycles for the AD7471. As the clock is off during nonconverting intervals, system power is saved. The BUSY signal can be used to gate the CLK IN pulses. The ADC does not begin the conversion process until the first CLK IN rising edge after BUSY goes high. The clock needs to start less than two clock cycles away from the $\overline{CONVST}$ active edge otherwise INL deteriorates; e.g., if the clock frequency is 10 MHz the clock must start within 200 ns of $\overline{CONVST}$ going low. In Figure 12 the A-D converter section is put into sleep mode once conversion is completed and on the rising edge of $\overline{CONVST}$ it is woken up again; the user must be wary of the wake-up time as this will reduce the sampling rate of the ADC.

V_{DRIVE}

The V_{DRIVE} pin is used as the voltage supply to the output drivers and is a separate supply from AV_{DD} and DV_{DD}. The purpose of using a separate supply for the output drivers is that the user can vary the output high voltage, V_{OH}, from the V_{DD} supply to the AD7471. For example, if AV_{DD} and DV_{DD} is using a 5 V supply, the V_{DRIVE} pin can be powered from a 3 V supply. The ADC has better dynamic performance at 5 V than at 3 V, so operating the part at 5 V, while still being able to interface to 3 V parts, pushes the AD7471 to the top bracket of high performance 12-bit A/Ds. Of course, the ADC can have its V_{DRIVE} and DV_{DD} pins connected together and be powered from a 3 V or 5 V supply.

All outputs are powered from V_{DRIVE}. These are all the data out pins and the BUSY pin. The $\overline{CONVST}$, $\overline{CS}$, $\overline{RD}$ and CLK IN signals are related to the DV_{DD} voltage.

POWER-UP

It is recommended that the user performs a dummy conversion after power-up, as the first conversion result could be incorrect. This also ensures that the parts is in the correct mode of operation. The recommended power-up sequence is as follows:

1 > GND	4 > Digital Inputs
2 > V_{DD}	5 > REF IN
3 > V_{DRIVE}	6 > V_{IN}

POWER V'S THROUGHPUT

The two modes of operation for this part will produce different power performances, Mode 1 and Mode 2 - see Operating Modes section of the data sheet for more detail descriptions of these modes. Mode 2 is Automatic Power-Down of the part after conversion and it achieves the optimum power poformance from the AD7471.

Mode 1

Figure 14 shows the AD7471 conversion sequence in Mode 1 using a throughput rate of 100 kSPS and a clock frequency of 10 MHz. At 5 V supply the current consumption for the part when converting is typically 200 µA and the quiescent current is 116 µA. The digital current consumption is typically 85 µA. The conversion time of 1.4 µs contributes 140 µW to the overall power dissipation in the following way:

$$(1.4\ \mu s/10\ \mu s) \times (5 \times 200\ \mu A) = 140\ \mu W$$

The contribution to the total power dissipated by the remaining 8.6 µs of the cycle is 498 µW.

$$(8.6\ \mu s/10\ \mu s) \times (5 \times 116\ \mu A) = 498\ \mu W$$

Thus the power dissipated during each cycle, which includes digital current consumption, is.....

$$140\ \mu W + 498\ \mu W + (5 \times 85\ \mu W) = 1.063\ mW$$

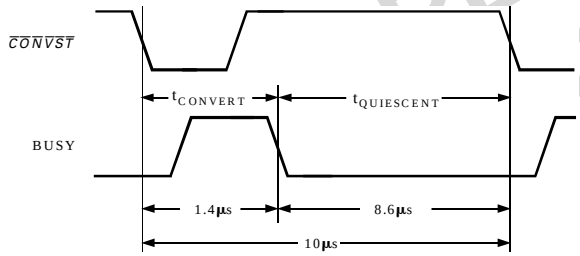


Figure 14. Mode 1 Power Dissipation

Mode 2

Figure 15 shows the AD7471 conversion sequence in Mode 2 using a throughput rate of 100 kSPS and a clock frequency of 10 MHz. At 5 V supply the current consumption for the part when converting is 200 µA, while the sleep current is 1 µA max. The power dissipated during this power-down is negligible and is thus not worth considering in the total power figure. During the wake-up phase, the AD7471 will draw 120 µA. Overall power dissipated is:

$$(1.4\ \mu s/10\ \mu s) \times (5 \times 200\ \mu A) + (1\ \mu s/10\ \mu s) \times (5 \times 120\ \mu A) = 200\ \mu W$$

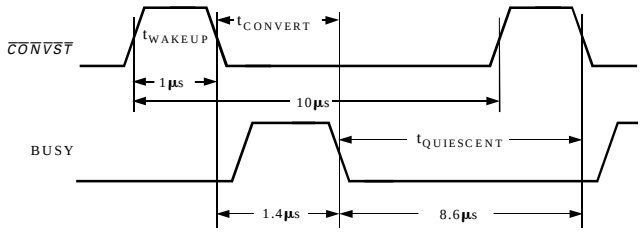


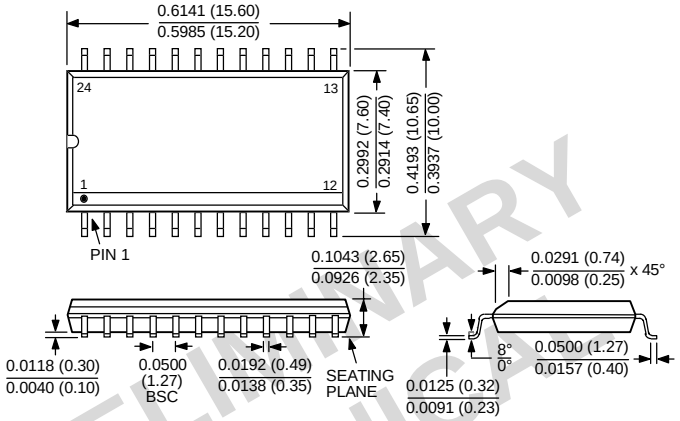
Figure 15. Mode 2 Power Dissipation

PRELIMINARY TECHNICAL DATA

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

24-LEAD SOIC (R-24)



PRELIMINARY TECHNICAL DATA

24-LEAD TSSOP (RU-24)