

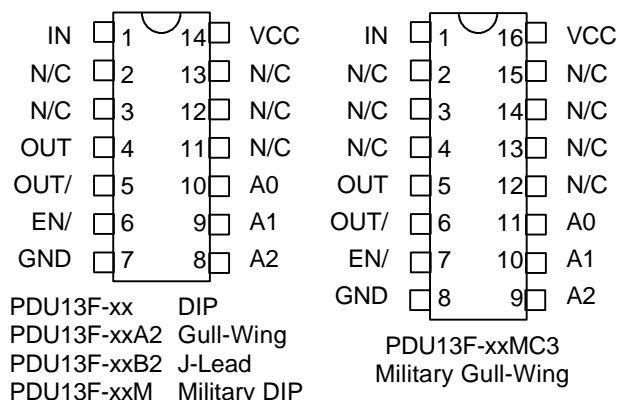
3-BIT PROGRAMMABLE DELAY LINE (SERIES PDU13F)



FEATURES

- Digitally programmable in 8 delay steps
- Monotonic delay-versus-address variation
- Two separate outputs: inverting & non-inverting
- Precise and stable delays
- Input & outputs fully TTL interfaced & buffered
- 10 T²L fan-out capability
- Fits standard 14-pin DIP socket
- Auto-insertable

PACKAGES



FUNCTIONAL DESCRIPTION

The PDU13F-series device is a 3-bit digitally programmable delay line. The delay, TD_A , from the input pin (IN) to the output pins (OUT, OUT/) depends on the address code (A2-A0) according to the following formula:

$$TD_A = TD_0 + T_{INC} * A$$

where A is the address code, T_{INC} is the incremental delay of the device, and TD_0 is the inherent delay of the device. The incremental delay is specified by the dash number of the device and can range from 0.5ns through 50ns, inclusively. The enable pin (EN/) is held LOW during normal operation. When this signal is brought HIGH, OUT and OUT/ are forced into LOW and HIGH states, respectively. The address is not latched and must remain asserted during normal operation.

PIN DESCRIPTIONS

IN Delay Line Input
 OUT Non-inverted Output
 OUT/ Inverted Output
 A2 Address Bit 2
 A1 Address Bit 1
 A0 Address Bit 0
 EN/ Output Enable
 VCC +5 Volts
 GND Ground

SERIES SPECIFICATIONS

- **Total programmed delay tolerance:** 5% or 1ns, whichever is greater
- **Inherent delay (TD_0):** 6ns typical (OUT)
5.5ns typical (OUT/)
- **Setup time and propagation delay:**
 Address to input setup (T_{AIS}): 6ns
 Disable to output delay (T_{DISO}): 6ns typ. (OUT)
- **Operating temperature:** 0° to 70° C
- **Temperature coefficient:** 100PPM/°C (excludes TD_0)
- **Supply voltage V_{CC} :** 5VDC \pm 5%
- **Supply current:** $I_{CCH} = 45\text{ma}$
 $I_{CCL} = 20\text{ma}$
- **Minimum pulse width:** 20% of total delay

DASH NUMBER SPECIFICATIONS

| Part Number | Incremental Delay Per Step (ns) | Total Delay Change (ns) |
|-------------|---------------------------------|-------------------------|
| PDU13F-.5 | .5 \pm .3 | 3.5 \pm 1.0 |
| PDU13F-1 | 1 \pm .4 | 7 \pm 1.0 |
| PDU13F-2 | 2 \pm .4 | 14 \pm 1.0 |
| PDU13F-3 | 3 \pm .5 | 21 \pm 1.1 |
| PDU13F-5 | 5 \pm .6 | 35 \pm 1.8 |
| PDU13F-10 | 10 \pm 1.0 | 70 \pm 3.5 |
| PDU13F-15 | 15 \pm 1.3 | 105 \pm 5.3 |
| PDU13F-20 | 20 \pm 1.5 | 140 \pm 7.0 |
| PDU13F-40 | 40 \pm 2.0 | 280 \pm 14.0 |
| PDU13F-50 | 50 \pm 2.5 | 350 \pm 17.5 |

NOTE: Any dash number between .5 and 50 not shown is also available.

APPLICATION NOTES

ADDRESS UPDATE

The PDU13F is a memory device. As such, special precautions must be taken when changing the delay address in order to prevent spurious output signals. The timing restrictions are shown in Figure 1.

After the last signal edge to be delayed has appeared on the OUT pin, a minimum time, T_{OAX} , is required before the address lines can change. This time is given by the following relation:

$$T_{OAX} = \max \{ (A_i - A_{i-1}) * T_{INC} , 0 \}$$

where A_{i-1} and A_i are the old and new address codes, respectively. Violation of this constraint may, depending on the history of the input signal, cause spurious signals to appear on the OUT pin. The possibility of spurious signals persists until the required T_{OAX} has elapsed.

A similar situation occurs when using the EN/ signal to disable the output while IN is active. In this case, the unit must be held in the disabled state until the device is able to “clear” itself. This is achieved by holding the EN/ signal high and the IN signal low for a time given by:

$$T_{DISH} = A_i * T_{INC}$$

Violation of this constraint may, depending on the history of the input signal, cause spurious signals to appear on the OUT pin. The

possibility of spurious signals persists until the required T_{DISH} has elapsed.

INPUT RESTRICTIONS

There are three types of restrictions on input pulse width and period listed in the **AC Characteristics** table. The **recommended** conditions are those for which the delay tolerance specifications and monotonicity are guaranteed. The **suggested** conditions are those for which signals will propagate through the unit without significant distortion. The **absolute** conditions are those for which the unit will produce some type of output for a given input.

When operating the unit between the recommended and absolute conditions, the delays may deviate from their values at low frequency. However, these deviations will remain constant from pulse to pulse if the input pulse width and period remain fixed. In other words, the delay of the unit exhibits frequency and pulse width dependence when operated beyond the recommended conditions. Please consult the technical staff at Data Delay Devices if your application has specific high-frequency requirements.

Please note that the increment tolerances listed represent a design goal. Although most delay increments will fall within tolerance, they are not guaranteed throughout the address range of the unit. Monotonicity is, however, guaranteed over all addresses.

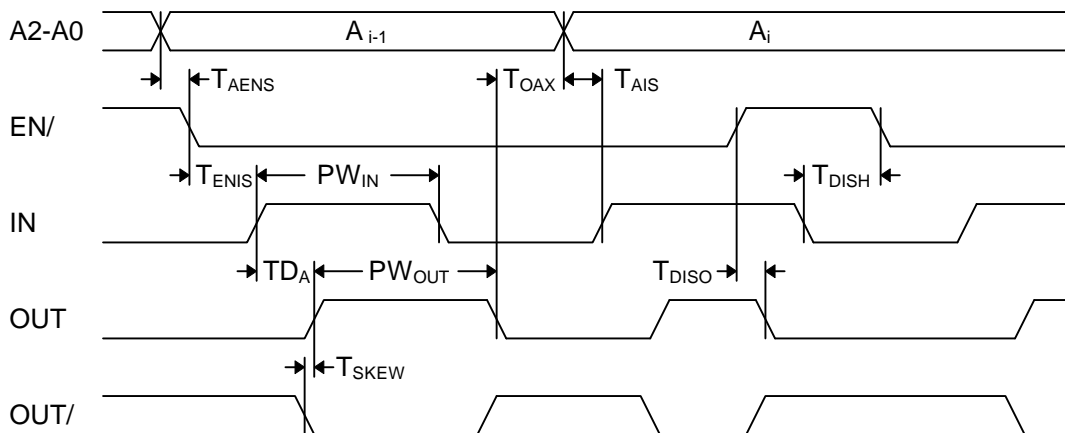


Figure 1: Timing Diagram

DEVICE SPECIFICATIONS

TABLE 1: AC CHARACTERISTICS

| PARAMETER | SYMBOL | MIN | TYP | UNITS |
|------------------------------|-------------|------------|-----|-------------|
| Total Programmable Delay | TD_T | | 7 | T_{INC} |
| Inherent Delay | TD_0 | | 6.0 | ns |
| Output Skew | T_{SKEW} | | 1.5 | ns |
| Disable to Output Low Delay | T_{DISO} | | 6.0 | ns |
| Address to Enable Setup Time | T_{AENS} | 2.0 | | ns |
| Address to Input Setup Time | T_{AIS} | 6.0 | | ns |
| Enable to Input Setup Time | T_{ENIS} | 6.0 | | ns |
| Output to Address Change | T_{OAX} | See Text | | |
| Disable Hold Time | T_{DISH} | See Text | | |
| Input Period | Absolute | PER_{IN} | 20 | % of TD_T |
| | Suggested | PER_{IN} | 50 | % of TD_T |
| | Recommended | PER_{IN} | 200 | % of TD_T |
| Input Pulse Width | Absolute | PW_{IN} | 10 | % of TD_T |
| | Suggested | PW_{IN} | 25 | % of TD_T |
| | Recommended | PW_{IN} | 100 | % of TD_T |

TABLE 2: ABSOLUTE MAXIMUM RATINGS

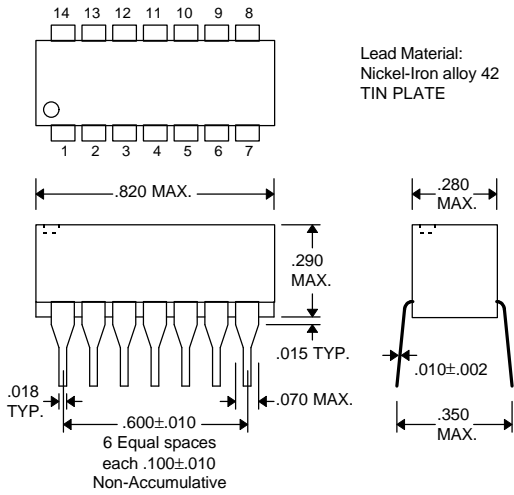
| PARAMETER | SYMBOL | MIN | MAX | UNITS | NOTES |
|---------------------|------------|------|--------------|-------|--------|
| DC Supply Voltage | V_{CC} | -0.3 | 7.0 | V | |
| Input Pin Voltage | V_{IN} | -0.3 | $V_{DD}+0.3$ | V | |
| Storage Temperature | T_{STRG} | -55 | 150 | C | |
| Lead Temperature | T_{LEAD} | | 300 | C | 10 sec |

TABLE 3: DC ELECTRICAL CHARACTERISTICS

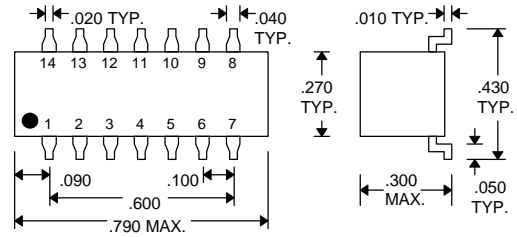
(0C to 70C, 4.75V to 5.25V)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|--|-----------|-----|------|------|---------|--|
| High Level Output Voltage | V_{OH} | 2.5 | 3.4 | | V | $V_{CC} = \text{MIN}, I_{OH} = \text{MAX}$ $V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$ |
| Low Level Output Voltage | V_{OL} | | 0.35 | 0.5 | V | $V_{CC} = \text{MIN}, I_{OL} = \text{MAX}$ $V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$ |
| High Level Output Current | I_{OH} | | | -1.0 | mA | |
| Low Level Output Current | I_{OL} | | | 20.0 | mA | |
| High Level Input Voltage | V_{IH} | 2.0 | | | V | |
| Low Level Input Voltage | V_{IL} | | | 0.8 | V | |
| Input Clamp Voltage | V_{IK} | | | -1.2 | V | $V_{CC} = \text{MIN}, I_I = I_{IK}$ |
| Input Current at Maximum Input Voltage | I_{IHH} | | | 0.1 | mA | $V_{CC} = \text{MAX}, V_I = 7.0V$ |
| High Level Input Current | I_{IH} | | | 20 | μA | $V_{CC} = \text{MAX}, V_I = 2.7V$ |
| Low Level Input Current | I_{IL} | | | -0.6 | mA | $V_{CC} = \text{MAX}, V_I = 0.5V$ |
| Short-circuit Output Current | I_{OS} | -60 | | -150 | mA | $V_{CC} = \text{MAX}$ |
| Output High Fan-out | | | | 25 | Unit | |
| Output Low Fan-out | | | | 12.5 | Load | |

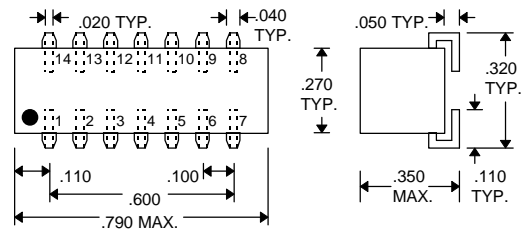
PACKAGE DIMENSIONS



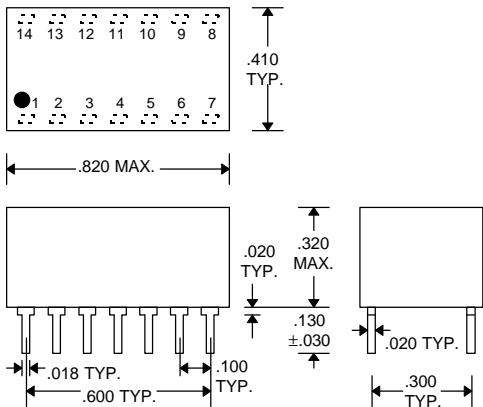
Commercial DIP (PDU13F-xx)



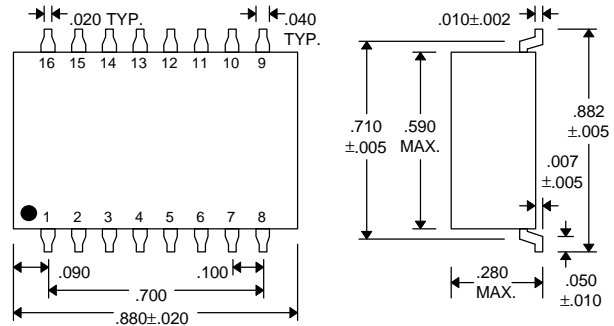
Commercial Gull-Wing (PDU13F-xxA2)



Commercial J-Lead (PDU13F-xxB2)



Military DIP (PDU13F-xxM)



Military Gull-Wing (PDU13F-xxMC3)

DELAY LINE AUTOMATED TESTING

TEST CONDITIONS

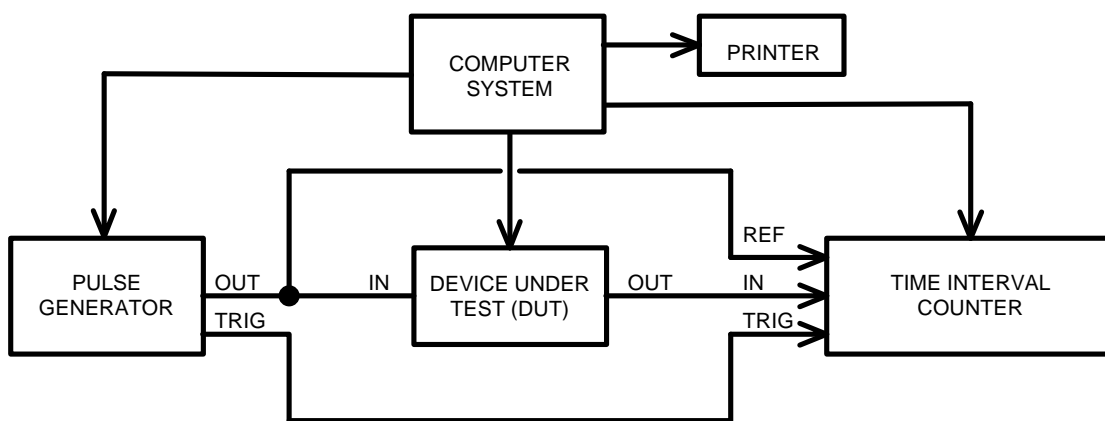
INPUT:

Ambient Temperature: $25^{\circ}\text{C} \pm 3^{\circ}\text{C}$
Supply Voltage (Vcc): $5.0\text{V} \pm 0.1\text{V}$
Input Pulse: High = $3.0\text{V} \pm 0.1\text{V}$
 Low = $0.0\text{V} \pm 0.1\text{V}$
Source Impedance: 50Ω Max.
Rise/Fall Time: 3.0 ns Max. (measured between 0.6V and 2.4V)
Pulse Width: $PW_{IN} = 1.5 \times \text{Total Delay}$
Period: $PER_{IN} = 4.5 \times \text{Total Delay}$

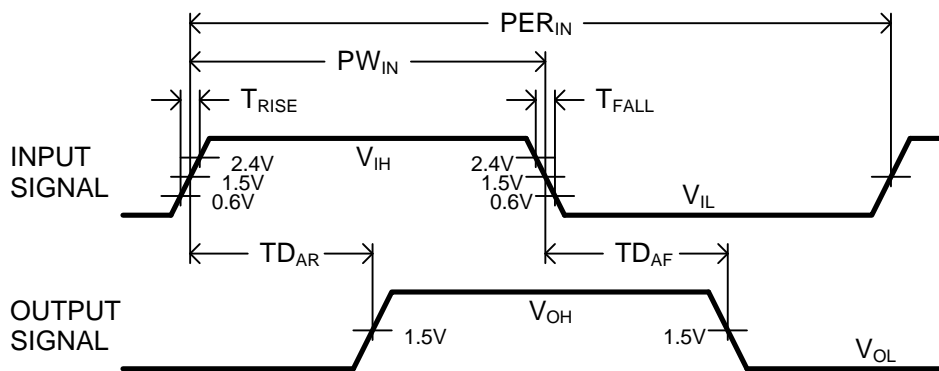
OUTPUT:

Load: 1 FAST-TTL Gate
C_{load}: $5\text{pf} \pm 10\%$
Threshold: 1.5V (Rising & Falling)

NOTE: The above conditions are for test only and do not in any way restrict the operation of the device.



Test Setup



Timing Diagram For Testing