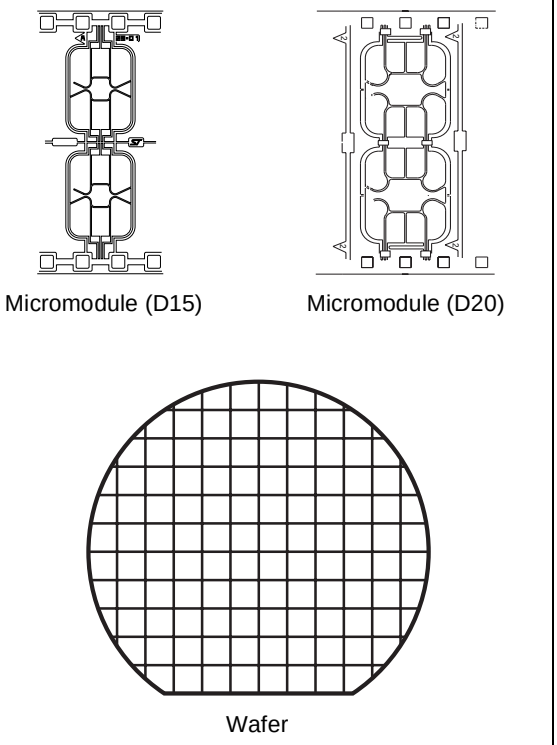
ST14C02C

Memory Card IC
2 Kbit (256 x 8) Serial I2C Bus EEPROM

- Single Supply Voltage (3 V to 5.5 V)
- Two Wire I^2C Serial Interface
- BYTE and MULTBYTE WRITE (up to 4 Bytes)
- PAGE WRITE (up to 8 Bytes)
- BYTE, RANDOM and SEQUENTIAL READ Modes
- Self-Timed Programming Cycle
- Automatic Address Incrementing
- Enhanced ESD/Latch-Up Behavior
- 1 Million Erase/Write Cycles (minimum)
- 10 Year Data Retention (minimum)



DESCRIPTION

This device is an electrically erasable programmable memory (EEPROM) fabricated with STMicroelectronics's High Endurance, Advanced Polysilicon, CMOS technology. This guarantees an endurance typically well above one million Erase/Write cycles, with a data retention of 10 years. The memory operates with a power supply as low as 3 V.

The device is available in wafer form (either sawn or unsawn) and in micromodule form (on film).

The memory is compatible with the I^2C standard. This is a two wire serial interface that uses a bi-directional data bus and serial clock. The memory carries a built-in 7-bit unique Device Type Identifier code (1010000) in accordance with the I^2C bus definition. Only one memory can be attached to each I^2C bus.

Figure 1. Logic Diagram

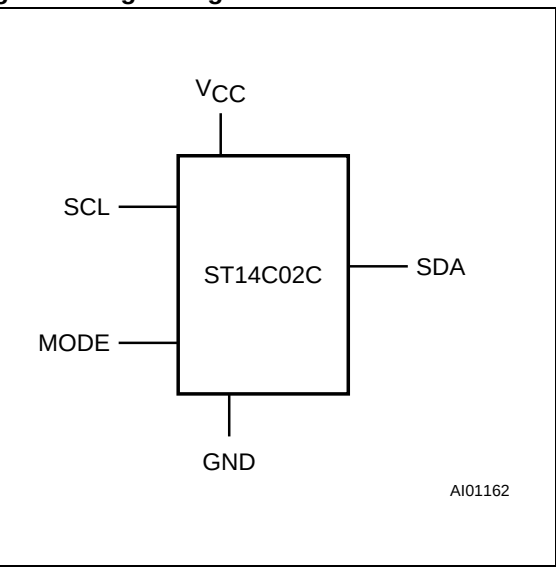


Table 1. Signal Names

SDA	Serial Data/Address Input/ Output
SCL	Serial Clock
MODE	Write Mode
V_{CC}	Supply Voltage
GND	Ground

Figure 2. D15 Contact Connections

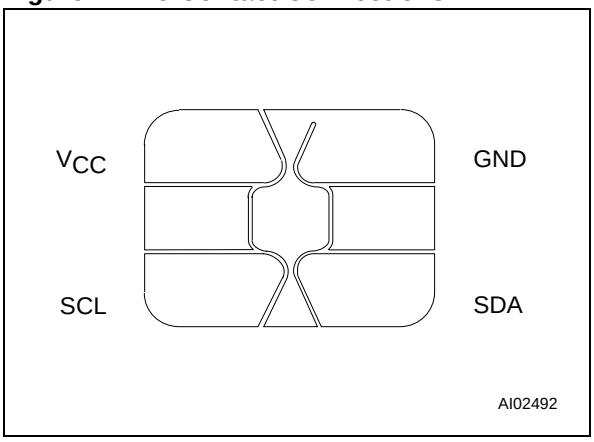
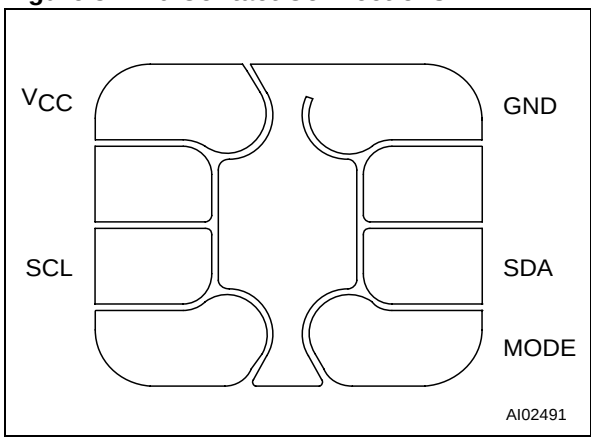


Figure 3. D20 Contact Connections



The memory behaves as a slave device in the I^2C protocol, with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition, generated by the bus master. The START condition is followed by the Device Select Code which is composed of a stream of 7 bits (1010000), plus one read/write bit ($R/\overline{W}$) and is terminated by an acknowledge bit.

When writing data to the memory, the memory inserts an acknowledge bit during the 9^{th} bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a STOP condition after an Ack for WRITE, and after a NoACK for READ.

Power On Reset: V_{CC} Lock-Out Write Protect

In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is included. The internal reset is held active until the V_{CC} voltage has reached the POR threshold value, and all operations are disabled – the device will not respond to any command. In the same way, when V_{CC} drops from the operating voltage, below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable and valid V_{CC} must be applied before applying any logic signal.

Table 2. Absolute Maximum Ratings [1]

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature		0 to 70	°C
T_{STG}	Storage Temperature	Wafer form Module form	-65 to 150 -40 to 120	°C
V_{IO}	Input or Output range		-0.3 to 6.5	V
V_{CC}	Supply Voltage		-0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) [2]		4000	V
	Electrostatic Discharge Voltage (Machine model) [3]		500	V

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the ST SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100 pF, 1500 Ω)
3. EIAJ IC-121 (Condition C) (200 pF, 0 Ω)

Table 3. Endurance and Data Retention

Device	Endurance (Erase/Write Cycles)	Data Retention (Years)
ST14C02C	1,000,000	10

SIGNAL DESCRIPTION

Serial Clock (SCL)

The SCL input pin is used to synchronize all data in and out of the memory. A pull up resistor can be connected from the SCL line to V_{CC}. (Figure 4 indicates how the value of the pull-up resistor can be calculated).

Serial Data (SDA)

The SDA pin is bi-directional, and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull up resistor must be connected from the SDA bus to V_{CC}. (Figure 4 indicates how the value of the pull-up resistor can be calculated).

Mode (MODE)

The MODE input may be driven dynamically. It must be held at:

- V_{IL} or V_{IH} for the Byte Write mode
- V_{IH} for Multibyte Write mode
- V_{IL} for Page Write mode

When unconnected, the MODE input is internally read as a V_{IH} (Multibyte Write mode). Note that the voltages are CMOS levels, and are not TTL compatible.

On the D15 micromodule, the MODE pin is not connected to a contact. This pin is left floating on the silicon. This type of ST14C02C is always in its MultiByte mode, and cannot be changed from this.

DEVICE OPERATION

The memory device supports the I^2C protocol, as summarized in Figure 5. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the master, and the other as the slave. A data transfer can only be initiated by the master, which will also provide the serial clock for synchronization. The memory device is always a slave device in all communication.

Figure 4. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I^2C Bus

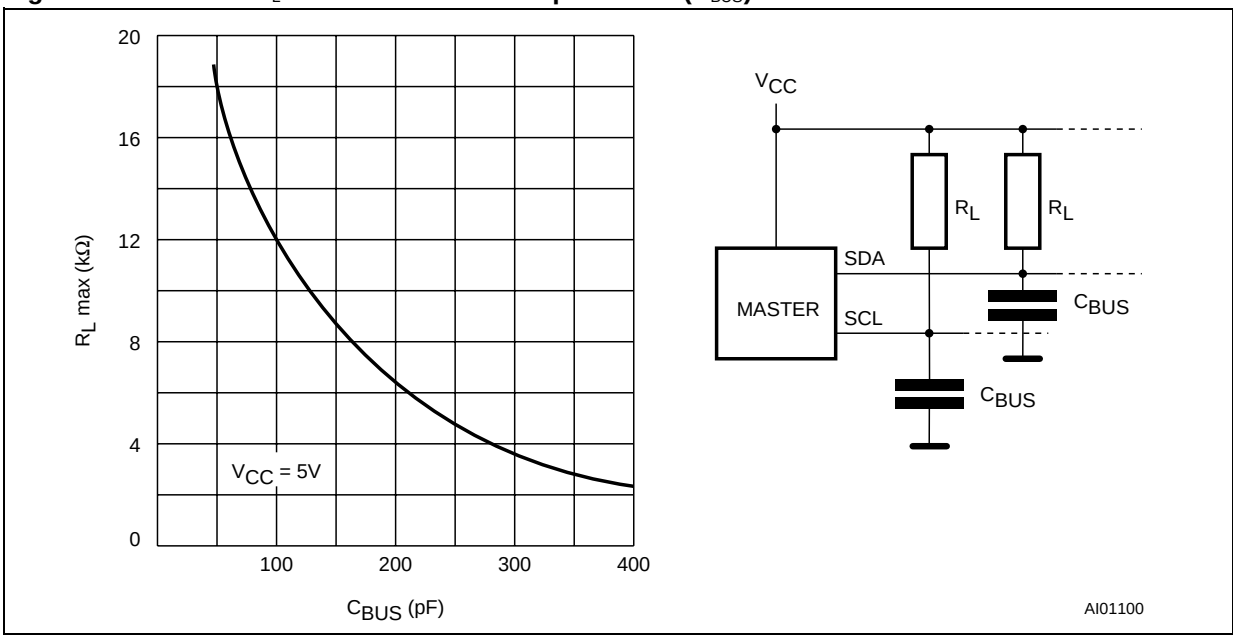
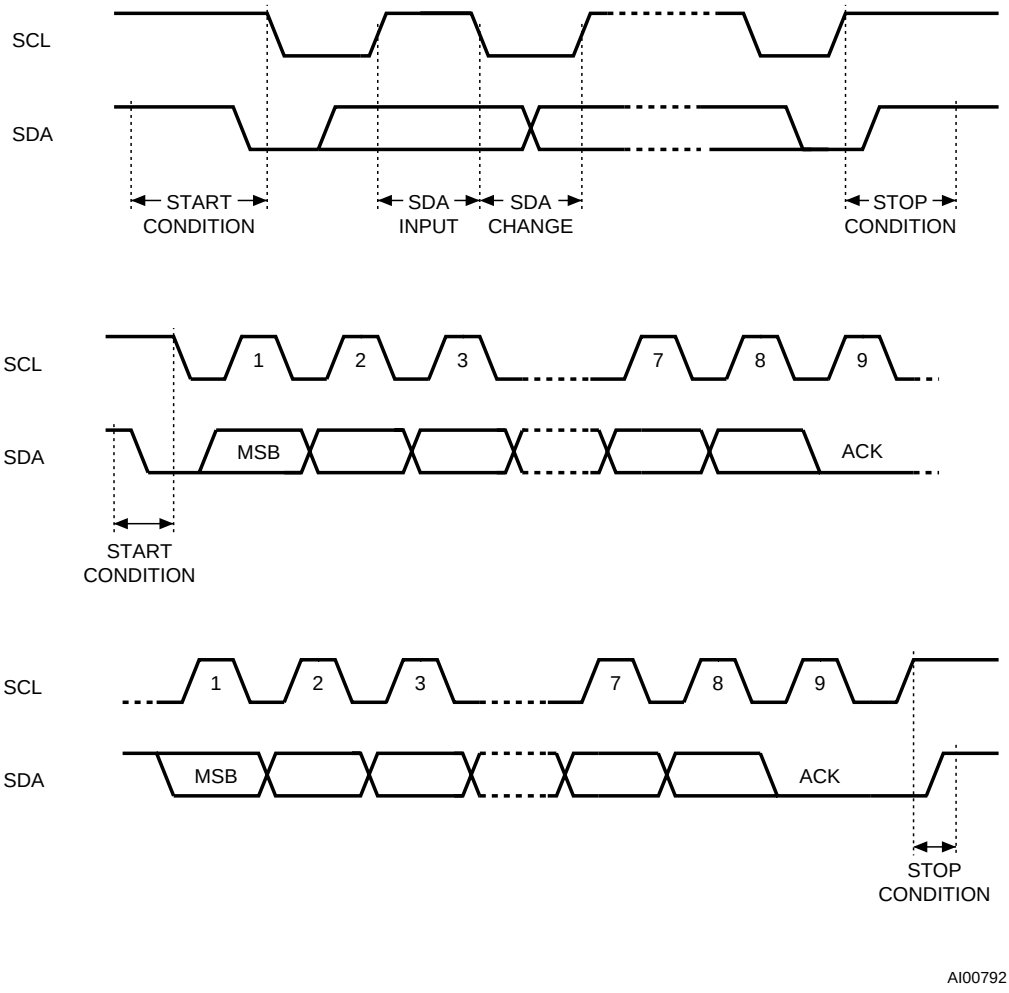


Figure 5. I²C Bus Protocol



Start Condition

START is identified by a high to low transition of the SDA line while the clock, SCL, is stable in the high state. A START condition must precede any data transfer command. The memory continuously monitors (except during a programming cycle) the SDA and SCL lines for a START condition, and will not respond unless one is given.

Stop Condition

STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the memory and the bus master. A STOP condition at the end of a Read command forces the memory device into its standby state. A STOP condition at the end of a Write command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK)

An acknowledge signal is used to indicate a successful data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data. During the 9th clock pulse

Table 4. Device Select Code [1]

	Device Code							$R\overline{W}$
	b7	b6	b5	b4	b3	b2	b1	b0
Device Select	1	0	1	0	0	0	0	$R\overline{W}$

Note: 1. The most significant bit, b7, is sent first.

period the receiver pulls the SDA bus low to acknowledge the receipt of the 8 data bits.

Data Input

During data input, the memory device samples the SDA bus signal on the rising edge of the clock, SCL. For correct device operation, the SDA signal must be stable during the clock low-to-high transition, and the data must change *only* when the SCL line is low.

Memory Addressing

To start communication between the bus master and the slave memory, the master must initiate a START condition. Following this, the master sends 8 bits to the SDA bus line (with the most significant bit first). These bits represent the Device Select Code (7 bits) and a $R\overline{W}$ bit.

The seven most significant bits of the Device Select Code are the Device Type Identifier, according to the I^2C bus definition. For the memory device, the seven bits are fixed at 1010000b (A0h), as shown in Table 4.

The 8^{th} bit is the read or write bit ($R\overline{W}$). This bit is set to '1' for read and '0' for write operations. If a match occurs on the Device Select Code, the corresponding memory gives an acknowledgment on the SDA bus during the 9^{th} bit time.

Write Operations

The Multibyte Write mode is selected when the MODE pin is at V_{IH}, and the Page Write mode is selected when MODE pin is at V_{IL}. The MODE pin may be driven dynamically to CMOS input levels.

Following a START condition, the master sends a Device Select Code with the $R\overline{W}$ bit reset to '0'. The memory device acknowledges this, and waits for a byte address. The 8-bit byte address allows access within a 256-byte memory address-space. After receipt of the byte address, the device again responds with an acknowledge bit.

Byte Write

In the Byte Write mode, the master sends one data byte, which is acknowledged by the memory, as shown in Figure 6. The master then terminates the transfer by generating a STOP condition. The Write mode is independent of the state of the MODE pin, as shown in Table 5, which could be left floating if only this mode is to be used. However this is not a recommended operating mode, as this pin has to be connected to either V_{IH} or V_{IL} to minimize the stand-by current.

Multibyte Write

For the Multibyte Write mode, the MODE pin must be held at V_{IH}, as shown in Table 5. The Multibyte Write mode can be started from any address in the memory. The master sends one, two, three or four bytes of data, which are each acknowledged by the memory. The transfer is terminated by the master generating a STOP condition. The maximum duration of the write cycle is t_W=10 ms (as shown in Table 8), except when bytes span across two rows. (That is, when they have different values for the 6 most significant address bits, A7-A2). The programming time is then doubled to a maximum of 20 ms. Writing more than four bytes in the Multi-

Figure 6. Write Mode Sequences

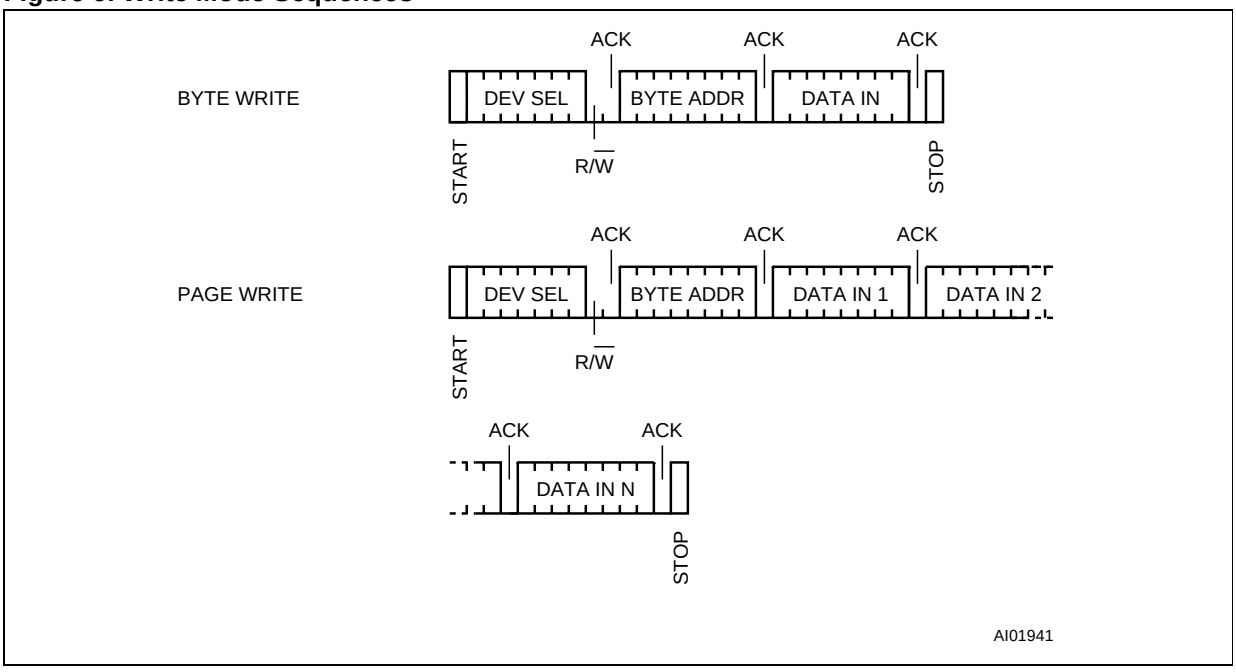


Table 5. Operating Modes

Mode	R$\overline{W}$ bit	MODE [1]	Bytes	Initial Sequence
Current Address Read	'1'	X	1	START, Device Select, R$\overline{W}$ = '1'
Random Address Read	'0'	X		START, Device Select, R$\overline{W}$ = '0', Address
	'1'	X	1	reSTART, Device Select, R$\overline{W}$ = '1'
Sequential Read	'1'	X	≥ 1	Similar to Current or Random Mode
Byte Write	'0'	X	1	START, Device Select, R$\overline{W}$ = '0'
Multibyte Write	'0'	V_{IH}	≤ 4	START, Device Select, R$\overline{W}$ = '0'
Page Write	'0'	V_{IL}	≤ 8	START, Device Select, R$\overline{W}$ = '0'

Note: 1. X = V_{IH} or V_{IL}.

byte Write mode may modify data bytes in an adjacent row. (Each row is 8 bytes long). However, the Multibyte Write can properly write up to eight consecutive bytes only if the first address is the first address of the row (the seven following bytes thereby being written to the seven following bytes of this same row).

When not connected, the MODE pin is internally pulled to "1" and the multibyte write option is selected.

Page Write

For the Page Write mode, the MODE pin must be held at V_{IL} (as shown in Table 5). The Page Write mode allows up to eight bytes to be written in a single write cycle, provided that they are all located in the same row. That is, the five most significant memory address bits (A7-A3) must be the same. The master sends between one and eight bytes of data, each of which are acknowledged by the memory. After each byte is transferred, the internal byte address counter is incremented (this handles the three least significant address bits). Care must be taken to avoid address counter 'roll-over', as this could result in data being overwritten.

The transfer is terminated by the master generating a STOP condition. For any write mode, the generation by the master of the STOP condition starts the internal memory program cycle. All inputs are disabled until the completion of this cycle and the memory will not respond to any request.

Minimizing System Delays by Polling On ACK

During the internal write cycle, the memory disconnects itself from the bus, and copies the data from its internal latches to the memory cells. The maximum write time (t_W) is indicated in Table 8, but the typical time is shorter. To make use of this, an ACK polling sequence can be used by the master.

The sequence, as shown in Figure 7, is as follows:

– Initial condition: a Write is in progress.
– Step 1: the master issues a START condition followed by a device select byte (first byte of the new instruction).
– Step 2: if the memory is busy with the internal write cycle, no ACK will be returned and the master goes back to Step 1. If the memory has terminated the internal write cycle, it responds with an ACK, indicating that the memory is ready to receive the second part of the next instruction (the first byte of this instruction having been sent during Step 1).

Read Operations

Read operations are independent of the state of the MODE pin. On delivery, the memory content is set at all "1's" (FFh).

Current Address Read

The memory has an internal byte address counter. Each time a byte is read, this counter is incremented. For the Current Address Read mode, following a START condition, the master sends a device select with the R$\overline{W}$ bit set to '1'. The memory device acknowledges this, and outputs the byte addressed by the internal byte address counter, as shown in Figure 9. The counter is then incremented. The master must *not* acknowledge the byte output, and terminates the transfer with a STOP condition.

Random Address Read

A dummy write is performed to load the address into the address counter, as shown in Figure 6. This is followed by another START condition from the master and the device select is repeated with the R$\overline{W}$ bit set to '1'. The memory device acknowledges this, and outputs the byte addressed. The master must *not* acknowledge the byte output, and terminates the transfer with a STOP condition.

Figure 7. Write Cycle Polling Flowchart using ACK

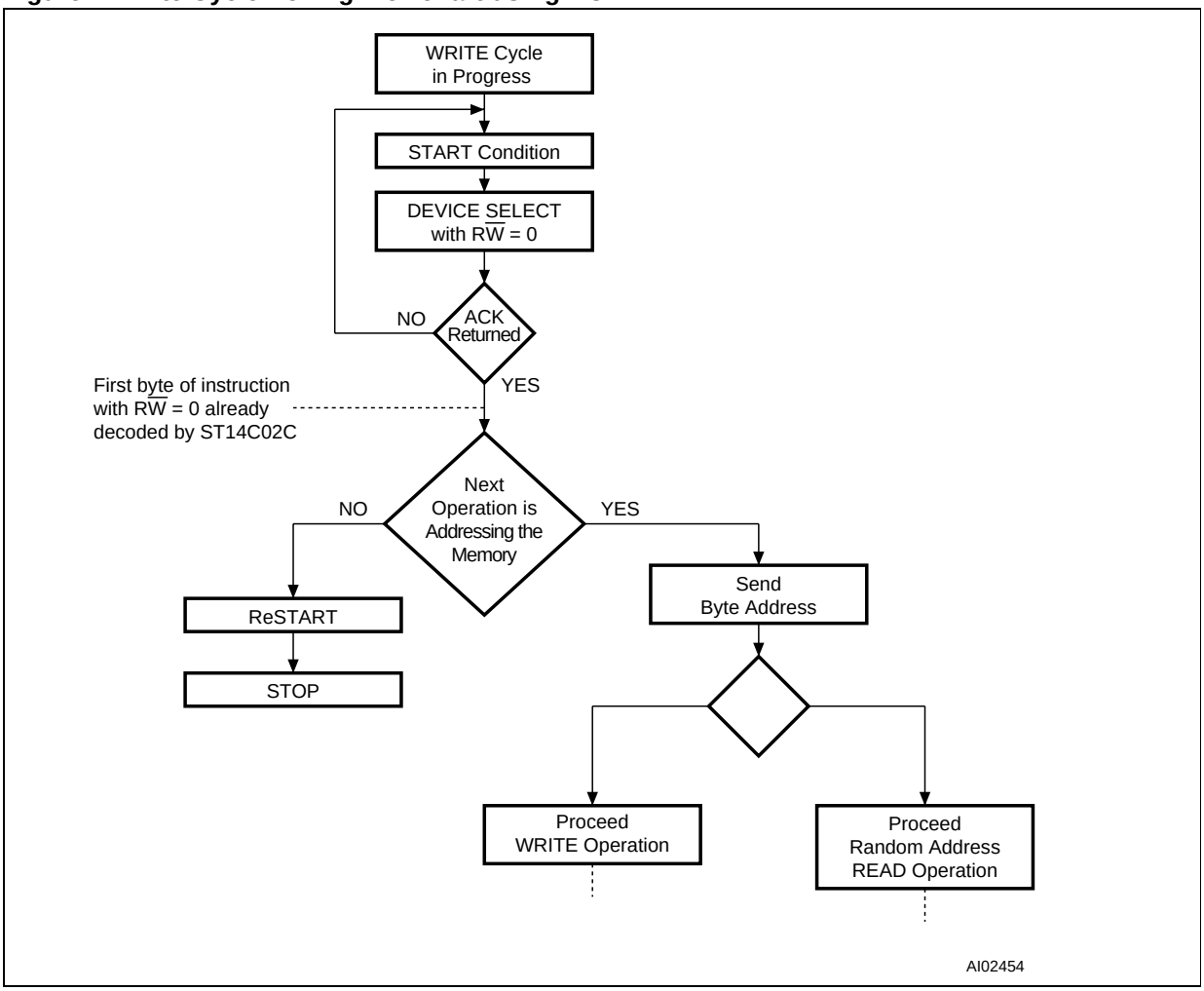


Table 6. AC Measurement Conditions

Input Rise and Fall Times	≤ 20 ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$

Figure 8. AC Testing Input/Output Waveform

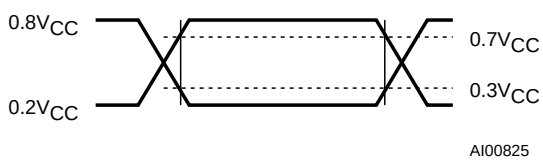
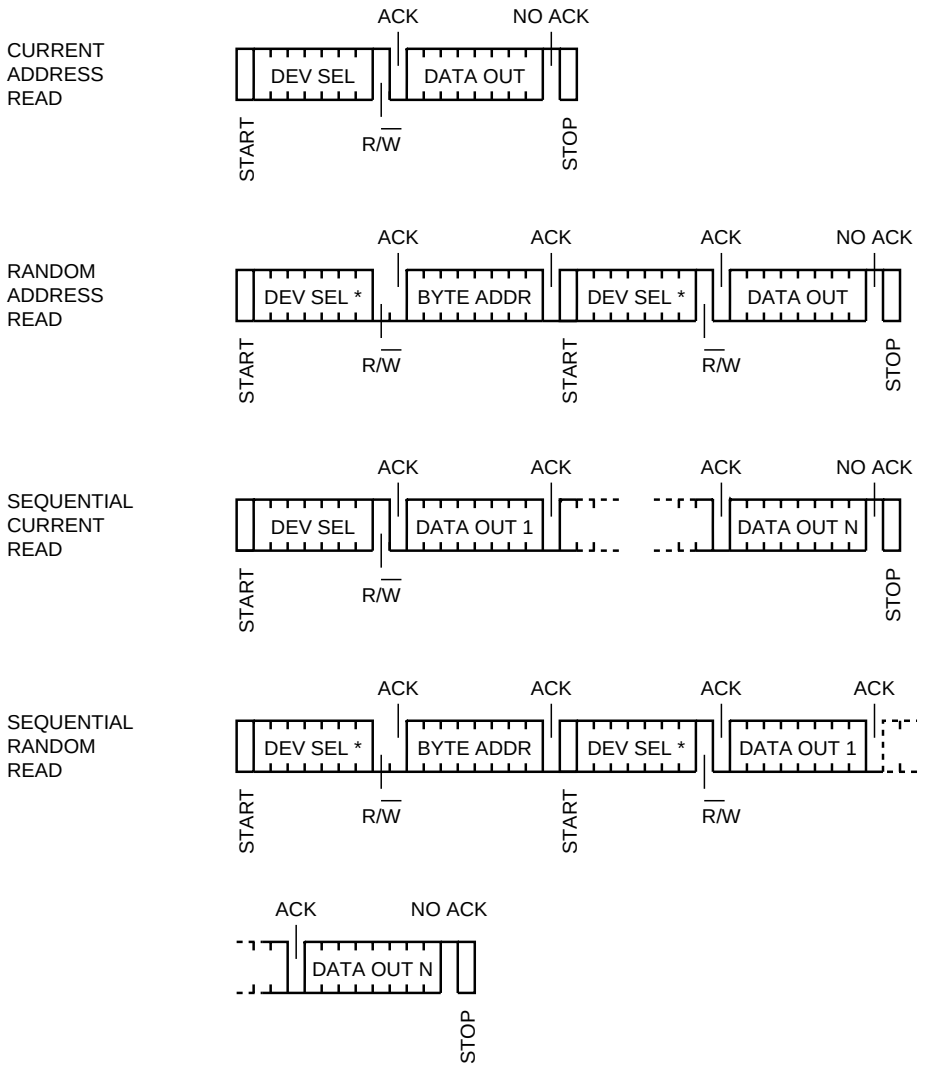


Table 7. Capacitance [1] (T_A = 25 °C, f = 100 kHz)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
t_{NS}	Noise suppression Time Constant (SCL & SDA Inputs)		100	400	ns

Note: 1. Sampled only, not 100% tested.

Figure 9. Read Mode Sequences



Sequential Read

This mode can be initiated with either a Current Address Read or a Random Address Read. However, in this case the master *does* acknowledge the data byte output, and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must *not* acknowledge the last byte output, and *must* generate a STOP condition. The output data comes from consecutive byte addresses, with the internal byte address counter automatically incremented after each byte output. After the last memory address, the address counter will 'roll-over' and the memory will continue to output data from the start of the memory block.

Acknowledge in Read Mode

In all read modes the memory waits for an acknowledgment during the 9th bit time. If the master does not pull the SDA line low during this time, the memory device terminates the data transfer and switches to its standby state.

Table 8. AC Characteristics
(T_A = 0 to 70 °C; V_{CC} = 3 V to 5.5 V)

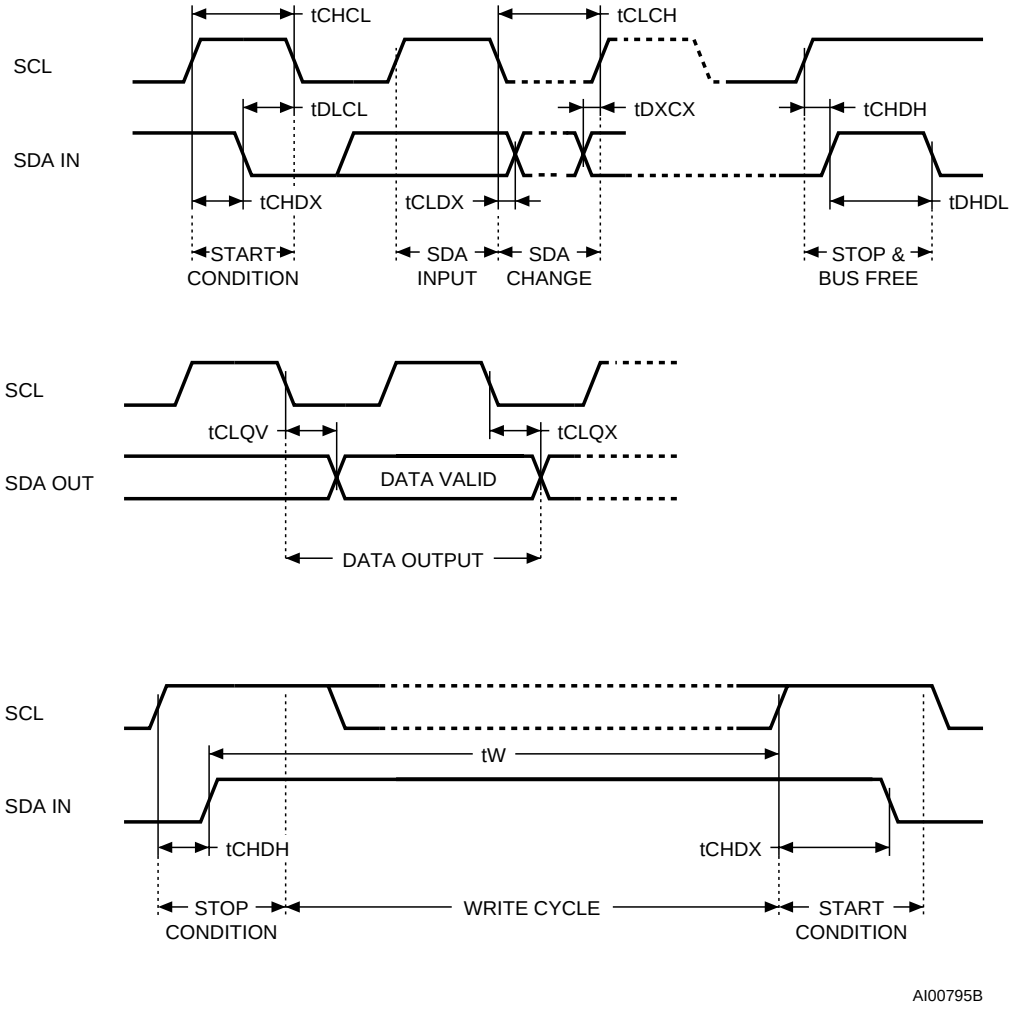
Symbol	Alt.	Parameter	ST14C02C		Unit
			Min	Max	
t_{CH1CH2}	t_R	Clock Rise Time		1	µs
t_{CL1CL2}	t_F	Clock Fall Time		300	ns
t_{DH1DH2}	t_R	SDA Rise Time		1	µs
t_{DL1DL2}	t_F	SDA Fall Time		300	ns
t_{CHDX} [1]	$t_{SU:STA}$	Clock High to Input Transition	4.7		µs
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	4		µs
t_{DLCL}	$t_{HD:STA}$	Input Low to Clock Low (START)	4		µs
t_{CLDX}	$t_{HD:DAT}$	Clock Low to Input Transition	0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	4.7		µs
t_{DXCX}	$t_{SU:DAT}$	Input Transition to Clock Transition	250		ns
t_{CHDH}	$t_{SU:STO}$	Clock High to Input High (STOP)	4.0		µs
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	4.7		µs
t_{CLQV}	t_{AA}	Clock Low to Data Out Valid		3.5	µs
t_{CLQX}	t_{DH}	Data Out Hold Time After Clock Low	300		ns
f_C	f_{SCL}	Clock Frequency		100	kHz
t_W [2]	t_{WR}	Write Time		10	ms

Note: 1. For a reSTART condition, or following a write cycle.
2. In the Multibyte Write mode only, if the accessed bytes span over two consecutive 8-byte rows (that is, if the 6 most significant address bits are not constant) the maximum programming time is doubled to 20 ms

Table 9. DC Characteristics
(T_A = 0 to 70 °C; V_{CC} = 3 V to 5.5 V)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$0 V \le V_{IN} \le V_{CC}$		± 2	µA
I_{LI}	Input Leakage Current (MODE pad)	$0 V \le V_{IN} \le V_{CC}$		± 10	µA
I_{LO}	Output Leakage Current	$0 V \le V_{OUT} \le V_{CC}$, SDA in Hi-Z		± 2	µA
I_{CC}	Supply Current	V_{CC} = 5 V, f_c = 100 kHz (Rise/Fall time < 10 ns)		2	mA
I_{CC1}	Supply Current (Stand-by)	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5 V		100	µA
V_{IL}	Input Low Voltage (SCL, SDA)		- 0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage (SCL, SDA)		0.7 V_{CC}	V_{CC} + 1	V
V_{IL}	Input Low Voltage (MODE)		- 0.3	0.5	V
V_{IH}	Input High Voltage (MODE)		V_{CC} - 0.5	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA, V_{CC} = 5 V		0.4	V

Figure 10. AC Waveforms



ORDERING INFORMATION

Devices are shipped from the factory with the memory content set at all '1's (FFh).

The notation used for the device number is as shown in Table 10. For a list of available options (speed, package, etc...) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

Sawn wafers are scribed and mounted in a frame on adhesive tape. The orientation is defined by the position of the GND pad on the die, viewed with active area of product visible, relative to the notches of the frame (as shown in Figure 11). The orientation of the die with respect to the plastic frame notches is specified by the Customer.

One further concern, when specifying devices to be delivered in this form, is that wafers mounted on adhesive tape must be used within a limited period from the mounting date:

– two months, if wafers are stored at 25°C, 55% relative humidity
– six months, if wafers are stored at 4°C, 55% relative humidity

Table 10. Ordering Information Scheme

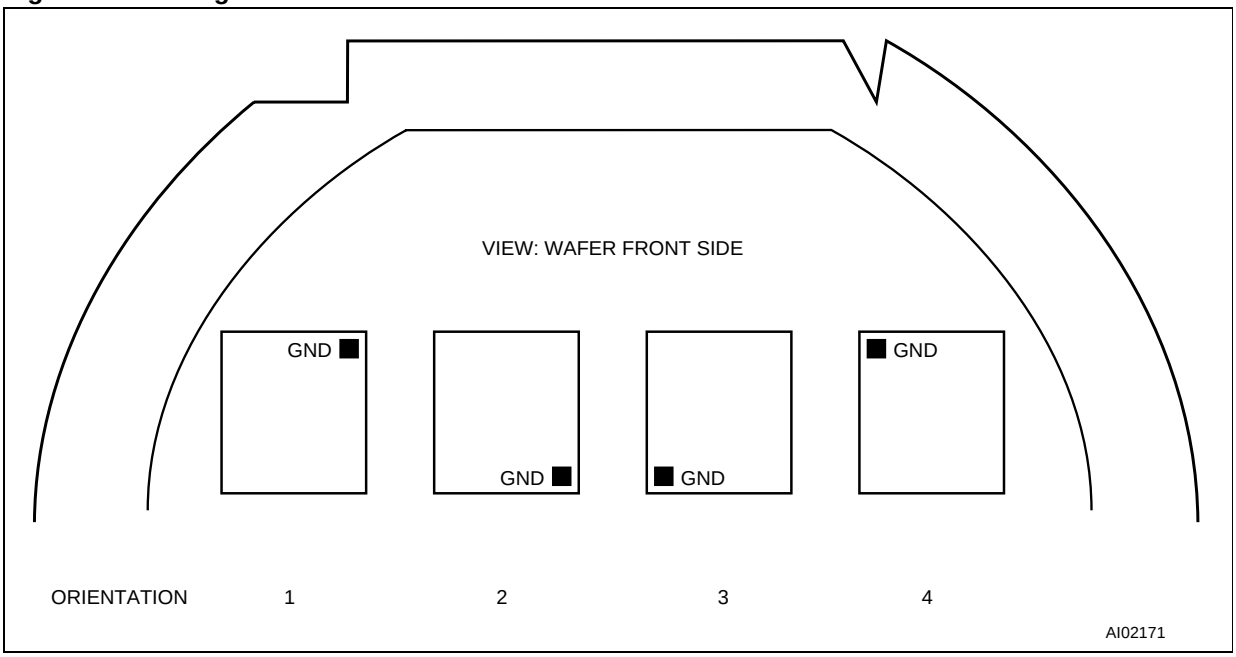
Example: ST14C02C - D20

Delivery Form	
D15	Module on Super 35 mm film
D20	Module on Super 35 mm film
W2	Unsawn wafer (275 µm ± 25 µm thickness)
W4	Unsawn wafer (180 µm ± 15 µm thickness)
S2x	Sawn wafer (275 µm ± 25 µm thickness)
S4x	Sawn wafer (180 µm ± 15 µm thickness)

where “x” indicates the sawing orientation, as follows (and as shown in Figure 11)

1	GND at top right
2	GND at bottom right
3	GND at bottom left
4	GND at top left

Figure 11. Sawing Orientation



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