- **Single Power Supply Supports 5-V ±10% Read/Write Operation**
- **Organization: . . . 262144 By 8 Bits**
- **Array-Blocking Architecture**
  - **One 16K-Byte Protected-Boot Sector**
  - **Two 8K-Byte Parameter-Sectors**
  - **One 32K-Byte Sector**
  - **Three 64K-Byte Sectors**
  - **Any Combination of Sectors Can Be Erased. Supports Full-Chip Erase**
  - **Any Combination of Sectors Can Be Marked as Read-Only**
- **Boot-Code Sector Architecture**
  - **T = Top Sector**
  - **B = Bottom Sector**
- **Sector Protection**
  - **Hardware Protection Method That Disables Any Combination of Sectors From Write or Erase Operations Using Standard Programming Equipment**
- **Embedded Program/Erase Algorithms**
  - **Automatically Pre-Programs and Erases Any Sector**
  - **Automatically Programs and Verifies the Program Data at Specified Address**
- **JEDEC Standards**
  - **Compatible With JEDEC Byte Pinouts**
  - **Compatible With JEDEC EEPROM Command Set**
- **Fully Automated On-Chip Erase and Program Operations**
- **100 000 Program/Erase Cycles**
- **Low Power Dissipation**
- **Low Current Consumption**
  - **40-mA Typical Active Read**
  - **60-mA Typical Program/Erase Current**
  - **Less Than 100-μA Standby Current**
- **All Inputs/Outputs TTL-Compatible**
- **Erase Suspend/Resume**
  - **Supports Reading Data From, or Programming Data to, a Sector Not Being Erased**
- **40-Pin Thin Small Outline Package (TSOP) (DCD Suffix)**
- **Detection Of Program/Erase Operation**
  - **Data Polling and Toggle Bit Feature of Program/Erase Cycle Completion**
- **High-Speed Data Access at 5-V V_{CC} ±10%**
  - **70 Commercial . . . 0°C to 70°C**
  - **80 Extended . . . –40°C to 85°C**

PIN NOMENCLATURE	
A0 – A17	Address Inputs
DQ0 – DQ7	Data In / Data out
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
NC	No Internal Connection
V_{CC}	Power Supply
V_{SS}	Ground
$\overline{WE}$	Write Enable

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description

The TMS29F002T/B is a 262144 by 8-bit (2097152-bit), 5-V single-supply, programmable read-only memory device that can be electrically erased and reprogrammed. This device is organized as 262144 x 8 bits, divided into seven sectors:

– One 16K-byte protected-boot sector

– Two 8K-byte sectors

– One 32K-byte sector

– Three 64K-byte sectors

Any combination of sectors can be marked as read-only or erased. Full chip erasure is also supported.

Sector data protection is afforded by methods that can disable any combination of sectors from write or read operations using standard programming equipment. An on-chip state machine provides an on-board algorithm that automatically pre-programs and erases any sector before it automatically programs and verifies program data at any specified address. The command set is compatible with that of the Joint Electronic Device Engineering Council (JEDEC) standards and is compatible with the JEDEC 2M-byte electrically erasable programmable read-only memory (EEPROM) command set. A suspend/resume feature allows access to

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description (continued)

unaltered memory blocks during a section-erase operation. All outputs of this device are TTL-compatible. Additionally, an erase/suspend/resume feature supports reading data from, or programming data to, a sector that is not being erased.

Device operations are selected by writing JEDEC-standard commands into the command register using standard microprocessor write timings. The command register acts as an input to an internal-state machine which interprets the commands, controls the erase and programming operations, outputs the status of the device, outputs data stored in the device, and outputs the device algorithm-selection code. On initial power up, the device defaults to the read mode.

The device has low power dissipation with a 40-mA active read for the byte mode, 60-mA typical program/erase current mode, and less than 100-µA standby current. These devices are offered with 70 and 80 ns access times. Table 1 and Table 2 show the sector-address ranges. The TMS29F002T/B is offered in a 40-pin (DCD suffix) thin small-outline package.

device symbol nomenclature

TMS29Fxxx T –90 C DCD L

Temperature Range
- L = Commercial (0°C to 70°C)
- E = Extended (–40°C to 85°C)

Package Type
- DCD = Thin Small-Outline Package

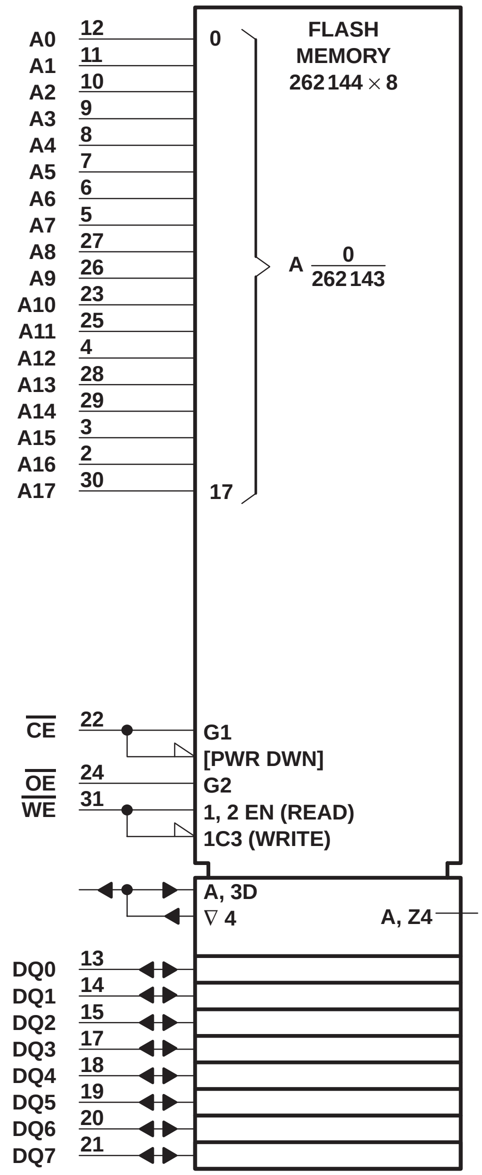
Program/Erase Endurance
- C = 100000 cyc
- B = 10000 cyc

Speed Option
- –70 = 70 ns
- –80 = 80 ns

Boot Code Selection Architecture
- T = Top Sector
- B = Bottom Sector

Device Number / Description
- xxx = 002
- 2M bit

logic symbol†



† This symbol is in accordance with ANSI / IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the FM package.

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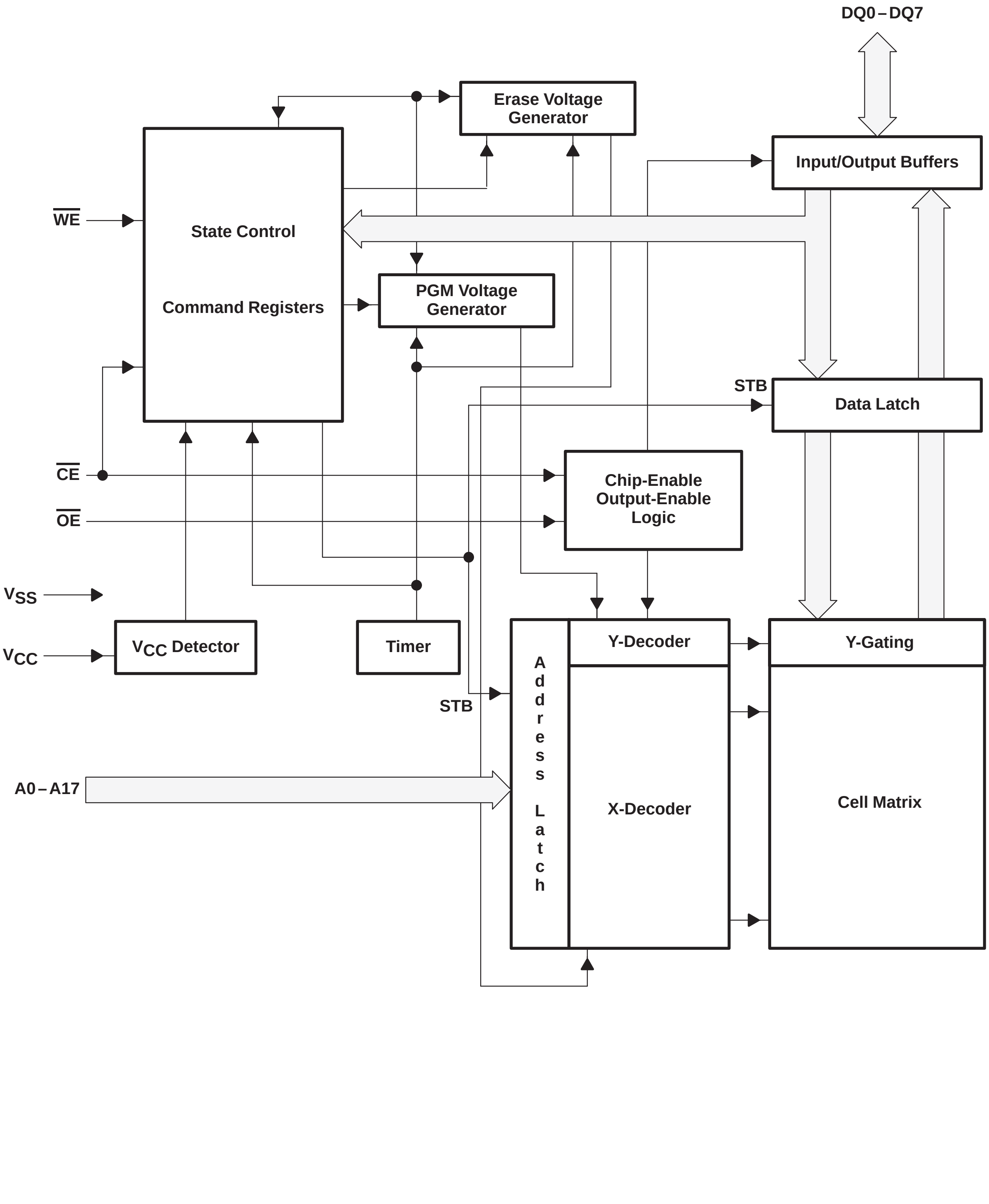
block diagram



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operation

See Table 1 and Table 2 for sector-address ranges of the TMS29F002T/B.

Table 1. Top-Boot Sector-Address Ranges†

	A17	A16	A15	A14	A13	SECTOR SIZE	ADDRESS RANGE
SA6	1	1	1	1	X	16K-Byte	30000H–3FFFFH
SA5	1	1	1	0	1	8K-Byte	3A000H–3BFFFH
SA4	1	1	1	0	0	8K-Byte	38000H–39FFFH
SA3	1	1	0	X	X	32K-Byte	30000H–37FFFH
SA2	1	0	X	X	X	64K-Byte	20000H–2FFFFH
SA1	0	1	X	X	X	64K-Byte	10000H–1FFFFH
SA0	0	0	0	X	X	64K-Byte	00000H–0FFFFH

† The address range is A17 – A0.

Table 2. Bottom-Boot Sector-Address Ranges†

	A17	A16	A15	A14	A13	SECTOR SIZE	ADDRESS RANGE
SA6	0	1	1	X	X	64K-Byte	30000H–3FFFFH
SA5	0	1	0	X	X	64K-Byte	20000H–2FFFFH
SA4	0	0	1	X	X	64K-Byte	10000H–1FFFFH
SA3	0	0	0	1	X	32K-Byte	08000H–0FFFFH
SA2	0	0	0	0	1	8K-Byte	06000H–07FFFH
SA1	0	0	0	0	1	8K-Byte	04000H–05FFFH
SA0	0	0	0	0	0	16K-Byte	00000H–03FFFH

† The address range is A17 – A0.

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operation (continued)

See Table 3 for operation modes of the TMS29F002T/B.

Table 3. Operation Mode

MODE	FUNCTIONS†							
	$\overline{CE}$	$\overline{OE}$‡	$\overline{WE}$	A0	A1	A6	A9	DQ0–DQ7
Algorithm-selection mode	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{ID}	Manufacturer-Equivalent Code 01H (TMS29F002)
5-V power supply	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{ID}	TBD
	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{ID}	TBD
Read	V_{IL}	V_{IL}	V_{IH}	A0	A1	A6	A9	Data out
Output disable	V_{IL}	V_{IH}	V_{IH}	X	X	X	X	Hi-Z
Standby and write inhibit	V_{IH}	X	X	X	X	X	X	Hi-Z
Write§	V_{IL}	V_{IH}	V_{IL}	A0	A1	A6	A9	Data in
Verify sector protect	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{ID}	Data out

Legend:
V_{IL} = Logic low
V_{IH} = Logic high
V_{ID} = 12.0 ± 0.5 V

† X can be V_{IL} or V_{IH}.
‡ If $\overline{OE}$ = V_{IL}, then $\overline{WE}$ can be V_{IL}. $\overline{OE}$ = V_{IH} permits write operations.
§ See Table 6 for valid address and data during write.

read mode

A logic-low signal applied to the $\overline{CE}$ and $\overline{OE}$ pins allows reading the output of the TMS29F002T/B . When two or more ’29F002T/B devices are connected in parallel, the output of any one device can be read without interference. The $\overline{CE}$ pin is for device selection. The $\overline{OE}$ pin gates the data output onto the bus from the selected device.

The address-access time (t_{AVQV}) is the delay from stable address to valid output data. The chip-enable ($\overline{CE}$) access time (t_{ELQV}) is the delay from $\overline{CE}$ low and stable addresses to valid output data. The output-enable access time (t_{GLQV}) is the delay from $\overline{OE}$ low to valid output data, when $\overline{CE}$ is low and addresses are stable for at least the duration of t_{AVQV}–t_{GLQV}.

standby mode

The I_{CC} supply current is reduced by applying a logic-high level on $\overline{CE}$ to enter the standby mode. In the standby mode, the outputs are placed in the high-impedance state. Applying a CMOS logic-high level on $\overline{CE}$ reduces the current to 60 µA. Applying a TTL logic-high level on $\overline{CE}$ reduces the current to 1 mA. If the ’29F002T/B is deselected during erasure or programming, the device continues to draw active current until the operation is complete.

output disable

When either $\overline{OE}$ or $\overline{CE}$ is high, output from the device is disabled and the output pins (DQ0–DQ7) are placed in the high-impedance state.

automatic sleep mode

The ’29F002 has a built-in feature called automatic sleep mode to minimize device energy consumption. The mode, which is independent of $\overline{CE}$, $\overline{WE}$, and $\overline{OE}$, is enabled when addresses remain stable for 300 ns. Typical sleep-mode current is 60 µA. Sleep mode does not affect output data, which remains latched and available to the system.

algorithm selection mode

The algorithm-selection mode provides access to a binary code that matches the device with its proper programming and erase command operations. This mode is activated when V_{ID} (11.5 V to 12.5 V) is placed on address pin A9. Address pins A1 and A6 must be logic low. Two bytes of code are accessed by toggling address pin A0 from V_{IL} to V_{IH}. Address pins other than A0, A1, and A6 can be at logic low or at logic high.

The algorithm-selection mode can also be read by using the command register, which is useful when V_{ID} is not available to be placed on address pin A9. Table 4 shows the binary algorithm-selection codes.

Table 4. Algorithm-Selection Codes (5-V Single Power Supply)†

	CODE	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Manufacturer equivalent code	01H	0	0	0	0	0	0	0	1
TMS29F002T	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
TMS29F008B	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
Sector protection	01H	0	0	0	0	0	0	0	1

† A1 = V_{IL}, A6 = V_{IL}, $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IL}

erasure and programming

Erasure and programming of the ’29F002 are accomplished by writing a sequence of commands using standard-microprocessor-write timings. The commands are written to a command register and input to the command-state machine. The command-state machine interprets the command entered and initiates program, erase, suspend, and resume operations as instructed. The command-state machine acts as the interface between the write-state machine and the external-chip operations. The write-state machine controls all voltage generation, pulse generation, preconditioning, and verification of the contents of the memory. Program and block-/chip-erase functions are fully automatic. Once the end of a program or erase operation is reached, the device resets internally to the read mode. If V_{CC} drops below the low-voltage-detect level, any programming or erase operation is aborted and subsequent writes are ignored until the V_{CC} level is greater than VLKO. The control pins must be correct logically to prevent unintentional command writes or programming or erasing.

command definitions

Device operating modes are selected by writing specific address and data sequences into the command register. Table 5 defines the valid command sequences. Writing incorrect address and data values or writing them in the incorrect sequence causes the device to reset to the read mode. The command register does not occupy an addressable memory location. The register stores the command sequence, along with the address and data needed by the memory array. Commands are written by setting $\overline{CE}$ low, $\overline{OE}$ high, and bringing $\overline{WE}$ from high to low. Addresses are latched on the falling edge of $\overline{WE}$ and data is latched on the rising edge of $\overline{WE}$. Holding $\overline{WE}$ low and toggling $\overline{CE}$ can be used as an alternative. See the switching characteristics of the write/erase/program-operations section for specific timing information.

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command definitions (continued)

Table 5. Command Definitions†

COMMAND	BUS CYCLES	1ST CYCLE ADDR	1ST CYCLE DATA	2ND CYCLE ADDR	2ND CYCLE DATA	3RD CYCLE ADDR	3RD CYCLE DATA	4TH CYCLE ADDR	4TH CYCLE DATA	5TH CYCLE ADDR	5TH CYCLE DATA	6TH CYCLE ADDR	6TH CYCLE DATA
Read/reset	1	XXXH	F0H										
Read/reset	3	555H	AAH	2AAH	55H	555H	F0H	RA	RD				
Algorithm selection	3	555H	AAH	2AAH	55H	555H	90H	01H	TBD TBD				
Program	4	555H	AAH	2AAH	55H	555H	A0H	PA	PD				
Chip erase	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
Sector erase	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA	30H
Sector-erase suspend	1	XXXH	B0H	Erase suspend valid during sector-erase operation									
Sector-erase resume	1	XXXH	30H	Erase resume valid only after erase suspend									

LEGEND:
- RA = Address of the location to be read
- PA = Address of the location to be programmed
- SA = Address of the sector to be erased
  Addresses A13:A17 select one to seven sectors.
- RD = Data to be read at selected address location
- PD = Data to be programmed at selected address location

† Unless otherwise noted, address bits A17 – A11 are don't care.

read/reset command

The read or reset mode is activated by writing either of the two read/reset command sequences into the command register. The device remains in this mode until one of the other valid command sequences is input in the command register. Memory data is available in the read mode and can be read with standard microprocessor read-cycle timing.

On power up, the device defaults to the read/reset mode. A read/reset command sequence is not required and memory data is available.

algorithm-selection command

The algorithm-selection command allows access to a binary code that matches the device with the proper programming and erase command operations. After writing the three-bus-cycle command sequence, the first byte of the algorithm-selection code can be read from address XX00h. The second byte of the code can be read from address XX01h (see Table 6). This mode remains in effect until another valid command sequence is written to the device.

program command

Programming is a four-bus-cycle command sequence. The first three bus cycles put the device into the program-setup state. The fourth bus cycle loads the address location and the data to be programmed into the device. The addresses are latched on the falling edge of $\overline{WE}$ and the data is latched on the rising edge of $\overline{WE}$ in the fourth bus cycle. The rising edge of $\overline{WE}$ starts the program operation. The embedded programming function automatically provides needed voltage and timing to program and to verify the cell margin. Any further commands written to the device during the program operation are ignored.

program command (continued)

Programming can be performed at any address location in any sequence. When erased, all bits are in a logic-high state. Logic lows are programmed into the device. Only an erase operation can change bits from logic lows to logic highs. Attempting to program a 1 into a bit that has been programmed previously to a 0 causes the internal-pulse counter to exceed the pulse-count limit, which sets the exceed-time-limit indicator (DQ5) to a logic-high state. The automatic-programming operation is complete when the data on (DQ7) is equivalent to the data written to this bit, at which time the device returns to the read mode and addresses are no longer latched. Figure 5 shows a flowchart of the typical device-programming operation.

chip-erase command

Chip erase is a six-bus-cycle command sequence. The first three bus cycles put the device into the erase-setup state. The next two bus cycles unlock the erase mode. The sixth bus cycle loads the chip-erase command. This command sequence is required to ensure that the memory contents are not erased accidentally. The rising edge of $\overline{WE}$ starts the chip-erase operation. Any further commands written to the device during the chip-erase operation are ignored.

The embedded chip-erase function automatically provides voltage and timing needed to program and to verify all the memory cells prior to electrical erase and then erases and verifies the cell margin automatically without programming the memory cells prior to erase.

Figure 8 shows a flow chart for the typical chip-erase device operation.

sector-erase command

Sector erase is a six-bus-cycle command sequence. The first three bus cycles cause the device to go into the erase-setup state. The next two bus cycles unlock the erase mode. The sixth bus cycle loads the sector-erase command and the sector-address location to be erased. Any address location within the desired sector can be used. The addresses are latched on the falling edge of $\overline{WE}$ and the sector-erase command (30h) is latched on the rising edge of $\overline{WE}$ in the sixth bus cycle. After a delay of 80 µs from the rising edge of $\overline{WE}$, the sector-erase operation begins on the selected sector(s).

Additional sectors can be selected to be erased concurrently during the sector-erase command sequence. For each additional sector to be selected for erase, another bus cycle is issued. The bus cycle loads the next sector-address location and the sector-erase command. The time between the end of the previous bus cycle and the start of the next bus cycle must be less than 100 µs, otherwise the new sector location is not loaded. A time delay of 100 µs from the rising edge of the last $\overline{WE}$ starts the sector-erase operation. If there is a falling edge of $\overline{WE}$ within the 100 µs time delay, the timer is reset.

One to seven sector-address locations can be loaded in any sequence. The state of the delay timer can be monitored using the sector-erase delay indicator (DQ3). If DQ3 is logic low, the time delay has not expired. See the operation status section for a description.

Any command other than erase suspend (B0h) or sector erase (30h) written to the device during the sector-erase operation causes the device to exit the sector-erase mode. The contents of the sector(s) selected for erase are not valid. To complete the sector-erase operation, the sector-erase command sequence must be repeated.

The embedded sector-erase function automatically provides needed voltage and timing to program and to verify all of the memory cells prior to electrical erase and then erases and verifies the cell margin automatically. Programming the memory cells prior to erase is not required.

See the operation status section for a full description. Figure 10 shows a flow chart for the typical sector-erase device operation.

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erase-suspend command

The erase-suspend command (B0h) allows interruption of a sector-erase operation to read data from unaltered sectors of the device. Erase-suspend is a one-bus-cycle command. The addresses can be low or high and the erase-suspend command (B0h) is latched on the rising edge of $\overline{WE}$. Once the sector-erase operation is in progress, the erase-suspend command requests the internal-write-state machine to halt operation at predetermined breakpoints. The erase-suspend command is valid only during the sector-erase operation and is invalid during programming and chip-erase operations. The sector-erase delay timer expires immediately if the erase-suspend command is issued while the delay is active.

After erase suspend is issued, the device takes between 0.1 µs and 15 µs to suspend the operation. The toggle bit must be monitored to determine when the suspend has been executed. When the toggle-bit stops toggling, data can be read from sectors that are not selected for erase. See the operation status section for a full description. Reading from a sector selected for erase can result in invalid data.

Once the sector-erase operation is suspended, reads or program to a sector not being erased can be performed. This command is applicable only during sector-erase operation. Any other command written during erase-suspend mode to the suspended sector is ignored.

erase-resume command

The erase-resume command (30h) restarts a suspended sector-erase operation from the point where it was halted. Erase resume is a one-bus-cycle command. The addresses can be V_{IL} or V_{IH} and the erase-resume command (30h) is latched on the rising edge of $\overline{WE}$. When an erase-suspend/erase-resume command combination is written, the internal-pulse counter (exceed timing limit) is reset. The erase-resume command is valid only in the erase-suspend state. After the erase-resume command is executed, the device returns to the valid sector-erase state and further writes of the erase-resume command are ignored. After the device has resumed the sector-erase operation, another erase-suspend command can be issued to the device.

operation status

The status of the device during an automatic-programming algorithm, chip-erase, or automatic-erase algorithm can be determined in three ways:

- DQ7: Data polling
- DQ6: Toggle bit

status-bit definitions

During operation of the automatic embedded program and erase functions, the status of the device can be determined by reading the data state of designated outputs. The data-polling bit (DQ7) and toggle bit (DQ6) require multiple successive reads to observe a change in the state of the designated output. Table 6 defines the values of the status flags.

status-bit definitions (continued)

Table 6. Operation Status Flags†

	DEVICE OPERATION‡		DQ7	DQ6	DQ5	DQ3	DQ2
In progress	Programming		$\overline{DQ7}$	T	0	0	No Tog
	Program/erase in auto-erase		0	T	0	1	§
	Erase-suspend mode	Erase-sector address	1	No Tog	0	0	T
		Non-erase sector address	D	D	D	D	D
	Program in erase suspend		$\overline{DQ7}$¶	T	0	0	1§
Exceeded time limits	Programming		$\overline{DQ7}$	T	1	0	No Tog
	Program/erase in auto erase		0	T	1	1	#
	Program in erase suspend		$\overline{DQ7}$	T	1	0	No Tog
Successful operation complete	Programming complete		D	D	D	D	D
	Sector/chip erase complete		1	1	1	1	1

† T= toggle, D= data, No Tog= no toggle
‡ DQ4, DQ1, DQ0 are reserved for future use.
§ DQ2 can be toggled when sector-address applied is an erasing sector. DQ2 cannot be toggled when the sector-address applied is a non-erasing sector. DQ2 is used to determine which sectors are erasing and which are not.
¶ Status flags apply when outputs are read from the address of a non-erase-suspend operation.
# If DQ5 is high (exceeded timing limits), successive reads from a problem sector causes DQ2 to toggle.

data-polling (DQ7)

The data-polling-status function outputs the complement of the data latched into the DQ7 data register while the write-state machine is engaged in a program or erase operation. Data bit DQ7 changing from complement to true indicates the end of an operation. Data-polling is available only during programming, chip-erase, sector-erase, and sector-erase-timing delay. Data-polling is valid after the rising edge of $\overline{WE}$ in the last bus cycle of the command sequence loaded into the command register. Figure 12 shows a flow chart for data-polling.

During a program operation, reading DQ7 outputs the complement of the DQ7 data to be programmed at the selected address location. Upon completion, reading DQ7 outputs the true DQ7 data loaded into the program-data register. During the erase operations, reading DQ7 outputs a logic low. Upon completion, reading DQ7 outputs a logic high. Also, data-polling must be performed at a sector address that is within a sector that is being erased. Otherwise, the status is invalid. When using data-polling, the address must remain stable throughout the operation.

During a data-polling read, while $\overline{OE}$ is logic low, data bit DQ7 can change asynchronously. Depending on the read timing, the system can read valid data on DQ7, while other DQ pins are still invalid. A subsequent read of the device is valid. See Figure 13 for the data-polling timing diagram.

toggle-bit (DQ6)

The toggle-bit status function outputs data on DQ6 which toggles between logic high and logic low while the write-state machine is engaged in a program or erase operation. When DQ6 stops toggling after two consecutive reads to the same address, the operation is complete. The toggle-bit is available only during programming, chip erase, sector erase, and sector-erase-timing delay. Toggle-bit data is valid after the rising edge of $\overline{WE}$ in the last bus cycle of the command sequence loaded into the command register. Figure 14 shows a flow chart for the toggle-bit-status-read algorithm. Depending on the read timing, DQ6 can stop toggling while other DQ pins are still invalid. A subsequent read of the device is valid.

exceed time limit (DQ5)

The program and erase operations use an internal-pulse counter to limit the number of pulses applied. If the pulse-count limit is exceeded, DQ5 is set to a logic-high data state, indicating that the program or erase operation has failed. DQ7 does not change from complemented data to true data and DQ6 does not stop toggling when read. To continue operation, the device must be reset.

This condition occurs when attempting to program a logic-high state into a bit that has been programmed previously to a logic low. Only an erase operation can change bits from logic low to logic high. After reset, the device is functional and can be erased and reprogrammed.

sector-load-timer (DQ3)

The sector-load-timer status bit, DQ3, is used to determine whether the time to load additional sector addresses has expired. After completion of a sector erase command sequence, DQ3 remains at a logic low for 100 µs. This indicates that another sector-erase command sequence can be issued. If DQ3 is at a logic high, it indicates that the delay has expired and attempts to issue additional sector-erase commands are ignored. See the sector-erase command section for a description.

The data-polling and toggle bit are valid during the 100-µs time delay and can be used to determine if a valid sector-erase command has been issued. To ensure additional sector-erase commands have been accepted, the status of DQ3 should be read before and after each additional sector-erase command. If DQ3 is at a logic low on both reads, the additional sector-erase command was accepted.

toggle bit 2 (DQ2)

The state of DQ2 determines whether the device is in algorithmic erase mode or erase-suspend mode. DQ2 toggles if successive reads are issued to the erasing or erase-suspended sector, assuming in case of the latter that the device is in erase suspend read mode. It also toggles when DQ5 becomes a logic high due to timer-exceed limit and reads are issued to the failed sector. DQ2 does not toggle in any other sector due to DQ5 fail. When the device is in erase-suspend program mode, successive reads from the non-erase-suspended sector causes a logic high on DQ2.

sector-protect programming

The sector-protect programming mode is activated when A6, A0, and $\overline{CE}$ at V_{IL}, and address pin A9 and control pin $\overline{OE}$ are forced to V_{ID}. Address pin A1 is set to V_{IH}.The sector-select-address pins A17 – A13 are used to select the sector to be protected. Address pins A12–A0 and I/O pins must be stable and can be either low or high. Once the addresses are stable, $\overline{WE}$ is pulsed low for 100 µs causing programming to begin on the falling edge of $\overline{WE}$ and terminate on the rising edge of $\overline{WE}$. Figure 16 is a flow chart of the sector-protect algorithm.

Commands to program or erase a protected sector do not change the data contained in the sector. Attempts to program and erase a protected sector causes data-polling and toggle-bit (DQ6) to operate from 2-µs to 100-µs and then return to valid data.

sector-protect verify

Verification of the sector-protection programming is activated when $\overline{WE}$ is high, $\overline{OE}$ is low, $\overline{CE}$ is low, and address pin A9 = V_{ID}. Address pins A0 and A6 are set to V_{IL}, and A1 is set to V_{IH}. The sector-address pins A17 – A13 select the sector that is to be verified. The other addresses can be V_{IH} or V_{IL}. If the sector that is selected is protected, the DQs output 01h. If the sector is not protected, the DQs output 00h.

Sector-protect verify also can be read using the algorithm-selection command. After issuing the three-bus-cycle command sequence, the sector-protection status can be read on DQ0. Set address pins A0 = V_{IL}, A1 = V_{IH}, and A6 = V_{IL}. The sector address pins A17 – A13 select the sector to be verified. The remaining addresses are set to V_{IL}. If the sector selected is protected, DQ0 outputs a logic-high state. If the sector selected is not protected, DQ0 outputs a logic-low state. This mode remains in effect until another valid command sequence is written to the device. Figure 17 shows a timing diagram of the sector-protect operation and Figure 16 is a flowchart of the sector-protect algorithm.

sector unprotect

Prior to sector unprotect, all sectors must be protected using the sector-protect programming mode. The sector unprotect is activated when address pin A9 and control pin $\overline{OE}$ are forced to V_{ID}. Address pins A6 and A1 are set to V_{IH} while $\overline{CE}$ and A0 are set to V_{IL}. The sector-select address pins A17 – A13 can be V_{IL} or V_{IH}. All sectors are unprotected in parallel. Once the inputs are stable, $\overline{WE}$ is pulsed low for 10 ms causing the unprotect operation to begin on the falling edge of $\overline{WE}$ and to terminate on the rising edge of $\overline{WE}$. Figure 18 is a flow chart of the sector-unprotect algorithm and Figure 19 shows a timing diagram of the sector-unprotect operation.

sector-unprotect verify

Verification of the sector unprotect is activated when $\overline{WE}$ = V_{IH}, $\overline{OE}$ = V_{IL}, $\overline{CE}$ =V_{IL} and address pin A9 = V_{ID}. Select the sector to be verified. Address pins A1 and A6 are set to V_{IH}, and A0 is set to V_{IL}. The other addresses can be V_{IH} or V_{IL}. If the sector selected is protected, the DQs output 01h. If the sector is not protected, the DQs output 00h. Sector unprotect also can be read using the algorithm-selection command.

low V_{CC} write lockout

During power up and power down operations, write cycles are locked out for V_{CC} less than V_{LKO}. If $V_{CC} < V_{LKO}$, the command input is disabled and the device is reset to the read mode. On power up, if $\overline{CE}$ is low, $\overline{WE}$ is low, and $\overline{OE}$ is high, the device does not accept commands on the rising edge of $\overline{WE}$. The device automatically powers up in the read mode.

glitching

Pulses of less than five ns (typical) on $\overline{OE}$, $\overline{WE}$, or $\overline{CE}$ do not issue a write cycle.

power supply considerations

Each device should have a 0.1-µF ceramic capacitor connected between V_{CC} and V_{SS} to suppress circuit noise. Printed circuit traces to V_{CC} should be appropriate to handle the current demand and minimize inductance.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . −0.6 V to 7 V
Input voltage range V_I: All inputs except A9, $\overline{CE}$, $\overline{OE}$ (see Note 2) . . . . −0.6 V to V_{CC} + 1 V
A9, $\overline{CE}$, $\overline{OE}$ . . . . −0.6 V to 13.5 V
Output voltage range V_O (see Note 3) . . . . −0.6 V to V_{CC} + 1 V
Operating free-air temperature range during read/erase/program, T_A
(L) . . . . 0°C to 70°C
(E) . . . . −40°C to 85°C
Storage temperature range, T_{stg} . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to V_{SS}.
2. The voltage on any input or output can undershoot to –2 V for periods of less than 20 ns. See Figure 2.
3. The voltage on any input or output can overshoot to V_{CC} + 2 V for periods of less than 20 ns. See Figure 3.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	V
V_{IH}	High-level input voltage	TTL	2	VCC+0.5	V
		CMOS	V_{CC}–0.5	V_{CC}+0.5	V
V_{IL}	Low-level input voltage	TTL	–0.5	0.8	V
		CMOS	–0.5	0.8	
V_{ID}	Algorithm selection and sector protect input voltage		11.5	12.5	V
VLKO	Low V_{CC} lock-out voltage		5.2	4.2	V
T_A	Operating free-air temperature	L version	0	70	°C
		E version	–40	85	

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	TTL-input level	$V_{CC} = V_{CC}$ MIN, I_{OH} = –2.5 mA	2.4		V
		CMOS-input level	$V_{CC} = V_{CC}$ MIN, I_{OH} = – 100 µA	V_{CC}–0.4		
		CMOS-input level	$V_{CC} = V_{CC}$ MIN, I_{OH} = –2.5 mA	0.85*V_{CC}		V
V_{OL}	Low-level output voltage		$V_{CC} = V_{CC}$ MIN, I_{OL} = 5.8 mA		0.45	V
I_I	Input current (leakage)		$V_{CC} = V_{CC}$ MAX, $V_{IN} = V_{SS}$ to V_{CC}		±1	µA
I_O	Output current (leakage)		$V_O = V_{SS}$ to V_{CC}, $\overline{CE} = V_{IH}$		±1	µA
I_{ID}	High-voltage current (standby)		A9 or $\overline{CE}$ or $\overline{OE} = V_{ID}$ MAX		35	µA
I_{CC1}	V_{CC} supply current (standby)	TTL-input level	$\overline{CE} = V_{IH}, V_{CC} = V_{CC}$ MAX		1	mA
		CMOS-input level	$\overline{CE} = V_{CC} \pm 0.2$, $V_{CC} = V_{CC}$ MAX		100	µA
I_{CC2}	V_{CC} supply current (see Notes 4 and 5)		$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		40	mA
I_{CC3}	V_{CC} supply current (see Note 6)		$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		60	mA
I_{CC5}	Automatic sleep mode (see Notes 5 and 7)		$V_{IH} = V_{CC} \pm 0.3$ V, $V_{IL} = V_{SS} \pm 0.3$ V		100	µA

NOTES: 4. I_{CC} current in the read mode, switching at 6 MHz
5. I_{OUT} = 0 mA
6. I_{CC} current while erase or program operation is in progress
7. Automatic sleep mode is entered when addresses remain stable for 300 ns.

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
C_{i1}	Input capacitance (All inputs except A9, $\overline{CE}$, $\overline{OE}$)	V_I = 0 V, f = 1 MHz		7.5	pF
C_{i2}	Input capacitance (A9, $\overline{CE}$, $\overline{OE}$)	V_I = 0 V, f = 1 MHz		9	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz		12	pF

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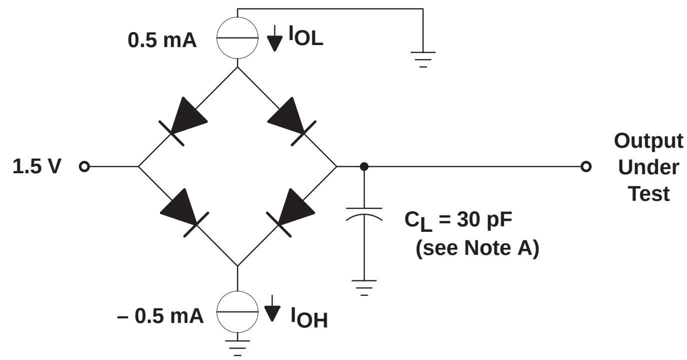
PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and fixture capacitance.

ac testing input/output waveforms

NOTE A: The ac testing inputs are driven at 2.4 V for logic high and 0.45 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low on both inputs and outputs. Each device should have a 0.1-µF ceramic capacitor connected between V_{CC} and V_{SS} as closely as possible to the device pins.

Figure 1. The ac Test Output Load Circuit

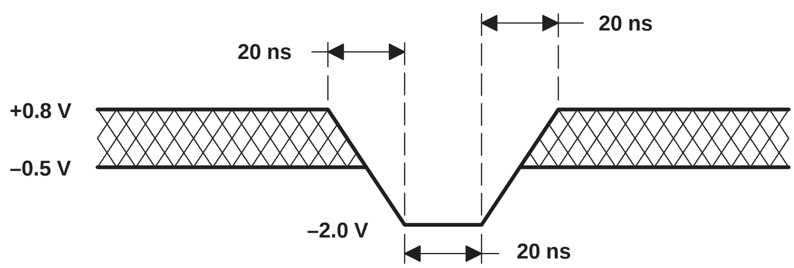


Figure 2. Maximum Negative Overshoot Waveform

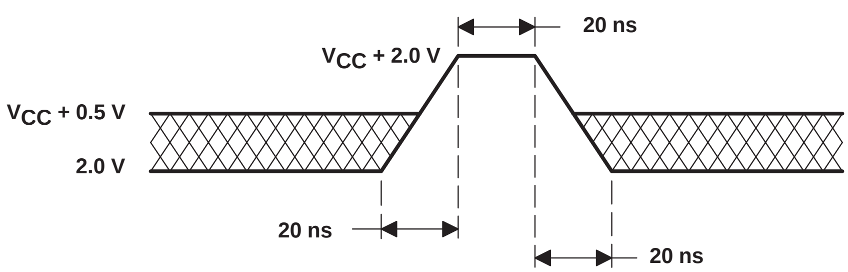


Figure 3. Maximum Positive Overshoot Waveform

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, read-only operation

PARAMETER		ALTERNATE SYMBOL	'29F002-70		'29F002-80		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(R)}$	Cycle time, read	t_{AVAV}	70		80		ns
$t_{a(A)}$	Access time, address	t_{AVQV}		70		80	ns
$t_{a(E)}$	Access time, $\overline{CE}$	t_{ELQV}		70		80	ns
$t_{a(G)}$	Access time, $\overline{OE}$	t_{GLQV}		35		40	ns
$t_{dis(E)}$	Disable time, $\overline{CE}$ to high impedance	t_{EHQZ}		30		30	ns
$t_{dis(G)}$	Disable time, $\overline{OE}$ to high impedance	t_{GHQZ}		30		30	ns
$t_{en(E)}$	Enable time, $\overline{CE}$ to low impedance	t_{ELQX}	0		0		ns
$t_{en(G)}$	Enable time, $\overline{OE}$ to low impedance	t_{GLQX}	0		0		ns
$t_{h(D)}$	Hold time, output from address $\overline{CE}$ or $\overline{OE}$ change	t_{AXQX}	0		0		ns
t_{READY}	$\overline{RESET}$ pin low to read			20		20	µs

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, controlled by $\overline{\text{WE}}$

PARAMETER		ALTERNATE SYMBOL	'29F002-70			'29F002-80			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$t_{c(W)}$	Cycle time, write	t_{AVAV}	70			80			ns
$t_{c(W)ER}$	Cycle time, sector-erase operation	t_{WHWH2}		1			1		s
	Cycle time, chip-erase operation	t_{WHWH3}		7	60		7	60	s
$t_{h(A)}$	Hold time, address	t_{WLAX}	45			45			ns
$t_{h(D)}$	Hold time, data valid after $\overline{\text{WE}}$ high	t_{WHDX}	0			0			ns
$t_{h(E)}$	Hold time, $\overline{\text{CE}}$	t_{EHWH}	0			0			ns
	Hold time, $\overline{\text{OE}}$ read	t_{WHGL1}	0			0			ns
	Hold time, $\overline{\text{OE}}$ toggle, data	t_{WHGL2}	10			10			µs
$t_{w(WL)}$	Pulse duration, $\overline{\text{WE}}$ low	t_{WLWH1}	45			45			ns
$t_{w(WH)}$	Pulse duration, $\overline{\text{WE}}$ high	t_{WHWL}	20			20			ns
	Pulse duration, $\overline{\text{WE}}$ low (see Note 8)	t_{WLWH2}	100			100			µs
	Pulse duration, $\overline{\text{WE}}$ low (see Note 9)	t_{WLWH3}	10			10			ms
$t_{rec(R)}$	Recovery time, read before write	t_{GHWL}	0			0			ns
$t_{su(A)}$	Setup time, address	t_{AVWL}	0			0			ns
$t_{su(D)}$	Setup time, data	t_{DVWH}	45			45			ns
$t_{su(E)}$	Setup time, $\overline{\text{CE}}$	t_{ELWL}	0			0			ns
	Setup time, V_{CC}	t_{VCEL}	45			50			µs
	Setup time, $\overline{\text{CE}}$ VID to $\overline{\text{WE}}$ (see Note 9)	t_{EHVWL}	4			4			µs
	Setup time, $\overline{\text{OE}}$ V_{ID} to $\overline{\text{WE}}$ (see Notes 8 and 9)	t_{GHVWL}	4			4			µs
	Transition time, V_{ID} (see Notes 8 and 9)	t_{HVT}	4			4			µs
$t_{c(W)PR}$	Programming operation	t_{WHWH1}		8			8		µs

NOTES: 8. Sector-protect timing
9. Sector unprotect timing

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, controlled by $\overline{CE}$

PARAMETER		ALTERNATE SYMBOL	'29F002-70			'29F002-80			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$t_{c(W)}$	Cycle time, write	t_{AVAV}	70			80			ns
	Cycle time, sector-erase operation	t_{EHEH2}	1			1			s
	Cycle time, chip-erase operation	t_{EHEH3}		7	60		7	60	s
$t_{h(A)}$	Hold time, address	t_{ELAX}	45			45			ns
$t_{h(D)}$	Hold time, data	t_{EHDX}	0			0			ns
$t_{h(W)}$	Hold time, $\overline{WE}$	t_{EHWH}	0			0			ns
$t_{h(C)}$	Hold time, $\overline{OE}$ read	t_{EHGL1}	0			0			ns
	Hold time, $\overline{OE}$ toggle, data	t_{EHGL2}	10			10			ns
$t_{w(EL)}$	Pulse duration, $\overline{CE}$ low	t_{ELEH1}	45			45			ns
$t_{w(EH)}$	Pulse duration, $\overline{CE}$ high	t_{EHEL}	20			20			ns
$t_{rec(R)}$	Recovery time, read before write	t_{GHEL}	0			0			ns
$t_{su(A)}$	Setup time, address	t_{AVEL}	0			0			ns
$t_{su(D)}$	Setup time, data	t_{DVEH}	45			45			ns
$t_{su(W)}$	Setup time, $\overline{WE}$	t_{WLEL}	0			0			ns
	Setup time, $\overline{OE}$	t_{GLEL}	0			0			ns
	Programming operation	t_{EHEH1}		8			8		µs

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erase and program performance †

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Sector erase time	Excludes 00H programming prior to erasure		1‡	15§	s
Program time	Excludes system-level overhead	9	9	3600§	µs
Chip programming time	Excludes system-level overhead		6‡	50§	s
Erase/program cycles		10000	100000		cycles

† The internal algorithms allow for 2.5 ms byte program time. DQ5 = 1 only after a byte takes the theoretical maximum time to program. A minimal number of bytes can require signficantly more programming pulses than the typical byte. The majority of the bytes program within one or two pulses. This is demonstrated by the typical and maximum programming time listed above.
‡ 25°C, 5 V V_{CC} 100000 cycles, typical pattern
§ Under worst case conditions, 90°C, 4.5 V V_{CC} 100000 cycles

latchup characteristics (see Note 10)

PARAMETER	MIN	MAX	UNIT
Input voltage with respect to V_{SS} on all pins except I/O pins (including A9 and $\overline{OE}$)	– 1	13	V
Input voltage with respect to V_{SS} on all I/O pins	– 1	V_{CC} + 1	V
Current	– 100	100	mA

NOTE 10: Includes all pins except V_{CC} test conditions: V_{CC} = 3 V, one pin at a time

pin capacitance, all packages (see Note 11)

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
C_{IN}	Input capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control pin capacitance	V_{IN} = 0	8	10	pF

NOTE 11: Test conditions T_A = 25°C, f = 1 MHz

data retention

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Minimum pattern data retention time	150°C	10		Years
	125°C	20		

read operation

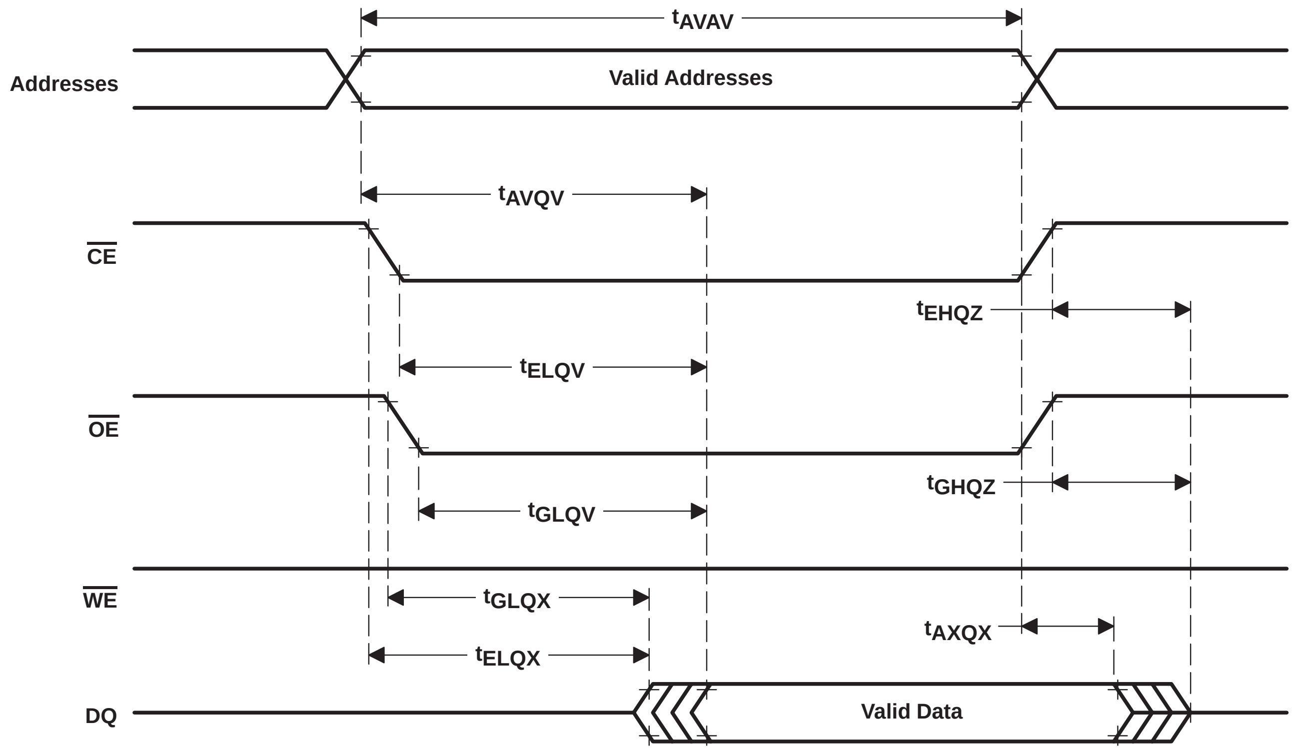

Figure 4. AC Waveform for Read Operation

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write operation

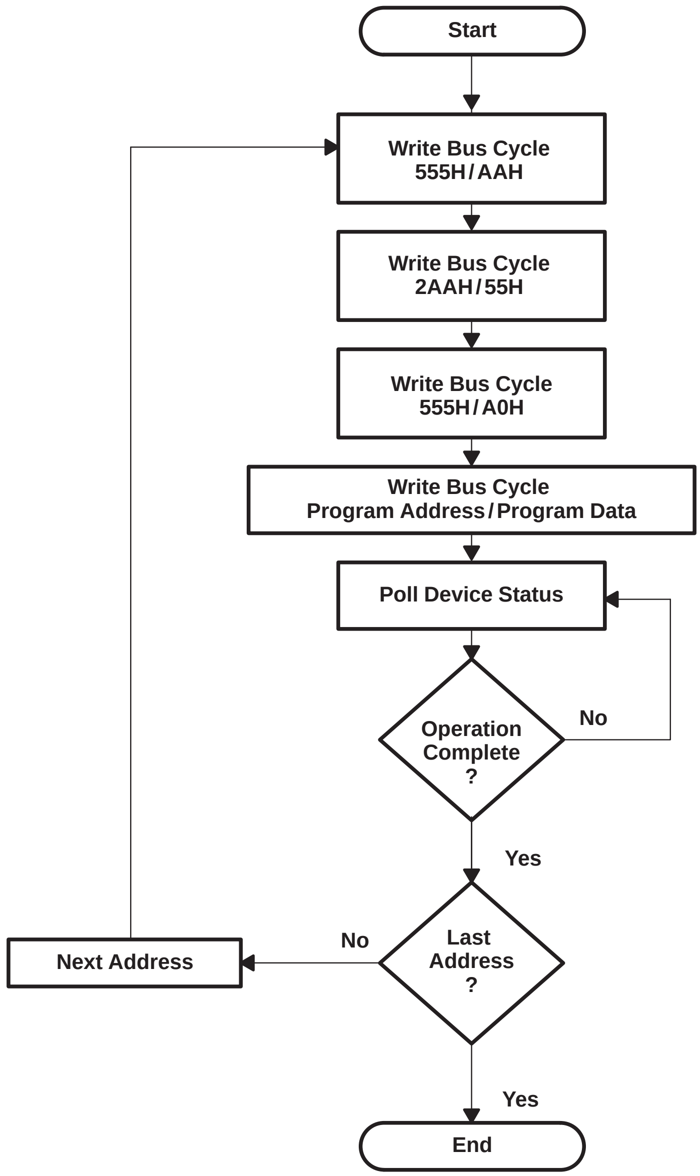
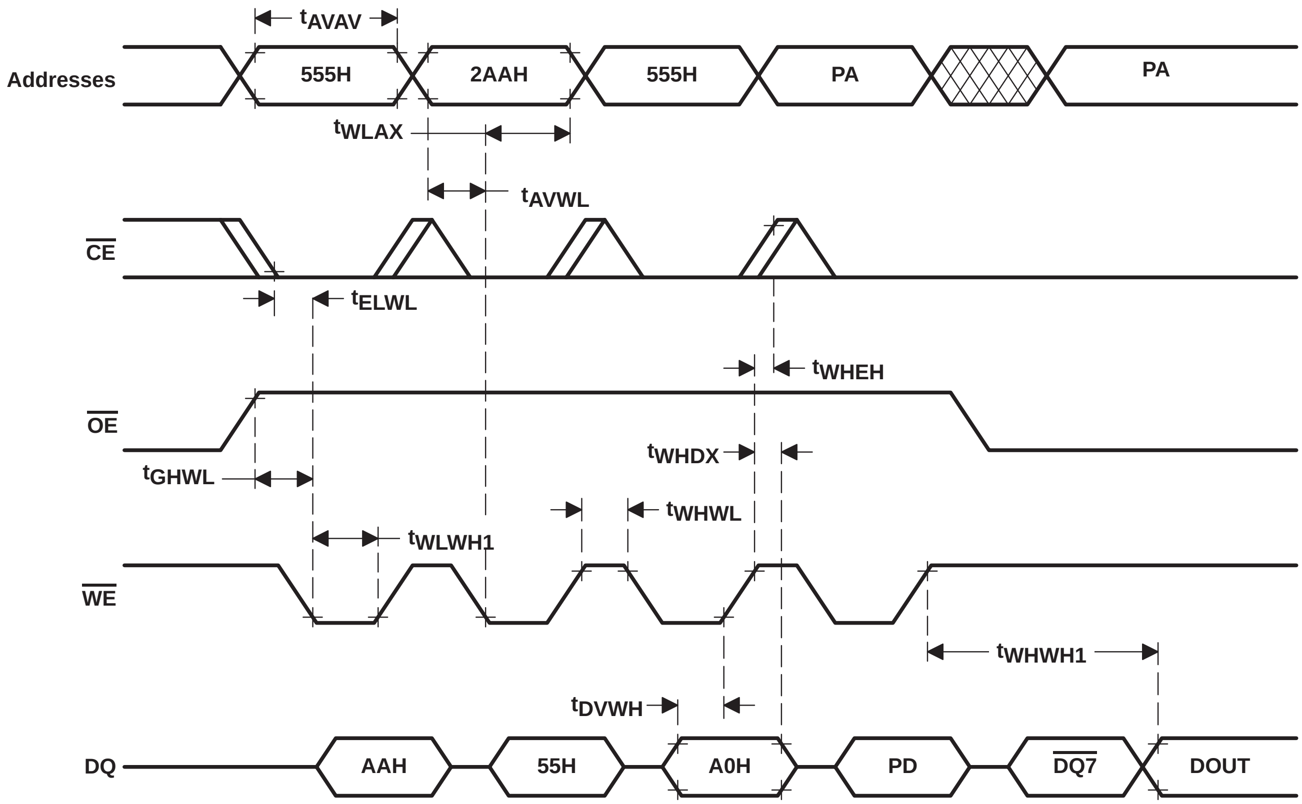


Figure 5. Program Algorithm Flow Chart

write operation (continued)



NOTES: A. PA = Address to be programmed
B. PD = Data to be programmed
C. $\overline{\text{DQ7}}$ = Complement of data written to DQ7

Figure 6. AC Waveform for Program Operation

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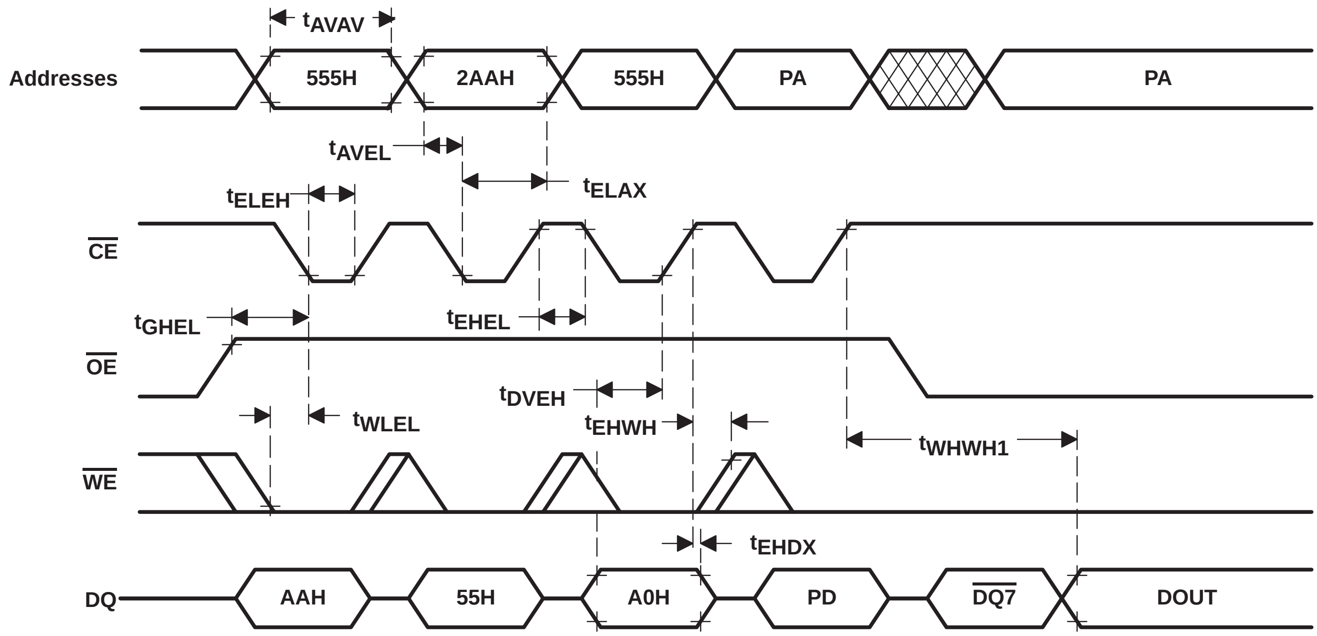
write operation (continued)



NOTES: A. PA = Address to be programmed
B. PD = Data to be programmed
C. $\overline{DQ7}$ = Complement of data written to DQ7

Figure 7. AC Waveform for Alternate $\overline{CE}$-Controlled Write Operation

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chip-erase operation

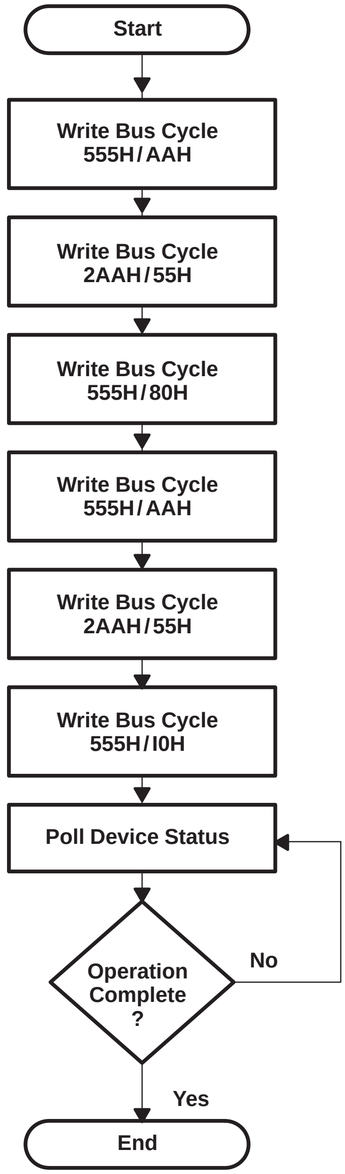

Figure 8. Chip-Erase Algorithm Flow Chart

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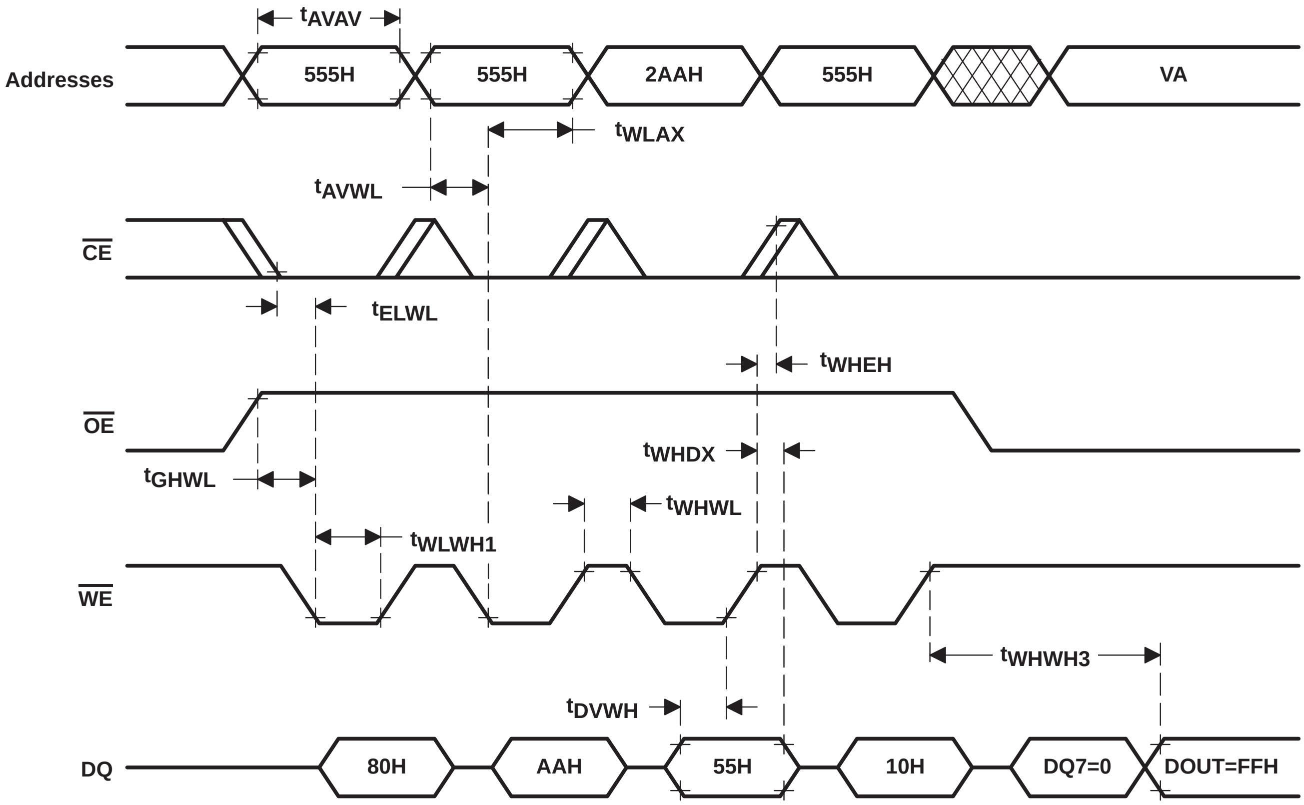
chip-erase operation (continued)



NOTES: A. VA = any valid address
B. Figure details the last four bus cycles in a six-bus-cycle operation

Figure 9. AC Waveform for Chip-Erase Operation

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sector-erase operation

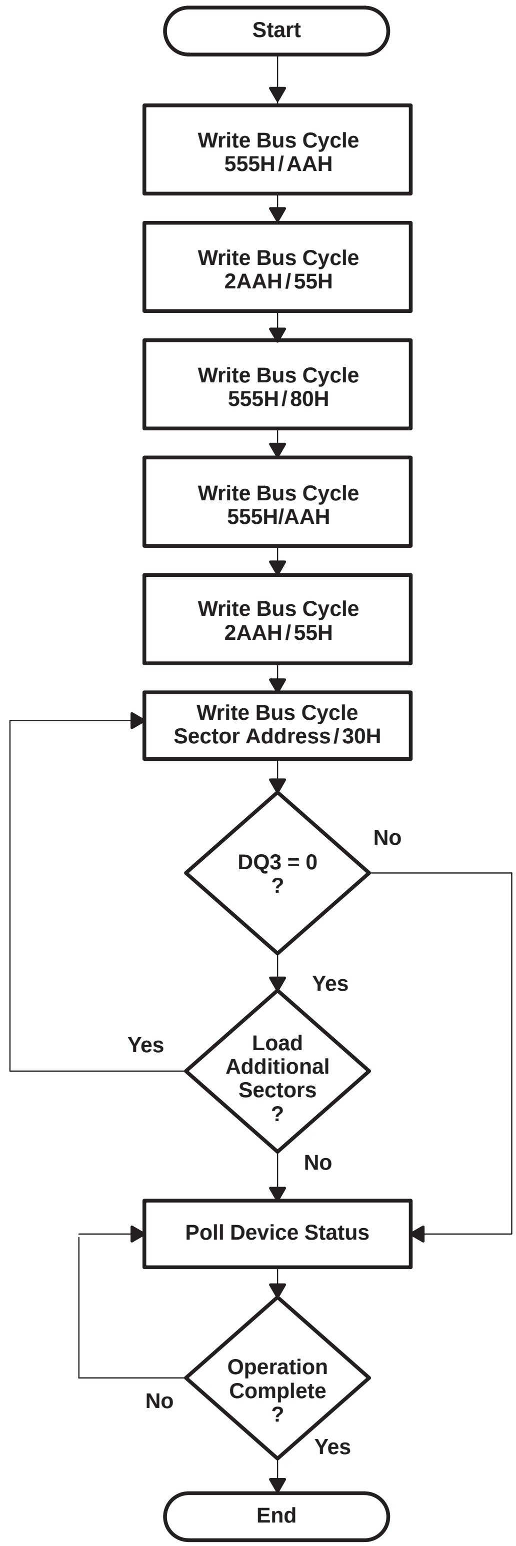

Figure 10. Sector-Erase Algorithm

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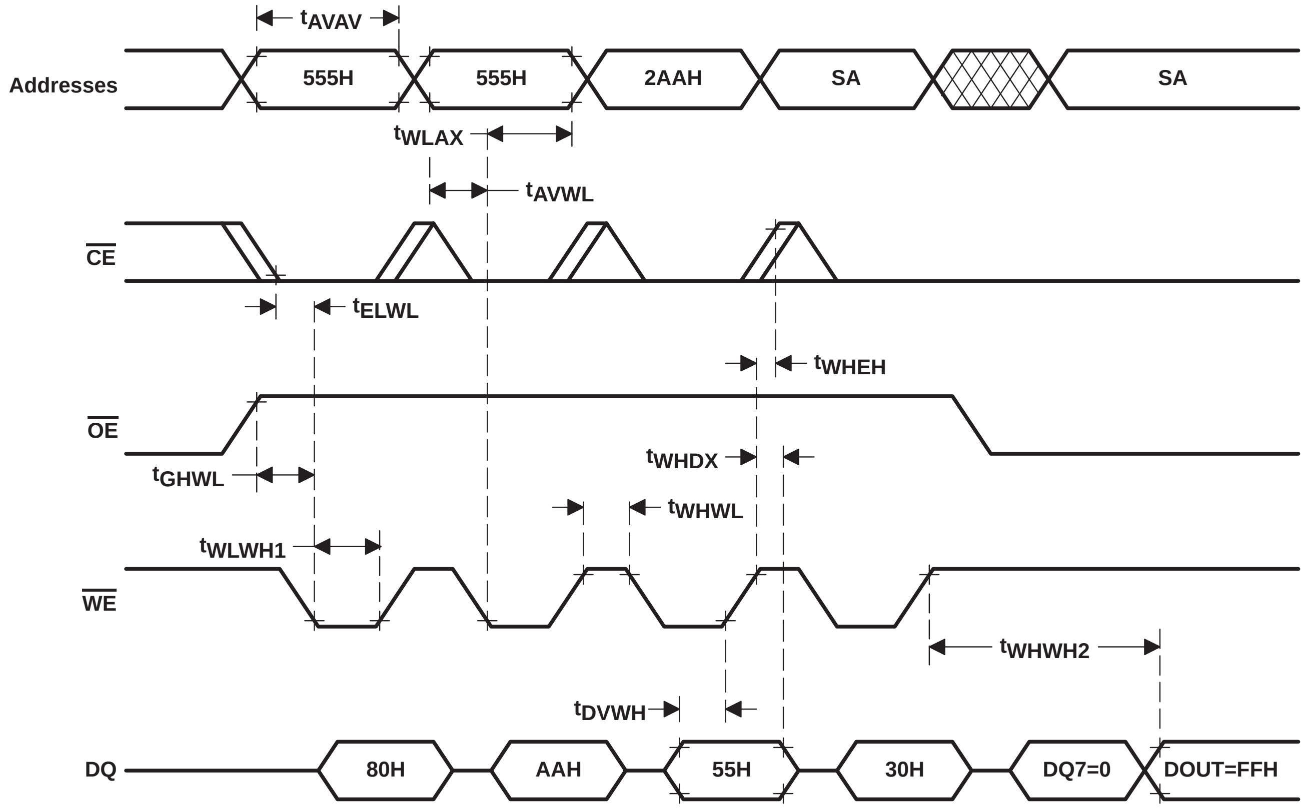
sector-erase operation (continued)



NOTES: A. SA = Sector address to be erased
B. Figure details the last four bus cycles in a six-bus-cycle operation.

Figure 11. AC Waveform for Sector-Erase Operation

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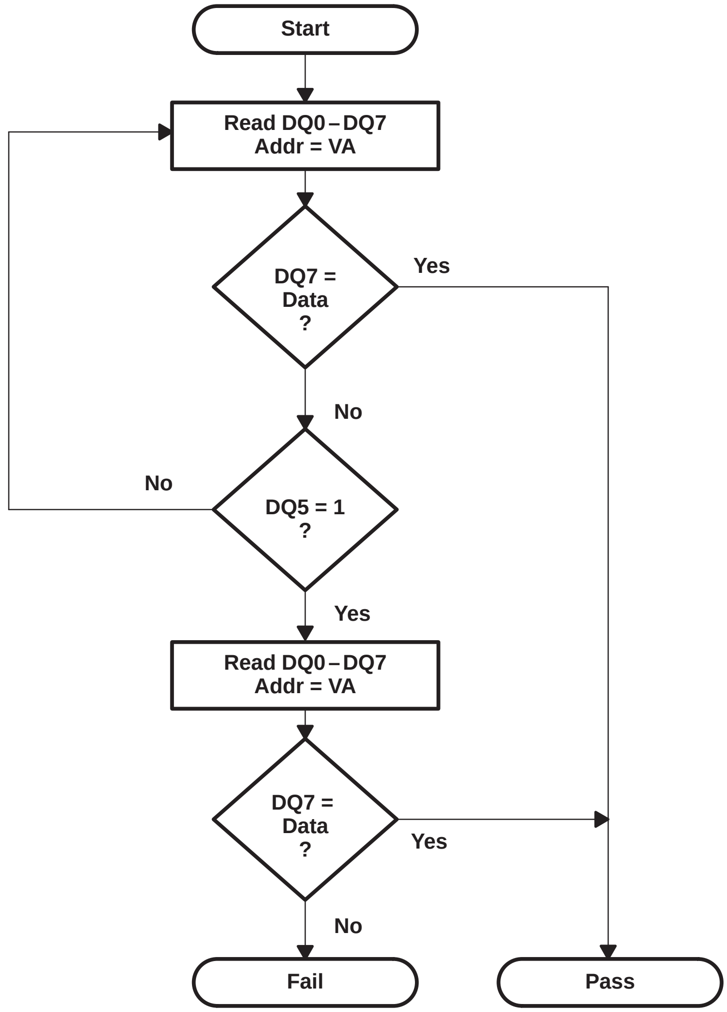
data-polling operation



NOTES: A. Polling status bits DQ7 and DQ5 may change asynchronously.
Read DQ7 after DQ5 changes states.
B. VA = Program address for byte programming
= Selected sector address for sector erase
= Any valid address for chip erase

Figure 12. Data-Polling Algorithm

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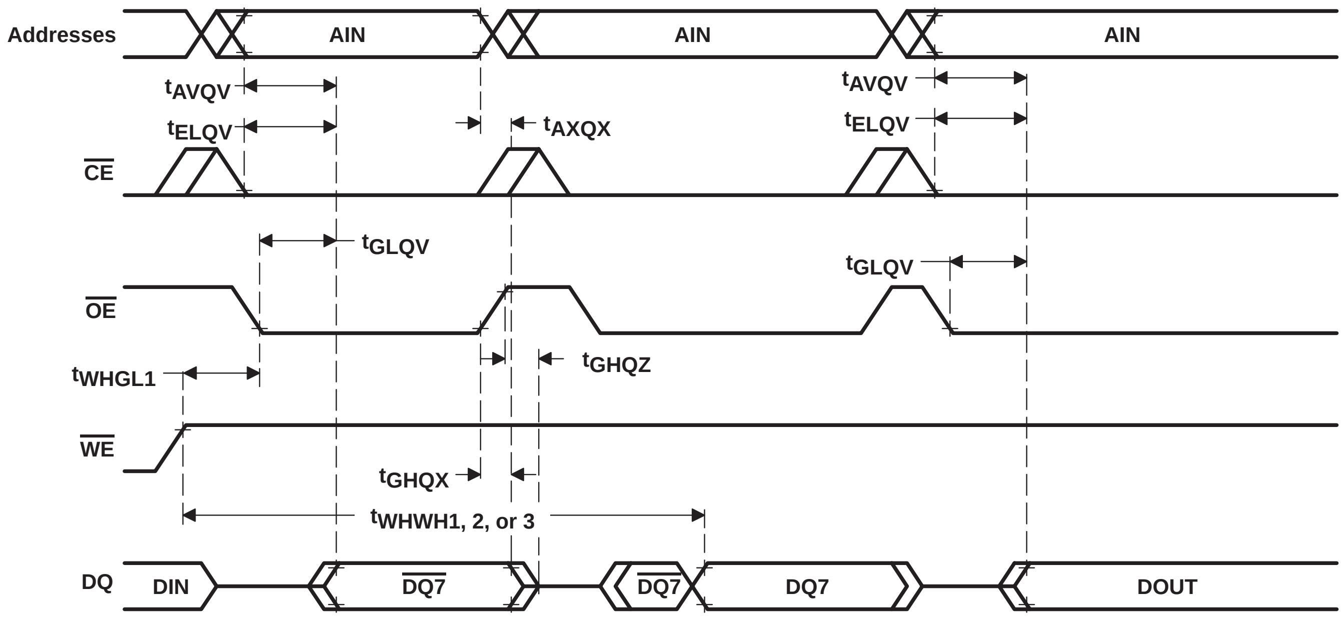
data-polling operation (continued)



NOTES: A. DIN = Last command data written to the device
B. $\overline{DQ7}$ = Complement of data written to DQ7
C. DOUT = Valid data output
D. AIN = Valid address for byte-program, sector-erase, or chip-erase operation

Figure 13. AC Waveform for Data-Polling Operation

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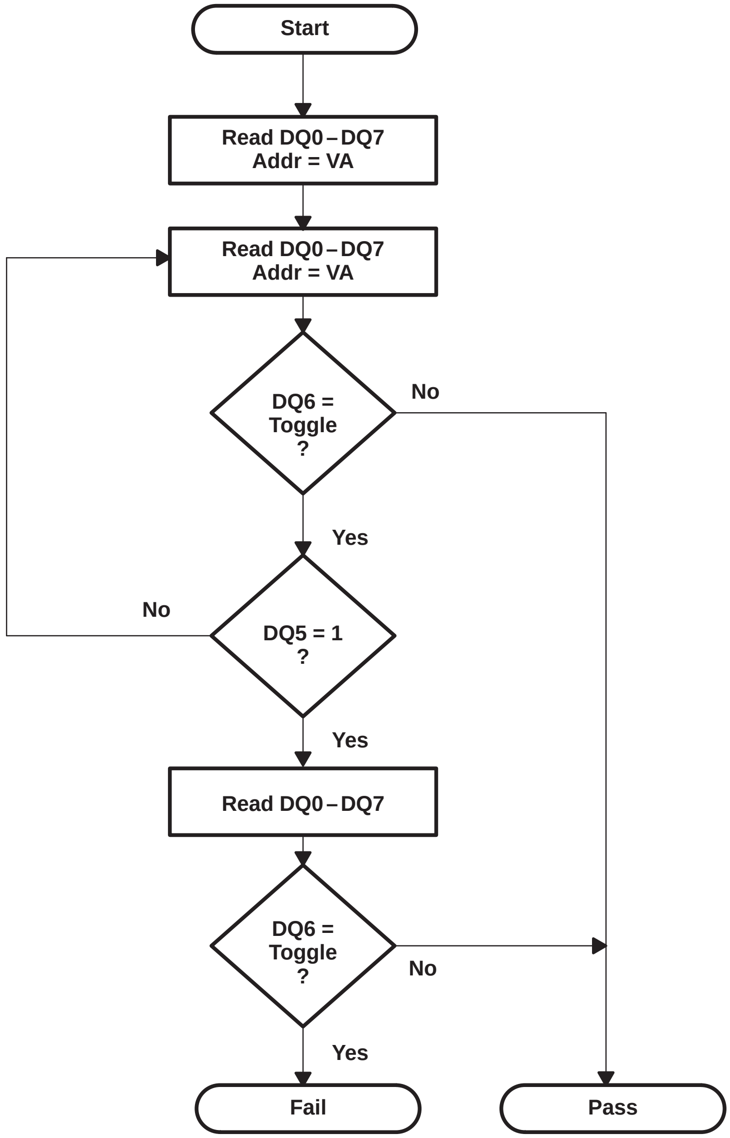
toggle-bit operation



NOTE A: Polling status bits DQ6 and DQ5 can change asynchronously. Read DQ6 after DQ5 changes states.

Figure 14. Toggle-Bit Algorithm

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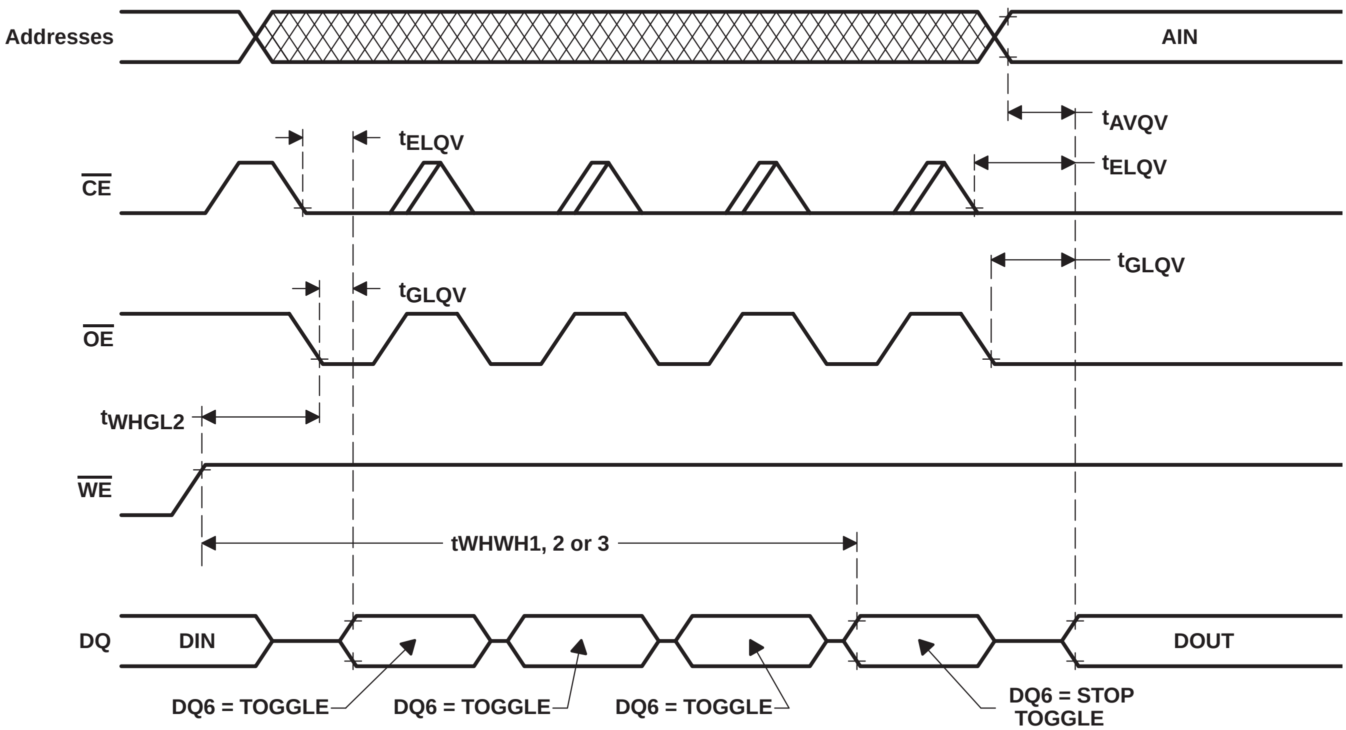
toggle-bit operation (continued)



NOTES: A. DIN = Last command data written to the device
B. DQ6 = Toggle bit output
C. DOUT = Valid data output
D. AIN = Valid address for byte-program, sector-erase, or chip-erase operation

Figure 15. AC Waveform for Toggle-Bit Operation

sector-protect operation

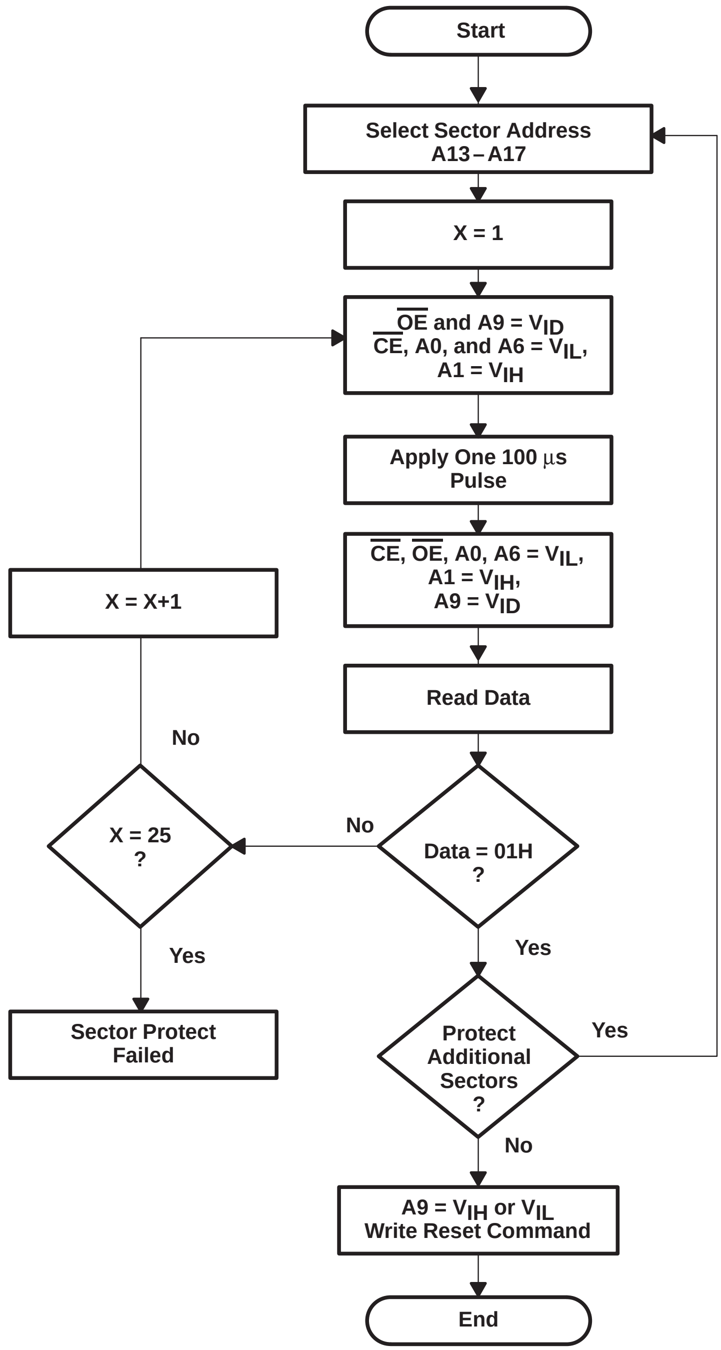


Figure 16. Sector-Protect Algorithm

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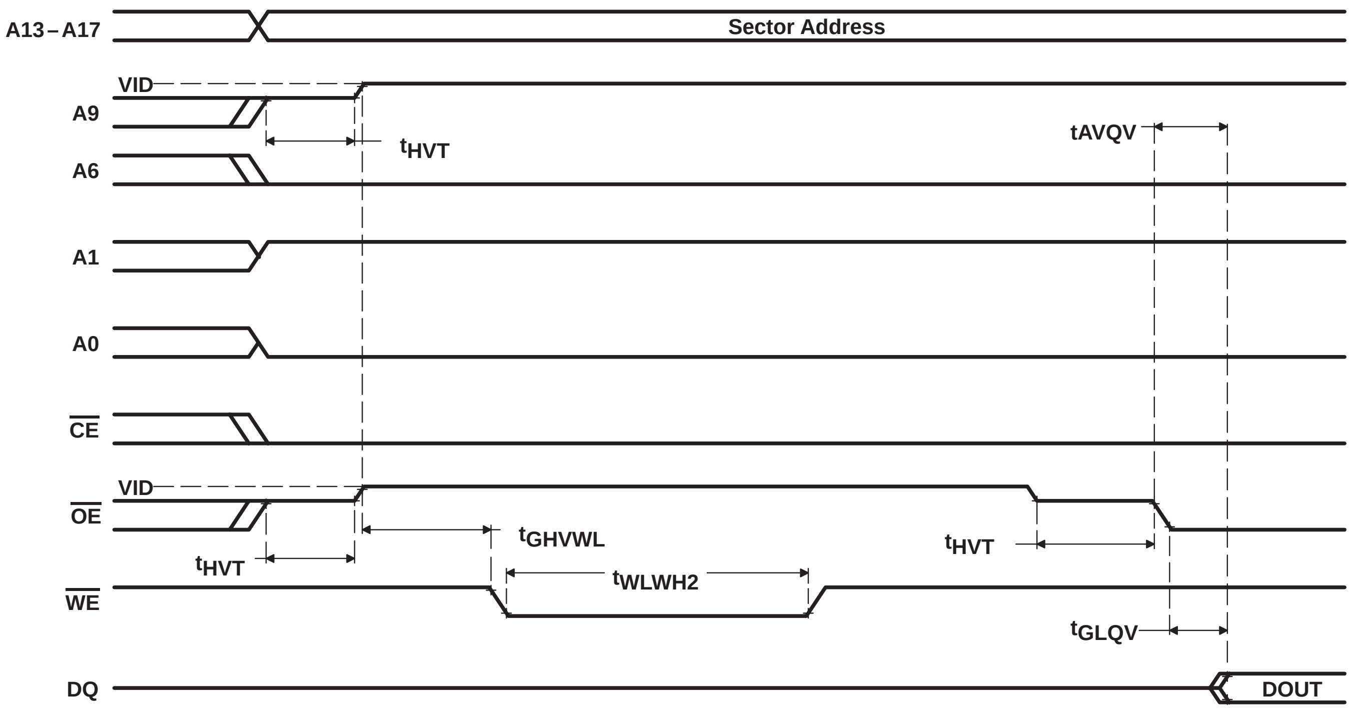
sector-protect operation (continued)



NOTE A: DOUT = 00H if selected sector is not protected,
01H if the sector is protected

Figure 17. AC Waveform for Sector-Protect Operation

sector-unprotect operation

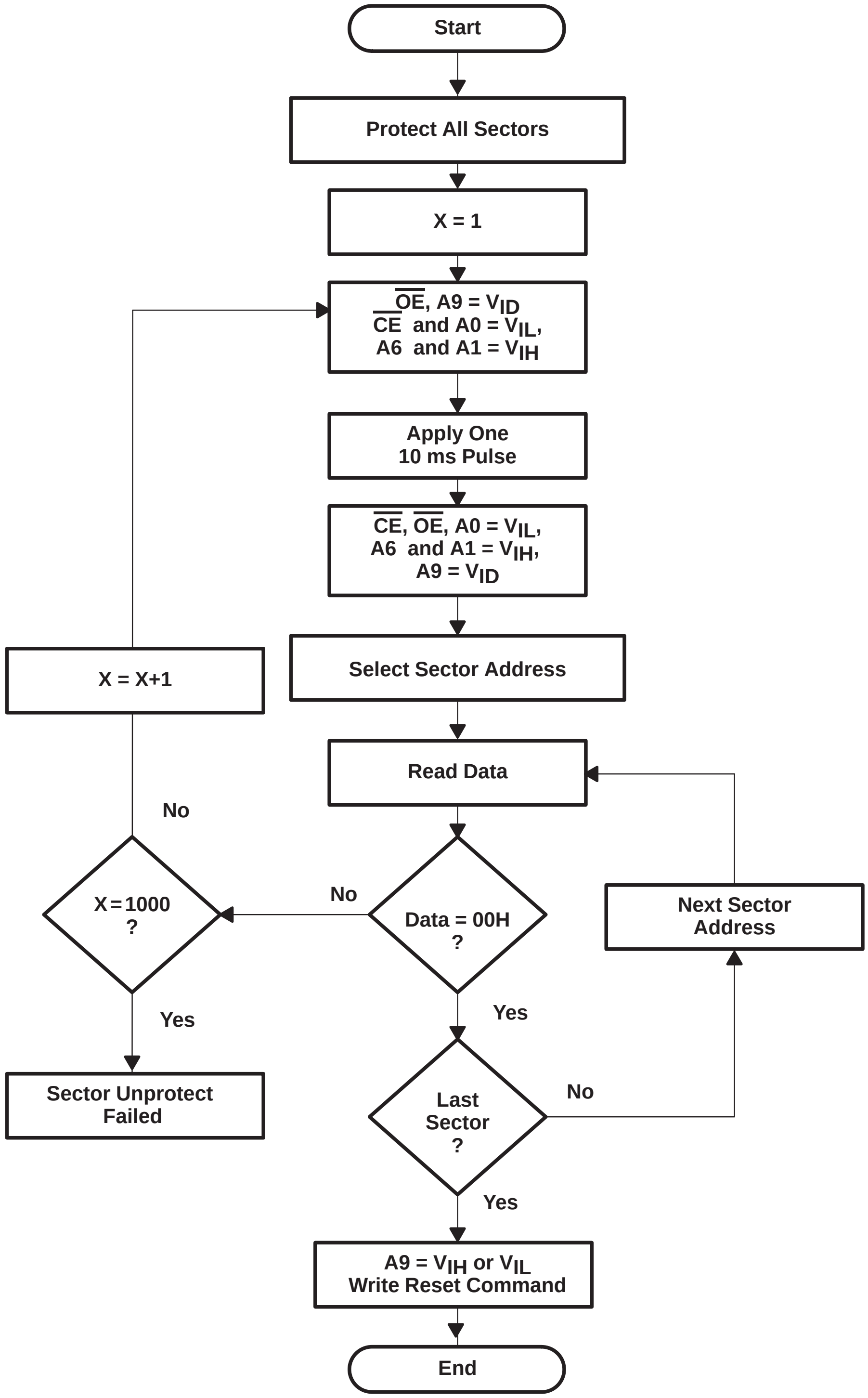


Figure 18. Sector-Unprotect Algorithm

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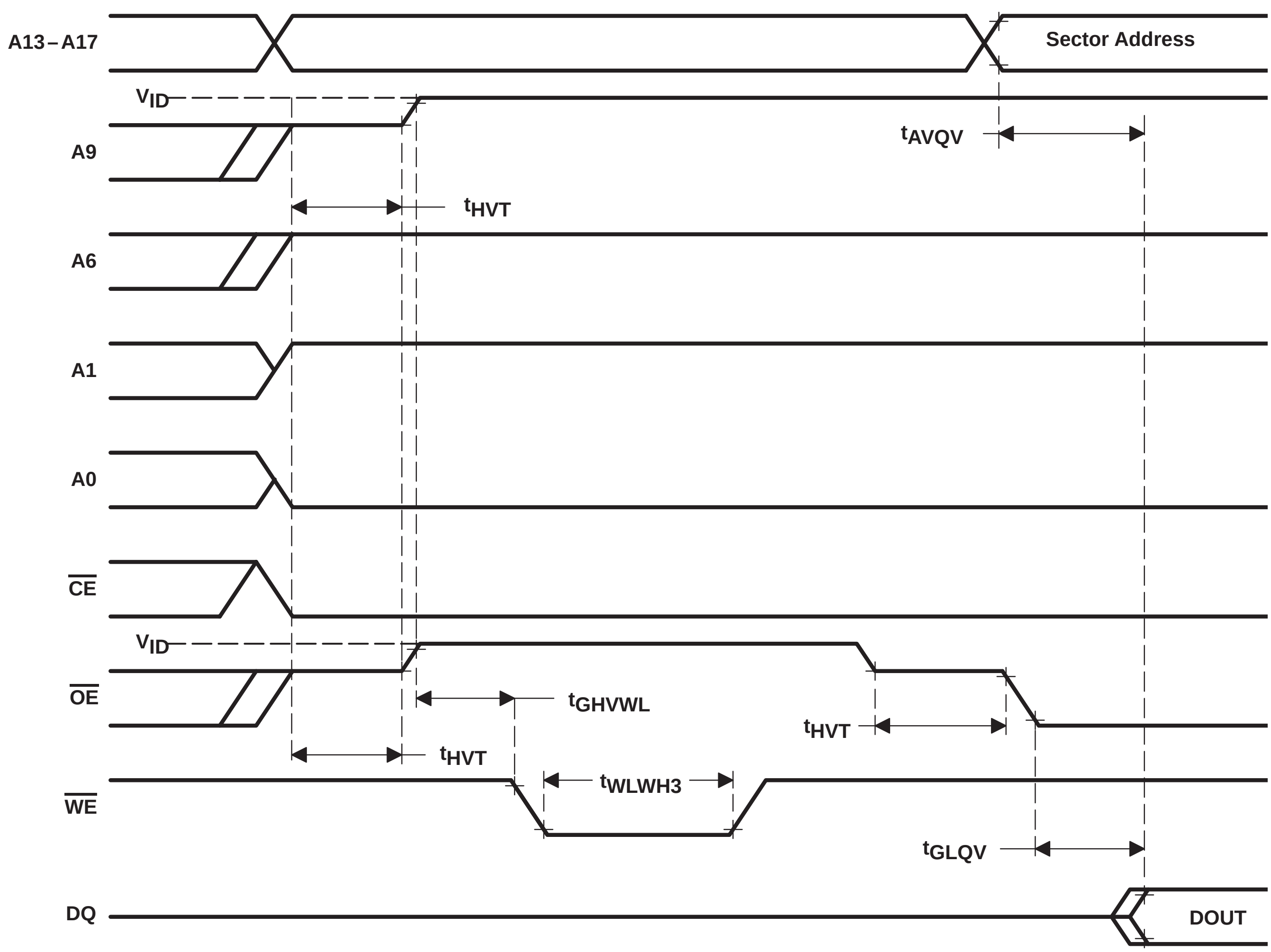
sector-unprotect operation (continued)

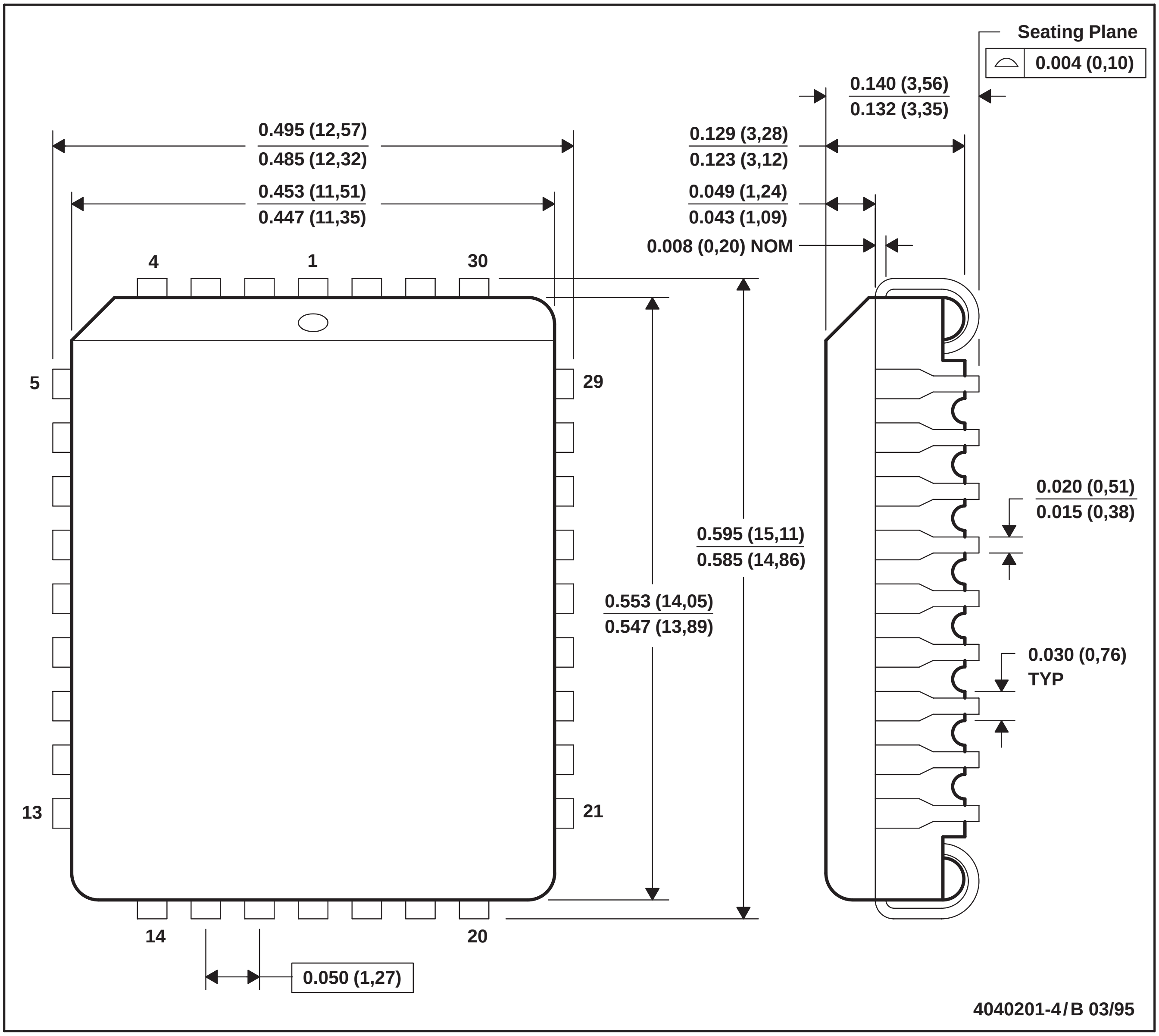


NOTE A: DOUT = 00H if selected sector is not protected,
01H if the sector is protected

Figure 19. AC Waveform for Sector-Unprotect Operation

MECHANICAL DATA

FM (R-PQCC-J32) **PLASTIC J-LEADED CHIP CARRIER**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-016

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