QUALITY SEMICONDUCTOR, INC.

High-Speed CMOS 1k x 64, 2k x 64 Content-Addressable Memory (QCAM™) Associative Processor

QS761480
QS762470

FEATURES

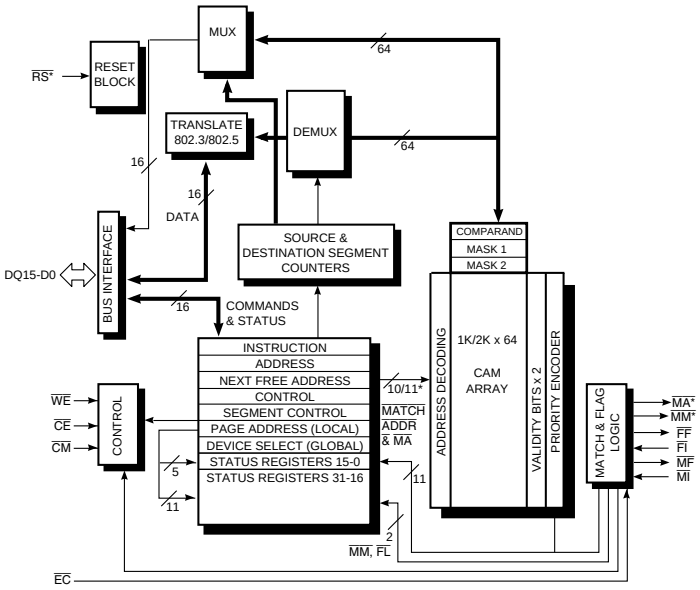
- 1k/2k x 64 CAM architecture
- 16-bit I/O interface
- Fast compare cycle times
- Pin compatible with the MUSIC MU9C1480/A and MU9C2480/A
- External reset pin (QS762470 device only)
- Power-up reset
- Extensive instruction set adds flexibility
- Memory array width can be configured as a mixture of RAM and CAM cell on 16-bit boundaries
- Programmable data translation between IEEE 802.3 and 802.5 formats
- Priority encoder for highest-priority address match
- Two Mask Registers allow masking of individual bits for both writing and comparing
- Memory operations allow random, associative, and write at-next-free-address cycles
- Depth-expandable with no additional logic and no performance penalty
- 48-bit word match in 3 cycles
- Commercial temperature range (0°C to 70°C)
- Available in 44-pin PLCC

DESCRIPTION

The QS761480 and QS762470 is a family of 1k and 2k x 64-bit CAMs (content-addressable memories). These devices are utilized in LAN (Local Area Network) environments for high-bandwidth, address-filtering applications, specifically in bridges, routers, and switches.

These devices are also ideal for other high-speed applications such as database accelerators, pattern recognition, and disk caches. QCAMs are easily depth-expanded with no additional logic. Another powerful feature is the instruction set which allows flexible bit and word masking

Figure 1. Functional Block Diagram



Note: Items marked with a " * " are applicable to the QS762470 only

Figure 2. Pinout for QS761480

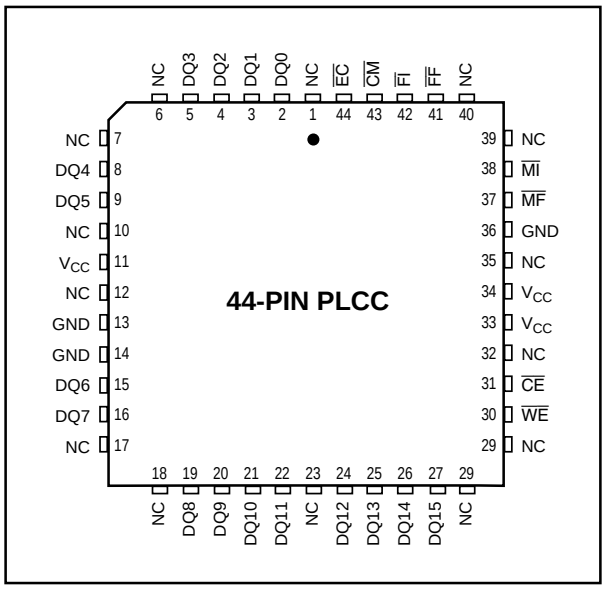
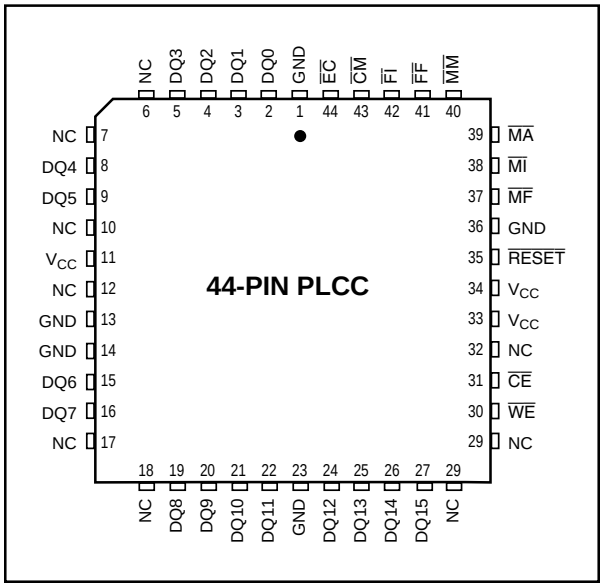


Figure 3. Pinout for QS762470



FUNCTIONAL DESCRIPTION

The QS761480 (1k x 64) and the QS762470 (2k x 64) are pin compatible with each other. This allows for an easy migration from the 1k to the 2k density in next generation board designs. The QCAM™ pin assignments for the 44-pin PLCC are shown in Figures 2 and 3.

Data/Command Bus

DQ15-DQ0

The DQ15-DQ0 lines convey data, commands, and status to and from the QS761480/QS762470. The state of the $\overline{WE}$ input determines whether data flows into or out of the device, while the $\overline{CM}$ input determines whether the information on the DQ15-DQ0 lines is interpreted as data or as a command or status. DQ0 is the least-significant bit (LSB) of the information.

In command write mode ($\overline{CM}$ is LOW, $\overline{WE}$ is LOW), the default destination of the data input on the DQ15-DQ0 lines is the Instruction Register; in command read mode ($\overline{CM}$ is LOW, $\overline{WE}$ is HIGH), the default source of the data output on the DQ15-DQ0 lines is the Status Register. A Temporary Command Override (TCO) instruction will temporarily change the default source or destination to the Address Register, the Control Register, the Page Address Register, the Device Select Register, the Next-Free-Address Register (read-only), or the Segment Control Register.

For data write cycles ($\overline{CM}$ is HIGH, and $\overline{WE}$ is LOW), and data read cycles ($\overline{CM}$ and $\overline{WE}$ are HIGH), the default destination/source of data input/output on the DQ15-DQ0 line is the Comparand Register. A select persistent source (SPS) or select persistent destination (SPD) command will change the destination/source to either the Mask Register 1, Mask Register 2, or CAM array.

Control Pins

$\overline{CE}$, Chip Enable (Input)

The $\overline{CE}$ input is the main clock control input of the QS761480/QS762470. It enables the QS761480/QS762470 while LOW, registers the control signals on its falling edge and releases them on the rising edge, and clocks the destination or source segment counter on its rising edge.

$\overline{CE}$ is also used in timing the locking and unlocking of the daisy-chain in depth-expanded systems. The daisy-chain is locked on the rising edge of $\overline{CE}$ during a cycle in which $\overline{EC}$ is LOW at the falling edge of $\overline{CE}$; correspondingly, the daisy-chain is unlocked on the rising edge of $\overline{CE}$ during a cycle in which $\overline{EC}$ is HIGH at the falling edge of $\overline{CE}$.

When $\overline{CE}$ is HIGH, the device is disabled and standby power is consumed, the output buffers are in their high-impedance state, and neither data nor commands can be written to the device, regardless of the state of $\overline{WE}$. When the $\overline{CE}$ input is LOW, the device is enabled for normal operation and active power is consumed.

$\overline{RESET}$ Qs762470 CAM Only
Driving reset low resets the device to conditions shown in Table 5. The external reset operates in parallel with the power-on reset. For compatibility with the QS761480 the reset has an internal pull-up so it can be left unconnected.

The QS761480 has a power-up reset only.

$\overline{WE}$, Write Enable (Input)
The $\overline{WE}$ input selects the direction of data transfer during a QCAM cycle. The state of the $\overline{WE}$ input is registered on the falling edge of $\overline{CE}$. When $\overline{WE}$ is registered HIGH, data are output from the selected source within the device. When the $\overline{WE}$ input is registered LOW, data are written into the selected destination within the device. When $\overline{WE}$ is registered LOW, the output buffers remain in the high-impedance state.

$\overline{CM}$, Data/Command Select (Input)
The $\overline{CM}$ input selects whether the information on the DQ15-DQ0 lines is interpreted as data or as a command or status. The state of the $\overline{CM}$ input is registered on the falling edge of $\overline{CE}$. When $\overline{CM}$ is HIGH, the data present on the DQ15-DQ0 lines are written into the persistently selected destination during a data write cycle ($\overline{WE}$ is LOW) or is read from the persistently selected source during a data read cycle ($\overline{WE}$ is HIGH).

When $\overline{CM}$ and $\overline{WE}$ are LOW (a command write cycle), the data on the DQ15-DQ0 lines are written by default into the Instruction Register. When $\overline{CM}$ is LOW, and $\overline{WE}$ is HIGH (a command read cycle), data is read by default from the Status Register. The default source or destination can be temporarily overridden by a TCO command.

$\overline{EC}$, Enable Comparison (Input)
The $\overline{EC}$ input locks and unlocks the daisy-chain in a depth-expanded system. It is registered internally by the falling edge of $\overline{CE}$ and is synchronized with the rising edge of $\overline{CE}$. If $\overline{EC}$ is LOW at the falling edge of $\overline{CE}$, the results of a comparison are conveyed via the $\overline{MF}$ output after the rising edge of $\overline{CE}$. When $\overline{EC}$ is HIGH on consecutive cycles, the $\overline{MF}$ flag stays HIGH regardless of the results of the comparison. When $\overline{EC}$ is LOW on consecutive cycles, the $\overline{MF}$ output will go LOW if enabled in the Control Register and the $\overline{MI}$ input is LOW, or a true comparison results between the value held in this particular Comparand Register and one or more of the unmasked contents of the CAM section. When the state of $\overline{EC}$ changes from LOW to HIGH at the start of a cycle, the $\overline{MF}$ output will go HIGH after the rising edge of $\overline{CE}$ of that cycle. $\overline{EC}$ must be HIGH to initialize the QCAM (Refer to Table 15 for $\overline{EC}$ operation).

Match And Flag Logic Pins

$\overline{MF}$, Match Flag (Output)
The $\overline{MF}$ output is the Match flag, which indicates whether a valid match has occurred during a comparison cycle. The $\overline{MF}$ output is active only when enabled in the Control Register in a cycle when the $\overline{EC}$ line was LOW at the falling edge of $\overline{CE}$ at the beginning of that cycle; the $\overline{MF}$ output will not go LOW until after the rising edge of $\overline{CE}$ during that cycle. Similarly, when $\overline{EC}$ was HIGH at the falling edge of $\overline{CE}$ at the beginning of a subsequent cycle, the $\overline{MF}$ output will go HIGH after the rising edge of $\overline{CE}$ during that cycle.

If the $\overline{MF}$ output (after being enabled by the Control Register, $\overline{EC}$, and $\overline{CE}$) is HIGH at the end of a comparison cycle, then there was no match between the unmasked portion of the value held in the Comparand Register and any of the valid contents of the CAM array in this or an upstream device. If the $\overline{MF}$ output is LOW, then there was at least one match between the unmasked portion of the value held in the Comparand Register and the valid contents of the CAM array in this or an upstream device. In a depth-expanded system, with $\overline{MF}$ active, the $\overline{MF}$ output will also go LOW if the $\overline{MI}$ input is LOW and $\overline{EC}$ is LOW at the beginning of a cycle, even with no match in that specific device.

The $\overline{MF}$ output can be deactivated by the flag disable state in the Control Register and the $\overline{MF}$ output will remain HIGH, even if there is a valid match during a compare cycle, unless $\overline{MI}$ goes LOW.

$\overline{MI}$, Match Input (Input)
The $\overline{MI}$ input is used in depth-expanded systems to prioritize QCAM devices. When the $\overline{MI}$ input is HIGH, the $\overline{MF}$ output state is determined by the state of $\overline{EC}$ and the internal match condition. When $\overline{MI}$ is LOW, $\overline{MF}$ will be forced LOW whenever $\overline{EC}$ was LOW at the start of the cycle. When multiple QCAMs are daisy-chained, the $\overline{MF}$ output of one device is connected to the $\overline{MI}$ input of the next-lower-priority device.

$\overline{MA}$ Internal Match Flag (Output)
QS762470 Only
$\overline{MA}$ goes LOW when one or more valid matches occur during the current or previous compare cycle. $\overline{MA}$ is NOT qualified by $\overline{EC}$ or $\overline{MI}$ and is only a reflection of the internal match flag from that specific device's status register.

$\overline{MM}$ Multiple Match Flag (Output)
QS762470 Only

$\overline{MM}$ goes LOW when more than one valid match occurs during the last or previous cycle. The $\overline{MM}$ output is not qualified by $\overline{EC}$ or $\overline{MI}$ and is only a reflection on the internal multiple match flag from that specific device's status register.

$\overline{FF}$, Full Flag (Output)
The $\overline{FF}$ output is the Full flag, which indicates if any memory locations are empty. When the $\overline{FF}$ output is HIGH, there is at least one empty location, or the $\overline{FI}$ input is HIGH. When the $\overline{FF}$ output is LOW, there are no empty locations. The $\overline{FF}$ output can be deactivated by the Control Register, in which case the $\overline{FF}$ output will remain LOW even if there is an empty location.

$\overline{FI}$, Full Input (Input)
The $\overline{FI}$ input is used in depth-expanded systems to generate a CAM memory system full indication. When the $\overline{FI}$ input is HIGH, the $\overline{FF}$ output is forced HIGH, even if the Full flag is disabled. When $\overline{FI}$ is LOW, the $\overline{FF}$ output will be HIGH if that device is not full, and will be LOW if that device is full. When multiple QCAMs are daisy-chained, the $\overline{FF}$ of one device is connected to the $\overline{FI}$ input of the next-lower-priority device.

BLOCK DIAGRAM DESCRIPTION

As shown in the block diagram of the QS761480/ QS762470 (Figure 1), the DQ15-DQ0 data I/O bus enters the device via an I/O buffer. A control bus comprising chip enable ($\overline{CE}$), write enable ($\overline{WE}$), command enable ($\overline{CM}$), and enable comparison ($\overline{EC}$) inputs, along with instructions loaded into an Instruction Register, controls the operation of the device.

The control bus and the Instruction Register are fed to the control block and flag logic block, which control the internal functions of the device. Independent source and destination segment counters control the multiplexing and demultiplexing of the 16-bit I/O data to and from the 64-bit internal bus. The Segment Control Register sets the count limits of the two segment counters independently and stores preset values to be loaded into the counters or current values to be read from the counters. When either of the segment counters contains a 00B, the segment pointed to for that transaction is the lowest-order 16-bit segment of the 64-bit resource involved.

The internal 16-bit databus is connected to the I/O buffer, the Instruction Register, the Address Register, the Page Address Register, the Device Select Register, the Control Register, the Segment Control Register, the Status Registers, the Next-Free-Address Register, the 802.3/802.5 format translator, and the output multiplexer. Internal 64-bit data are multiplexed and demultiplexed between the 16-bit and 64-bit buses.

The Comparand Register, the two Mask Registers, and each location in the CAM array hold 64 bits of data and are loaded via the demultiplexer over one, two, three, or four cycles, depending on the start-count and end-count values set for the destination segment counter. During loading from the I/O port, the data can be translated between IEEE 802.3 and IEEE 802.5 formats.

Instructions can move 64-bit data among the Comparand Register, the two Mask Registers, and the CAM array. The data transfers between the

Comparand Register and the CAM array can be masked by the contents of either Mask Register, as can the memory write operation.

The memory array comprises a 1k/2k x 64-bit CAM array and a 1k/2k x 2-bit validity bit array. The memory array is configurable as a CAM field and a RAM field on 16-bit boundaries. This partitioning feature allows the creation of storage space for associated data that can be stored alongside the associative data on which searches or comparisons are done. RAM segment partitions are located at the lower-order end of the 64-bit word. In other words, a 48-bit CAM, 16-bit RAM configuration will assign the RAM bits to data bits 0-15 in the array. This segment will be accessed whenever the source or destination segment counters contain a 00B value. During a compare cycle, the value held in the Comparand Register corresponding to the unmasked bits of the CAM field is compared simultaneously with all valid locations in the CAM field.

The bits of the selected Mask Register control which corresponding bits of the comparand are used in the comparison with the contents of the CAM field. If a given bit is set HIGH in the Mask Register, the corresponding bit in the CAM field is forced to match at all locations, regardless of the value of that bit in the Comparand Register. During a compare, the RAM field of the memory array is automatically excluded from the comparison.

Each memory location has a two-bit field that indicates the validity of the location. The two validity bits are designated the empty bit and the skip bit and are encoded to give the four validity conditions shown in Table 1. The unmasked portion of locations with their validity bits set to valid will enter into a comparison with the comparand during compare cycles and can be accessed randomly (read and write at address).

Table 1. Validity Bit Encoding

Skip	Empty	Condition
LOW	LOW	Valid location
LOW	HIGH	Empty location
HIGH	LOW	Temporarily withdrawn from comparison (skip)
HIGH	HIGH	Random access only

Locations that are encoded empty will not enter into a comparison; they are eligible to be randomly accessed and can be loaded by write at next-free-address cycles. Locations set to skip will not enter into a comparison; they are eligible to be randomly accessed for read or write cycles, but are considered to contain valid data, and will not be overwritten by write-at-next-free-address cycles. The skip state is used to process multiple matches. Locations set to random access will not enter into a comparison; these locations can be accessed by random-access cycles or by associative cycles that search the validity bit field for the random-access status indication. These locations are considered to contain valid data and will not be overwritten by write-at-next-free-address cycles. The random-access condition reserves in a buffer area locations that contain data such as mask or constant values and other information up to 64-bits wide. Such data will not be changed with the associative data. The validity bits can be manipulated by instructions as a function of both address and content.

Each of the 1024/2048 64-bit content fields in the memory array has a match line connected to the priority encoder. All the cells of a content field are wire-ANDed onto the match line. If any one (or more) of the nonmasked CAM cells of a valid content field differs from the corresponding bit of the comparand (a mismatch), that (or those) cell(s) pulls the match line of that content field LOW.

The priority encoder generates the address of the highest-priority content field whose match line remains HIGH during a comparison cycle. The prioritization scheme is hard-wired such that for the QS761480, the address 000H is the highest priority,

and the address 3FFH is the lowest. For the QS762470, the address 000H is the highest priority, and the address 7FFH is the lowest. The match address generated by the priority encoder is fed to the Status Register, where it can be read out on the DQ15-DQ0 bus during a command read cycle.

The match lines are also fed to the match and flag logic block which generates the external Match Flag signal ($\overline{MF}$) and the internal Match flag ($\overline{MA}$) and Multiple Match flag ($\overline{MM}$), which are sent to the Status Register. The Match flag is affected by the Match Input signal, $\overline{MI}$, in depth-expanded systems, and is further affected by the $\overline{EC}$ input. The internal $\overline{MA}$ and $\overline{MM}$ flags are **not** affected by the flag enable bits in the Control Register or the $\overline{MI}$ or $\overline{EC}$ inputs.

The empty bits in the array are connected to the priority encoder to generate the next-free-address for writes to the NFA. The empty bits are also connected to the Match and flag logic block, which generates the Full flag signal ($\overline{FF}$) and the internal Full flag ($\overline{FL}$) in the Status Register. The Full flag is affected by the Full Input signal, $\overline{FI}$, in depth-expanded systems. The internal $\overline{FL}$ flag is **not** affected by the $\overline{FI}$ input or the flag enable bits in the Control Register.

The output flags, $\overline{MF}$ and $\overline{FF}$, can be enabled and disabled independently by loading certain values into the Control Register. Since the internal flags, $\overline{MA}$, $\overline{MM}$, and $\overline{FL}$, are not controlled by external conditions, local conditions within a single QS761480/ QS762470 in a multi-device system can be determined from the Status Register.

HARDWARE DESCRIPTION

The Control Bus

Throughout the text that follows, “aaaH” represents a three-digit hexadecimal number “aaa,” while “bbB” represents a two-digit binary number “bb.”

Refer to the Block Diagram of Figure 1 for the discussion that follows. The primary control mechanism for the QS761480/QS762470 is the control bus, which comprises the chip enable ($\overline{CE}$), the write enable ($\overline{WE}$), and the command enable ($\overline{CM}$) inputs. The enable comparison ($\overline{EC}$) input of the control bus is responsible for enabling the Match flag output when LOW, but does not influence comparisons or the flow of data into or out of the device. The secondary control mechanism of the QS761480/ QS762470 is via the instructions that are loaded into the Instruction Register. Logical combinations of the control bus inputs, coupled with the execution of select persistent source (SPS), select persistent destination (SPD), and temporary command override (TCO) instructions, allow the I/O operations to and from the DQ15-DQ0 lines shown in Table 2.

The default source and destination for data read and write cycles is the Comparand Register. This default state can be overridden independently by executing a select persistent source or select persistent destination instruction. If a particular source or destination is selected, subsequent data read or write cycles will access that source or destination until another such instruction is executed. The sources and destinations available for persistent access are those resources on the 64-bit bus: Comparand Register, Mask Register 1, Mask Register 2, and the memory (CAM) array.

Table 2. Input/Output Operations

Cycle Type	$\overline{CE}$	$\overline{CM}$	$\overline{WE}$	I/O Status	Instruction Type	Operation	Notes
Com Write	L	L	L	IN	—	Load Instruction decoder	1
				IN	TCO	Load Address Register	2,3
				IN	TCO	Load Control Register	3
				IN	TCO	Load Page Address Register	3
				IN	TCO	Load Segment Control Register	3
				IN	TCO	Load Device Select Register	3
				IN	—	Deselected	9
Com Read	L	L	H	OUT	TCO	Read Next-Free-Address Register	3
				OUT	TCO	Read Address Register	3
				OUT	—	Read Status Register bits 15-0	4
				OUT	—	Read Status Register bits 31-16	5
				OUT	TCO	Read Control Register	3
				OUT	TCO	Read Page Address Register	3
				OUT	TCO	Read Segment Control Register	3
				OUT	TCO	Read Device Select Register	3
				OUT	TCO	Read current persistent source or destination	3,11
				HIGH-Z		Deselected	10
Data Write	L	H	L	IN	SPD	Load Comparand Register	6,9
				IN	SPD	Load Mask Register 1	7,9
				IN	SPD	Load Mask Register 2	7,9
				IN	SPD	Write memory array at address	7,9
				IN	SPD	Write memory array at next-free-address	7,9
				IN	SPD	Write memory array at highest-priority match	7,9
				IN		Deselected	10
Data Read	L	H	H	OUT	SPS	Read Comparand Register	6,9
				OUT	SPS	Read Mask Register 1	8,9
				OUT	SPS	Read Mask Register 2	8,9
				OUT	SPS	Read memory array at address	8,9
				OUT	SPS	Read memory array at highest-priority match	8,9
				HIGH-Z		Deselected	10
	H	X	X	HIGH-Z		Deselected	

Notes:
1. Default command write cycle destination.
2. Command write cycle destination on the consecutive command write cycle if address flag was set in bit IR11 of the instruction loaded in the previous cycle.
3. Loaded or read on the consecutive command write or read cycle after a TCO instruction has been loaded. Active for one command write or read cycle only. NFA Register cannot be loaded this way.
4. Default command read cycle source.
5. Command read cycle source on the consecutive command read cycle. If next cycle is not a command read cycle, it accesses the Status Register low-order 16-bits.
6. Default persistent source and destination on power-up and after reset. If other resources were sources or destinations, SPD CR or SPS CR restores the Comparand Register as the destination or source.
7. Selected by executing a select persistent destination.
8. Selected by executing a select persistent source instruction.
9. May require multiple 16-bit read or write cycles. Segment Control Register used to control selection of desired 16-bit segment(s) by establishing segment counters' limits and start values.
10. Device is also deselected if contents of Device Select Register do not match contents of Page Address Register except when Device Select Register contains all 1's (FFFFH). All Device Select Registers in a depth-expanded device array are written in a command write cycle immediately following a TCO with the Device Select Register as the destination.
11. TCO PS or TCO PD read back the Instruction Register bits that were last set to select a source or destination on the next cycle which must be a command read cycle.

Access to the Control Register, the Page Address Register, the Segment Control Register, the Address Register, the Next-Free-Address Register, and Device Select Register is by temporary command override (TCO) instructions which are active only for one command read or write cycle after being loaded into the Instruction Register. In other words, the override instructions are not persistent. The currently selected persistent source or destination can be read back via a TCO PS (or PD) instruction. Each control state has alternative functions, dependent on the selected temporary and permanent operating conditions.

The data and control interfaces to the QS761480/ QS762470 are synchronous. During a write cycle, the control and data inputs are registered by the falling edge of $\overline{CE}$. When writing to the persistently selected data destination, the destination segment counter is clocked by the rising edge of $\overline{CE}$. During a read cycle, the control inputs are registered by the falling edge of $\overline{CE}$, and the data outputs are enabled while $\overline{CE}$ is LOW. When reading from the persistently selected data source, the source segment counter is clocked by the rising edge of $\overline{CE}$.

The Register Set

Instruction and Address Registers

The nature of ensuing operations within the device is selected by loading the Instruction Register. Only one command write cycle is required if the instruction does not define a specific address. A second command write cycle, during which the address is presented on the DQ15-DQ0 lines and is loaded into the Address Register, is required if the instruction does require a specific address, as indicated by the address field flag in the instruction. If the instruction normally requires an address, but the address field flag is not set, then the instruction executes at the address currently pointed to by the contents of the Address Register.

The lower-order 12-bits of the Instruction Register comprise the instruction. Details of the bit allocations within this subfield are given in the “Instruction Set Description” paragraphs of the “Instruction Set” section (see p. 26-36). The upper-order 4 bits of the Instruction Register are not used. The Address Register holds the 10-bit memory address to be operated upon. Attempts to write these unused bits are ignored by the device. The unused bits are always read as zeroes during a command read operation with the Address Register as the source.

Writing to the Instruction Register can be interrupted for one command write cycle by loading a temporary command override (TCO) instruction into the Instruction Register. The next cycle must be a command write cycle and will load the Control Register, the Page Address Register, the Segment Control Register, the Device Select Register, or the Address Register, depending on the destination selected by the TCO instruction. After loading the Register selected by the TCO instruction, subsequent command write cycles are again directed to the Instruction Register until another TCO instruction is executed. Details of the instruction set are given in the “Instruction Set Description” section (see p. 27). The bit assignments for the instruction word and the Address Register are shown in Table 3. The Instruction Register is actually not a Register but the decode logic for instructions and as such, cannot be read. The persistent source and destination for data reads and writes can be read, however, by a TCO instruction .

If the Address flag is set in the instruction, the address at which the memory is to be accessed is loaded by a second command write cycle after the select persistent source memory array at address instruction. If the Address flag is not set, the memory access occurs at the address currently contained in the Address Register. Addresses can be generated in two additional ways. A new address can be forced into the Address Register by a TCO instruction that targets the Address Register and supplies an absolute address on the immediately following command write cycle. Alternatively, by correctly setting Control Register bits CT3 and CT2, the Address Register auto-increments or decrements during data writes or reads to memory at Address Register when either of the segment counters reaches its end count, or moves to memory at Address Register or VBC instructions at Address Register.

Status Register

The internal status of the QS761480/QS762470 is read from the Status Register, which is the default source for command read cycles. In the first command read cycle, bits 15-0 of the Status Register are available on DQ15-DQ0. If the next cycle is also a command read, bits 16-31 of the Status Register are available on DQ15-DQ0. If the next cycle is not a command read, on a subsequent command read cycle, bits 15-0 of the Status Register will again be accessed.

Status Register bits ST15-ST0 contain the Match flag, $\overline{MA}$, and the 10/11-bit match address from the priority encoder, AM9-AM0/AM10-AM0; they reflect the contents of the lower-order five/four bits of the Page Address Register, PA4-PA0/PA3-PA0. Bits ST31-ST16 reflect the contents of the remaining 11/12 bits of the Page Address Register, PA15-PA5/PA15-PA4, the Full flag, $\overline{FL}$, and the Multiple Match flag, $\overline{MM}$. Table 4 lists the Status Register bit assignments.

Access to the Status Register can be overridden for one command read cycle by a TCO instruction. The next cycle must be a command read cycle and will read the Control Register, the Page Address Register, the Segment Control Register, the Device

Table 3. Instruction Register and Address Register Bit Assignments

IR15	IR14	IR13	IR12	IR11	IR10	IR9	IR8	IR7	IR6	IR5	IR4	IR3	IR2	IR1	IR0
AR15	AR14	AR13	AR12	AR11	AR10	AR9	AR8	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0

	BIT	FUNCTION
QS761480	IR15-IR12	Reserved
1k x 64	IR11-IR0	Instruction bits, I11-I0
	AR15-AR10	Reserved, readback as zeros
	AR9-AR0	Address bits, A9-A0
QS762470	IR15-IR12	Reserved
2k x 64	IR11-IR0	Instruction bits, I11-I0
	AR15-AR11	Reserved, readback as zeros
	AR10-AR0	Address bits, A10-A0

Table 4. Status Register Bit Assignments

ST15	ST14	ST13	ST12	ST11	ST10	ST9	ST8	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0
ST31	ST30	ST29	ST28	ST27	ST26	ST25	ST24	ST23	ST22	ST21	ST20	ST19	ST18	ST17	ST16

	BIT	FUNCTION
QS761480	ST31	Full flag, $\overline{FL}$
1k x 64	ST30	Multiple match flag, $\overline{MM}$
	ST29-ST27	Reserved (LOW)
	ST26-ST16	Concatenated page address bits, PA15-PA5
	ST15-ST11	Concatenated page address bits, PA4-PA0
	ST10-ST1	Match address from priority encoder, AM9-AM0
	ST0	Match flag, $\overline{MA}$
QS762470	ST31	Full flag, $\overline{FL}$
2k x 64	ST30	Multiple match flag, $\overline{MM}$
	ST29-ST28	Reserved (LOW)
	ST27-ST16	Concatenated page address bits, PA15-PA4
	ST15-ST12	Concatenated page address bits, PA3-PA0
	ST11-ST1	Match address from priority encoder, AM10-AM0
	ST0	Match flag, $\overline{MA}$

Select Register, the Next-Free-Address Register, or the Address Register, depending on the source selected by the TCO instruction. After reading the Register selected by the TCO instruction, subsequent command read cycles again access the Status Register until another TCO instruction is executed. The Status Register bits will be invalidated if a write to the Page Address Register occurs.

The Control Register

The Control Register can be written to or read from by executing a TCO instruction, specifying in the instruction the Control Register as the destination or source for the next command write or read cycle, respectively. The next cycle must be a command write or read cycle. Subsequent command cycles again access the Instruction Register (write) or the Status Register (read) until another TCO instruction is executed. Writing a value to the Control Register forces a compare cycle to occur, so that the Registers are updated according to the new configuration.

The most-significant bit of the Control Register, CT15, controls the software resetting of the device. This bit of the Control Register does not physically exist and will be read back as a zero when reading the contents of the Control Register. If CT15 is LOW, the device is reset, and all lower-order bits, CT14-CT0, are ignored. The reset operation sets all locations to the empty condition (skip is LOW, empty is HIGH); the Match and Full flag outputs are enabled; the input is not translated according to the mapping between IEEE 802.3 and IEEE 802.5; the CAM/RAM partitioning is set to 64 bits CAM, 0 bits RAM; the comparison masking is disabled; the address auto-increment/autodecrement mode is disabled; the default sources and destinations are restored (Status Register and Instruction Register for command reads and writes and Comparand Register for data reads and writes); the source and destination segment counters are set to count from 00B to 11B and are loaded with 00B (this state is reflected by the value forced into the Segment Control Register); the Address Register is loaded with all zeros; the page address and Device Select Registers are left unchanged; and the value 0008H is loaded into the Control Register. The page address and Device Select Registers contain all zeros after a power-on reset. See Table 5 for the device control state after a reset command. Care must be taken to make sure that the voltage on $\overline{CE}$ rises at the same rate as V_{CC} during the power up to prevent spurious operations from occurring. To make sure that the QCAM starts from a known state, the first instructions in the initialization routine are designed to account for any spurious operations resulting from the too slow rise of the voltage on $\overline{CE}$. (See “Initializing the QCAM,” p. 24.)

Table 5. Device Control State After Reset Command

Control Register Resource	After $\overline{Reset}$, or Power-on reset*
Validity bits at all memory location	Skip = 0, Empty = 1
Match and full flag outputs	Enabled
IEEE 802.3-802.5 input translation	Not translated
CAM/RAM partitioning	64 bits CAM, 0 bits RAM
Comparison masking	Disabled
Address Register auto-increment and autodecrement	Disabled
Source and destination segment counters count ranges	00B to 11B; loaded with 00B
Address Register and next free address register	Contains all zeros
Page address and Device Select Registers	Contains all zeros*
Control Register after reset (including CT15)	Contains 0008H
Persistent destination for command writes	Instruction Register
Persistent source for command reads	Status Register (bits 15-0)
Persistent source and destination for data reads and writes	Comparand Register

***Note:** For a software reset all the conditions stay the same; PAR & DSR CONTENTS DO NOT CHANGE.

Table 6. Control Register Bit Assignments

CT15	CT14	CT13	CT12	CT11	CT10	CT9	CT8	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0

CONTROL REGISTER BIT — **FUNCTION**

CT15

CT15	
0	Reset
1	Do not reset

CT14	CT13	
0	0	Enable match flag
0	1	Disable match flag
1	0	Reserved
1	1	No change to match flag state

CT12	CT11	
0	0	Enable full flag
0	1	Disable full flag
1	0	Reserved
1	1	No change to full flag state

CT10	CT9	
0	0	Input not translated
0	1	Input translated
1	0	Reserved
1	1	No change to translation state

CT8	CT7	CT6	Seg 3	Seg 2	Seg 1	Seg 0
0	0	0	CAM	CAM	CAM	CAM
0	0	1	CAM	CAM	CAM	RAM
0	1	0	CAM	CAM	RAM	RAM
0	1	1	CAM	RAM	RAM	RAM
1	0	0	RAM	RAM	RAM	RAM
1	0	1	Reserved			
1	1	0	Reserved			
1	1	1	No change to partitioning			

CT5	CT4	
0	0	Disable comparison masking
0	1	Mask comparison with Mask Register 1
1	0	Mask comparison with Mask Register 2
1	1	No change to masking condition

CT3	CT2	
0	0	Enable address increment
0	1	Enable address decrement
1	0	Disable address increment/decrement
1	1	No change to address increment/decrement

CT1	CT0	
X	X	Reserved

If a value is loaded into the Control Register with CT15 set HIGH, then no reset occurs and the lower-order 15 bits persistently determine the settings of the device. CT1 and CT0 do not actually exist and are read back as zeros. All the control fields have an enable state, so each can be independently set, although the reset function overrides all the other control bits and prevents them from being loaded. The bit assignments for the Control Register are shown in Table 6.

Page Address Register

The Page Address Register is loaded during initialization with a specific device address. Each device in a depth-expanded system will have a different page address loaded into its Page Address Register. This page address is then used when selecting a specific chip for unconditional reads and writes by setting the Device Select Register equal to its page address. In a single-chip system, the Page Address Register and Device Select Register are normally set to the same value, not FFFFH.

The Page Address Register can be written to or read from by executing a TCO instruction, specifying in the instruction the Page Address Register to be the destination or source for the next command write or read cycle. The next cycle must be a command write or read cycle. Subsequent such cycles access the Instruction Register or the Status Register, respectively, until another TCO instruction is executed.

In a depth-expanded system, loading the individual Page Address Registers is controlled through the full-flag daisy-chain. The loading of each Page Address Register is always local, never global. Each device is selected in turn to have its page address written and is then forced full in turn, using the set full flag instruction. This procedure permits access to the next device in the chain to load its Page Address Register, which must be done before it can be selected by the global setting of the Device Select Registers.

The value written into the Page Address Register is appended to the match address that results from a compare cycle, and can be read in the combined form from the Status Register. The Page Address Register bit assignments are shown in Table 7.

Device Select Register

The Device Select Register can be written to or read from by executing a TCO instruction, specifying in the instruction the Device Select Register to be the destination or source for the next command write or read cycle. The next cycle must be a command write or read cycle. Subsequent command write or read cycles access the Instruction Register or the Status Register, respectively, until another TCO instruction is executed.

In a depth-expanded system, the Device Select Register allows a particular device to be selected for access without the need for any external decoding. A value is broadcast to all Device Select Registers via a TCO DS instruction, and only the device whose page address value matches the device select value will respond to further transactions. Device selection is overridden when the value FFFFH is written into the Device Select Registers of all devices in the

Table 7. Page Address Register Bit Assignments

PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0

BIT	FUNCTION
PA15-PA0	Page address

Table 8. Device Select Register Bit Assignments

DS15	DS14	DS13	DS12	DS11	DS10	DS9	DS8	DS7	DS6	DS5	DS4	DS3	DS2	DS1	DS0

BIT	FUNCTION
DS15-DS0	Device select value

array. The loading of the Device Select Registers is always global, never local. The Device Select Register bit assignments are shown in Table 8.

Segment Control Register

The Segment Control Register controls which data segment is addressed and is written to or read from by executing a TCO instruction with the Segment Control Register as the destination or source for the next command write or read cycle. The next cycle must be a command write or read cycle. Subsequent command write or read cycles access the Instruction Register or the Status Register, respectively, until another TCO instruction is executed.

The Segment Control Register bit SC15 enables the loading of SC14-SC11, which set the destination segment counter limits. SC10 enables the loading of SC9-SC6, which set the source segment counter limits. SC5 enables the loading of SC4 and SC3 into the destination segment counter. SC2 enables the loading of SC1 and SC0 into the source segment counter. When the Segment Control Register is read, SC4 and SC3 contain the current value of the destination segment counter, and SC1 and SC0 contain the current value of the source segment counter. The enable bit for each of the control fields allows each to be set independently.

If the source or destination segment counter load values are outside the count limits, the value is loaded into the counter, which then increments, once per data read or write cycle on the rising edge of $\overline{CE}$, until the end-count value is reached. On the next clock cycle, the counter returns to the start-count value. On subsequent cycles, the count is from start count to end count. Operations that generate an automatic compare do so when the actual segment counter value equals the end-count value stored in the Segment Control Register. If operations that are loading data with more than one segment are interrupted, care must be taken to keep track of the values in the respective segment counters so that the operation may be resumed without error. The bit assignments for the Segment Control Register are shown in Table 9.

The segment counters control the multiplexing and demultiplexing between the 64-bit and 16-bit resources on the chip. When the memory array has been partitioned into RAM and CAM subfields, the RAM subfields are assigned to the lower-order segments. Thus, if the memory array is configured to be 16 bits of RAM and 48 bits of CAM, as is likely in address-filtering applications, the associated data stored in the RAM segment are accessed when the source or destination segment counter contains a 00B value.

Comparand Register

The Comparand Register contains the data value against which the unmasked portion of the CAM array contents is compared. The Comparand Register is the default source and destination for data read and write cycles. During a data write cycle, the Comparand Register is loaded in one, two, three, or four cycles, depending on the start-count and end-count values of the destination segment counter. Each falling edge of $\overline{CE}$ Registers a 16-bit segment of data from DQ15-DQ0 into the Comparand Register. Each rising edge of $\overline{CE}$ increments the destination segment counter. During a data read cycle, the Comparand Register is accessed in one, two, three, or four cycles, depending on the start-count and end-count values of the source segment counter. Each falling edge of $\overline{CE}$ enables the DQ15-DQ0 outputs, while each rising edge of $\overline{CE}$ increments the source segment counter and turns off the DQ15-DQ0 outputs.

Default read or write access to the Comparand Register can be overridden by executing a select persistent source (SPS) or select persistent destination (SPD) instruction. The persistent source and destination of data during a data read or data write cycle can be selected independently. The sources and destinations that can be selected on a persistent basis for data during a data read or write cycle are either of the Mask Registers or the memory array with various combinations of status conditioning or addressing. The bit assignments for the Comparand Register are shown in Table 10.

Table 9. Segment Control Register Bit Assignments

SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0

SEGMENT CONTROL REGISTER BIT				FUNCTION
SC15				
0				Set destination segment counter limits
1				No change to destination segment counter limits
SC14	**SC13**	**SC12**	**SC11**	
0	0	0	0	Destination count start 00, end 00
0	0	0	1	Destination count start 00, end 01
0	0	1	0	Destination count start 00, end 10
0	0	1	1	Destination count start 00, end 11
0	1	0	0	Reserved
0	1	0	1	Destination count start 01, end 01
0	1	1	0	Destination count start 01, end 10
0	1	1	1	Destination count start 01, end 11
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Destination count start 10, end 10
1	0	1	1	Destination count start 10, end 11
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Destination count start 11, end 11
SC10				
0				Set source segment counter limits
1				No change to source segment counter limits
SC9	**SC8**	**SC7**	**SC6**	
0	0	0	0	Source count start 00, end 00
0	0	0	1	Source count start 00, end 01
0	0	1	0	Source count start 00, end 10
0	0	1	1	Source count start 00, end 11
0	1	0	0	Reserved
0	1	0	1	Source count start 01, end 01
0	1	1	0	Source count start 01, end 10
0	1	1	1	Source count start 01, end 11
1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Source count start 10, end 10
1	0	1	1	Source count start 10, end 11
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Source count start 11, end 11
SC5				
0				Load destination segment counter
1				No change to destination segment counter

(continued)

Table 9. Segment Control Register Bit Assignments (continued)

SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0

SEGMENT CONTROL REGISTER BIT		FUNCTION
SC4	**SC3**	
0	0	Load destination segment counter with 00
0	1	Load destination segment counter with 01
1	0	Load destination segment counter with 10
1	1	Load destination segment counter with 11
SC2		
0		Load source segment counter
1		No change to source segment counter
SC1	**SC0**	
0	0	Load source segment counter with 00
0	1	Load source segment counter with 01
1	0	Load source segment counter with 10
1	1	Load source segment counter with 11
		Note: Bits 2, 5, 10, 15 are read back as zeros.

Table 10. Comparand Register Bit Assignments

CR63-CR48	CR47-CR32	CR31-CR16	CR15-CR0
Comparand Register Segment 3	Comparand Register Segment 2	Comparand Register Segement 1	Comparand Register Segment 0

Mask Register 1 and Mask Register 2

Mask Registers 1 and/or 2 can be chosen as the persistent source and/or destination for data read or write cycles by executing a SPS Mask Register 1 (or 2) or SPD Mask Register 1 (or 2) instruction. Once chosen, the Mask Register remains the source or destination for subsequent data read or write cycles until another source or destination is chosen via an SPS or SPD instruction, or with a reset occurs.

Mask Register 1 or 2 can also be selected to mask compare cycles through bits CT5 and CT4 in the Control Register. Masking of data write and data Move operations is controlled by instruction. In a compare operation, if a Mask Register has been enabled, bits set LOW in the Mask Register cause corresponding bits throughout the CAM array to be compared with Comparand bits. Bits set HIGH in the Mask Register force a match between corresponding bits in the CAM array and Comparand bits so they become “don’t cares.” During masked data write and move cycles, destination bits corresponding to LOW values in the selected Mask Register are updated, while bits corresponding to HIGH values in the selected Mask Register remain unchanged. The bit assignments for Mask Registers 1 and 2 are shown in Table 11.

Next-Free-Address Register

The Next-Free-Address Register is a read-only register that contains the memory address of the next free address in the memory array. See Table 12 for bit assignments. The QCAM generates this address automatically by internally feeding the validity bits to the priority encoder, determining the lowest numerical memory address that is empty and storing that

address location in the Next-Free-Address Register. The Next-Free-Address Register is updated during any instruction that could potentially change the state of the validity bits (e.g., write to memory, move to memory, and VBC instructions). The new address stored will be the next numerically higher empty memory address. The stored memory address is available to the user by issuing a TCO NF command. This address is also used as a pointer to the memory array during a write at next-free-address cycle. In a depth-expanded system, the Full flag daisy-chain causes only the device that is not full and whose $\overline{FI}$ input is low to respond during a write at next-free-address cycle. Disabling the Full flag in the Control Register of a particular device also disables the ability of that device to write at next-free-address.

The Memory Array

The memory array is organized as 1024/2048 64-bit locations, each having two validity bits, the skip bit and empty bit. By default each location is a 64-bit CAM cell. However, the array can be reconfigured by writing to the Control Register to divide each location into a CAM field and a RAM field. The RAM field is assigned to the lower-order segments, starting with segment 0. The CAM/RAM partitioning is allowed on 16-bit boundaries, permitting selections of 64 CAM bits, 0 RAM bits; 48 CAM bits, 16 RAM bits; 32 CAM bits, 32 RAM bits; 16 CAM bits, 48 RAM bits; 0 CAM bits, 64 RAM bits. Memory array bits designated to be RAM bits can be used to store and retrieve associated data (data associated with a CAM content). The bit assignments for the memory array are shown in Table 13.

Read Memory at Address

The memory array can be selected as the persistent source for data read cycles as a function of a specified address by executing a select persistent source memory array at address instruction. If address auto-increment/decrement is enabled (via CT3, CT2), the source address automatically increments/decrements once the destination count returns to its lowest value on subsequent read cycles. If address auto-increment/decrement is disabled, the same address will remain the source for subsequent read cycles or until another destination is selected by executing a SPS instruction. Refer to Table 15 for reading preconditions.

Read Memory at Highest-Priority Match Address

Once a compare cycle establishes a match, the memory array can be selected as the persistent source for data read cycles as a function of the highest-priority match address by executing a select

Table 11. Mask Register 1 and 2 Bit Assignments

MX63-MX48	MX47-MX32	MX31-MX16	MX15-MX0
Mask Register 1 or 2 Segment 3	Mask Register 1 or 2 Segment 2	Mask Register 1 or 2 Segment 1	Mask Register 1 or 2 Segment 0

Table 12. Next-Free-Address Register Bit Assignments

NFl5	NF14	NF13	NF12	NF11	NF10	NF9	NF8	NF7	NF6	NF5	NF4	NF3	NF2	NF1	NF0
		BIT					**FUNCTION**								
QS761480		NF15-NF10 ..... Reserved													
1k x 64		NF9-NF0 ..... Next free address													
QS762470		NF15-NF11 ..... Reserved													
2k x 64		NF10-NF0 ..... Next free address													

persistent source memory array at the highest-priority match address. Once selected to be accessed at the highest-priority match address, the memory array at the highest priority match address remains the source for subsequent data read cycles until another source is selected by executing a SPS instruction.

No explicit address field is required to access the memory during these associative read cycles. Instead, the memory is addressed as a function of the highest-priority location whose CAM field contents match the contents of the Comparand Register taking the selected Mask Register, if any, into account. The comparison may or may not be masked by the contents of Mask Register 1 or Mask Register 2, depending on what comparison conditions have been selected by earlier instructions written to the device.

If no match exists between the contents of the Comparand Register and the contents of the CAM section of the memory array, the DQ15-DQ0 bus remains in the high-impedance state to facilitate the daisy-chain operation. If enabled, $\overline{MF}$ will indicate whether or not a match has occurred. In a daisy-chained system, only the highest-priority responding device, if any, will be accessed by a data read cycle. For this reason, the $\overline{MF}$ line must be enabled and checked by the system to determine the no-match condition in depth-expanded systems. If the daisy-chain feature is not used, individual devices can still be accessed if the contents of their Page Address Register match those of their Device Select Register.

If a context-specific operation is desired where a particular device's Status Register is to be queried, the DQ15-DQ0 lines of that device will be enabled for one or more command read cycles if its Device Select Register's contents match its Page Address Register's contents. In this case, the selected device's $\overline{MA}$, $\overline{MM}$, and other Status Register bits can be used to reflect a match or no-match condition.

Write Memory at Address

The memory array can be selected as the persistent destination for data write cycles as a function of a specified address by executing a select persistent destination (SPD) memory array at address instruction. If address auto-increment/decrement is enabled (via CT3, CT2), the destination address automatically increments/decrements once the destination count returns to its lowest value on subsequent write cycles. If address auto-increment/decrement is disabled, the same address will remain the destination for subsequent write cycles or until another destination is selected by executing a SPD instruction. Refer to Table 15 for writing pre-conditions.

The data write to the memory array may be masked by either Mask Register 1 or 2, depending on the conditions set up by the SPD instruction. During the cycle in which the last 16-bit segment of the current data word is written into the memory array, the validity of the addressed location will be set according to the condition specified by the SPD instruction most recently executed.

Write Memory at Highest-Priority Match Address

After a compare cycle establishes a match, the memory array can be selected as the persistent destination for data write cycles as a function of the highest-priority match address by executing a select persistent destination memory array at highest-priority match address instruction. Once selected, the memory array at the highest-priority match address remains the destination for subsequent data write cycles until another destination is selected by executing a SPD instruction.

No explicit address field is required to write the memory during these associative write cycles. Instead, the memory is addressed at the highest-priority location having CAM-field contents match with the contents of the Comparand Register taking the selected Mask Register, if any, into account. The comparison could

Table 13. Memory Array Bit Assignments

D63-D48	D47-D32	D31-D16	D15-D0
Memory Array Segment 3	Memory Array Segment 2	Memory Array Segment 1	Memory Array Segment 0

be masked by the contents of Mask Register 1 or 2, depending on what comparison conditions have been selected by previous instructions.

The write to memory array operations may be masked by either Mask Register 1 or Mask Register 2, depending on the conditions set up by the select persistent destination instruction. During the cycle in which the last 16-bit segment of the current data word is written into the memory array, the validity of the addressed location will be set according to the condition specified by the select persistent destination instruction most recently executed.

Write Memory at Next Free Address

The memory array can be selected as the persistent destination for data write cycles as a function of the next free address by executing a select persistent destination (SPD) memory at next-free-address instruction. After data are loaded at this address and the destination count has reached its lowest value, a new destination is established at the next free address. Therefore, subsequent writes will continue to fill the memory array until full or until another destination is selected by executing a SPD.

If the QCAM becomes full and no locations indicate empty by the 2-bit validity encoding, the data input port enters a high-impedance state at further write attempts. Since there are no next-free-addresses, no more data can be entered into the QCAM until another SPD instruction is executed or the validity bits associated with a certain address indicates an empty status.

No explicit address field is required to write to the memory during these Associative write cycles. Instead, the memory is addressed as a function of the next free location. The QCAM generates this address automatically by internally feeding the validity bits to the Priority encoder. The next free address is contained in the Next-Free-Address Register which can be read (but not written) using the TCO NF instruction.

The write at next-free-address cycle can be used in a depth-expanded system when the full flags are daisy-chained. When a write at next-free-address cycle is broadcast, the first device in the daisy-chain that is not full and whose $\overline{FI}$ input is LOW will respond to the write cycle storing the data in the address pointed to by the Next-Free-Address Register.

The write to the memory array may be masked by either Mask Register 1 or 2, depending on the conditions set up when loading the select persistent destination instruction. During the cycle in which the last segment of the current data word is written into the memory array, the validity bits of the addressed location are set according to the condition specified by the select persistent destination instruction most recently executed. Data move instructions from the Comparand Register and the two Mask Registers to the memory array either set the location valid or leave the validity bits unchanged, depending on the instruction.

APPLICATIONS

I/O Cycles

The QS761480/QS762470 supports four basic I/O cycles: data read, data write, command read, and command write. The nature of a particular cycle is determined by the states of the $\overline{WE}$ and $\overline{CM}$ control inputs. These signals are registered at the beginning of a cycle by the falling edge of $\overline{CE}$. Table 14, a summary of Table 15, shows how the $\overline{WE}$ and $\overline{CM}$ lines select the cycle type.

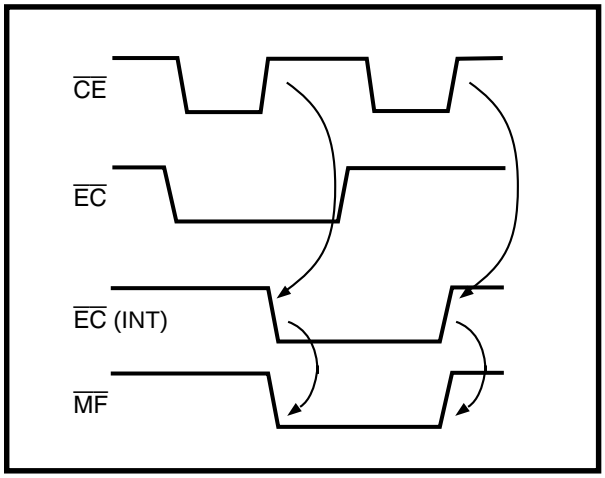
During read cycles, the outputs are enabled when $\overline{CE}$ is LOW. During write cycles, the data or command to be written is captured at the beginning of the cycle by the falling edge of $\overline{CE}$. Figures 11 and 12 (p. 41 and 42) show read and write cycles respectively. Figures 13-15 (p. 42-44) show the match cycle of a stand-alone QCAM as well as 3 daisy-chained QCAMs. Figure 16 (p. 45) shows cycle-to-cycle timing with the Match flag valid at the end of the third load cycle if $\overline{EC}$ is LOW at the start of the third cycle. The compare operation automatically occurs when the segment counter reaches the end count set in the Segment Control Register (for data writes to the Comparand or Mask Registers). The fourth cycle reads status or associated data, depending on the state of $\overline{CM}$. For depth-expanded devices, $\overline{EC}$ is held LOW for the fourth cycle to continue the locked daisy-chain until the second read cycle is complete. Figure 4 shows how the internal $\overline{EC}$ timing holds the daisy-chain

locking effect holds over into the next cycle. In a single-chip system with DS=PA, taking $\overline{EC}$ HIGH for the fourth cycle will allow status reads with a match. Inserting a NOP takes $\overline{EC}$ HIGH to read the status without a match. Refer to Table 15, "Operational Truth Table."

Table 14. Summary of I/O Cycles

$\overline{WE}$	$\overline{CM}$	Cycle Type
LOW	LOW	Command write cycle
LOW	HIGH	Data write cycle
HIGH	LOW	Command read cycle
HIGH	HIGH	Data read cycle

Figure 4. $\overline{EC}$ Internal Timing Diagram



Because the QS761480/QS762470 does not use an address bus, the device can be memory mapped in a system, which sees the device as four locations: reading and writing command and data resources. The four locations correspond to the logical combinations of the $\overline{CM}$ and the $\overline{WE}$ control inputs. The $\overline{EC}$ control input enables the comparison flag, $\overline{MF}$, provided CT13 and CT14 are appropriately set, and activates the daisy-chain in a depth-expanded system.

Quite often, an external state machine is constructed to provide the proper control signal sequences and timing to the QS761480/QS762470. Such logic can provide the non-symmetrical $\overline{CE}$ signal needed in time-critical applications. Note in the “Switching Characteristics” chart of Table 24, the minimum values for t_{CEH} and t_{CEL}, below which the QS761480/QS762470 may not provide proper operation under voltage and temperature extremes. t_{CEH} varies, based on the type of cycle being performed, as defined in the notes to the timing specifications, with memory access cycles being longer than others. Thus, the user can take advantage of faster cycles such as writing to the Comparand Register without a compare, or reading the Status Register.

Depth Expansion

The QS761480/QS762470 can be depth-expanded in a system to increase its depth. The depth expansion uses a daisy-chaining technique that allows system prioritizing of the match response and control of the memory-full status. The 5ns (worst case) serial delay per device in the daisy-chained depth-expanding can easily be handled in the system. Should this delay be too long, the daisy-chaining need not be used, and system match ordering can be done with external logic.

Daisy-chaining is achieved through the $\overline{FI}$ and $\overline{FF}$ flags for the full indication, and the $\overline{MI}$ and $\overline{MF}$ flags, controlled by the $\overline{EC}$ input, for the match indication. The two expanding processes can be used independently. In other words, the full flag cascading can be used, and the match flags can be prioritized externally, or both expansion schemes can be used together. A system in which four QS761480/QS762470s are depth-expanded using daisy-chaining for both the full and match flags is shown in Figure 5.

Locked Daisy-chain

In a locked daisy-chain, the highest-priority device is the one with $\overline{MI}$ HIGH and $\overline{MF}$ LOW. Only this device will respond to command and data reads and writes, regardless of the state of the Device Select Registers and Page Address Registers, with the following exceptions: write to Device Select Register is always active in all devices; write to Page Address Register is always active in the device with $\overline{FI}$ LOW and $\overline{FF}$ HIGH; and, the set full flag (SFF) instruction is always active in the device with $\overline{FI}$ LOW and $\overline{FF}$ HIGH.

Table 15. Operational Truth Table

Case	$\overline{EC}$(int)	$\overline{MA}$(int)	$\overline{MI}$	Device Select Reg.	Command Write(1)	Data Write(1)	Command Read(1)	Data Read(1)
1	1	X	X	DS=FFFFH	YES	YES	NO	NO
2	1	X	X	DS=PA	YES	YES	YES	YES
3	1	X	X	DS≠FFFFH and DS≠PA	NO	NO	NO	NO
4	0	X	0	X	NO	NO	NO	NO
5	0	1	1	X	NO	NO	NO	NO
6	0	0	1	X	YES	YES	YES	YES

Where:

$\overline{EC}$(int) = the $\overline{EC}$ internal signal that indicates whether the daisy-chain is locked or unlocked

$\overline{MA}$(int) = the internal match flag that indicates whether the device had a match or not (available as an external signal in the QS762470)

$\overline{MI}$ = the match input signal that indicates whether there was a match further up the daisy-chain or not

DS = the Device Select Register

PA = the Page Address Register X = Don't Care

Notes:

1. Exceptions are: **A.** Write to Device Select Register is always active in all devices, **B.** Write to Page Address Register is active in the device with $\overline{FI}$ LOW and $\overline{FF}$ HIGH; **C.** the Set Full Flag (SFF) instruction is active in the device with $\overline{FI}$ LOW and $\overline{FF}$ HIGH.

Table 15 shows the response of the QCAMs to reads or writes, based on the state of $\overline{EC}$. $\overline{EC}$(int) is registered from the external $\overline{EC}$ pin on the rising edge of $\overline{CE}$, so it controls what happens in the next cycle. When you first take $\overline{EC}$ LOW in a chain of QCAM devices (and assuming the Device Select Registers are all set to FFFFH), all devices will respond to that command write or data write. However, when DS=FFFFH, none of the devices will respond to a command read or data read to prevent data bus contention (see Case 1 of Table 15). From then on the daisy-chain is locked and on subsequent cycles when $\overline{EC}$ is kept LOW on the falling edge of $\overline{CE}$, only the highest priority device will respond. (See Case 6 of Table 15.) If, for example, all of the CAM memory locations were empty, there would be no match, and $\overline{MF}$ would be HIGH. Since none of the devices could then be the highest priority device, none will respond to reads or writes except as noted above.

If there is a match between the data in the Comparand Register and a location or locations in memory, then only the highest-priority device will respond to a status read. If there isn't a match then an NOP with $\overline{EC}$ HIGH needs to be inserted before a write to the next free address is executed. To read the Status Registers of specific devices when there is no match requires the use of the TCO DS command to set DS=PA of each device.

Interconnecting Full Flags

The full flag daisy-chain is used to point the system to the first device with an empty location. Referring to Figure 5, the condition that the full flag is set LOW in a particular device is that the $\overline{FI}$ input is LOW, and that device is full. If the $\overline{FI}$ input is HIGH, at least one (or more) location(s) is free above that device.

Under this circumstance whether or not that particular device is full, its $\overline{FF}$ flag will remain HIGH. In this way, system-full indication takes into account free locations in devices higher up in the daisy-chain.

The daisy-chain also allows write-at-next-free-address cycles to operate globally over the entire system, and not just locally in a device. All devices in the system can be set to have memory at-next-free-address selected as their persistent destination for data write cycles. Data write cycles can then be broadcast to all devices. Only the device in which $\overline{FI}$ input is LOW, and which is not full, will respond to the write cycle. This scheme allows deletions and insertions to take place in the memory automatically, without the need to keep track of addresses. The daisy-chaining also gives a system-full indication. When the device at the end of the chain has its $\overline{FF}$ LOW, the system must be full. The first device in the chain must have its $\overline{FI}$ input tied LOW. The truth table for the full flag cascading is shown in Table 16.

Table 16. Full Flag Cascading Logic

$\overline{FI}$	Device Full	$\overline{FF}$	Write @ Next Free Address
LOW	NO	HIGH	YES
LOW	YES	LOW	NO
HIGH	NO	HIGH	NO
HIGH	YES	HIGH	NO

Interconnecting Match Flags

Referring to Figure 5, the match flag will be LOW in a particular device if its $\overline{MI}$ input is LOW, or if there is a match in that device and the match flag is enabled in the Control Registers of all devices in the daisy-chain. If the $\overline{MI}$ input is LOW, there is one (or more) matching location(s) above that device. Under this circumstance, whether or not that particular device has a match, its $\overline{MF}$ flag will be forced LOW. In this way, the system-match indication flags match locations in devices higher up in the daisy-chain.

The daisy-chain also controls access to the highest-priority Status Register, and allows data-reads from and writes-to the highest-priority matching address to operate over the entire system, and not just in one device. When a command read cycle is broadcast to the CAM system, access is allowed to the Status Register of the device which has its $\overline{MI}$ input HIGH and has a match. Similarly, all devices in the system can be set to have memory at highest-priority match as their persistent source or destination for data read or write cycles. Data read or write cycles can then be broadcast to all devices. Only the device in which the $\overline{MI}$ input is HIGH and that has a match will respond to the read or write cycle. This scheme automatically prioritizes a system of depth-expanded devices: the highest up in the chain has the highest priority.

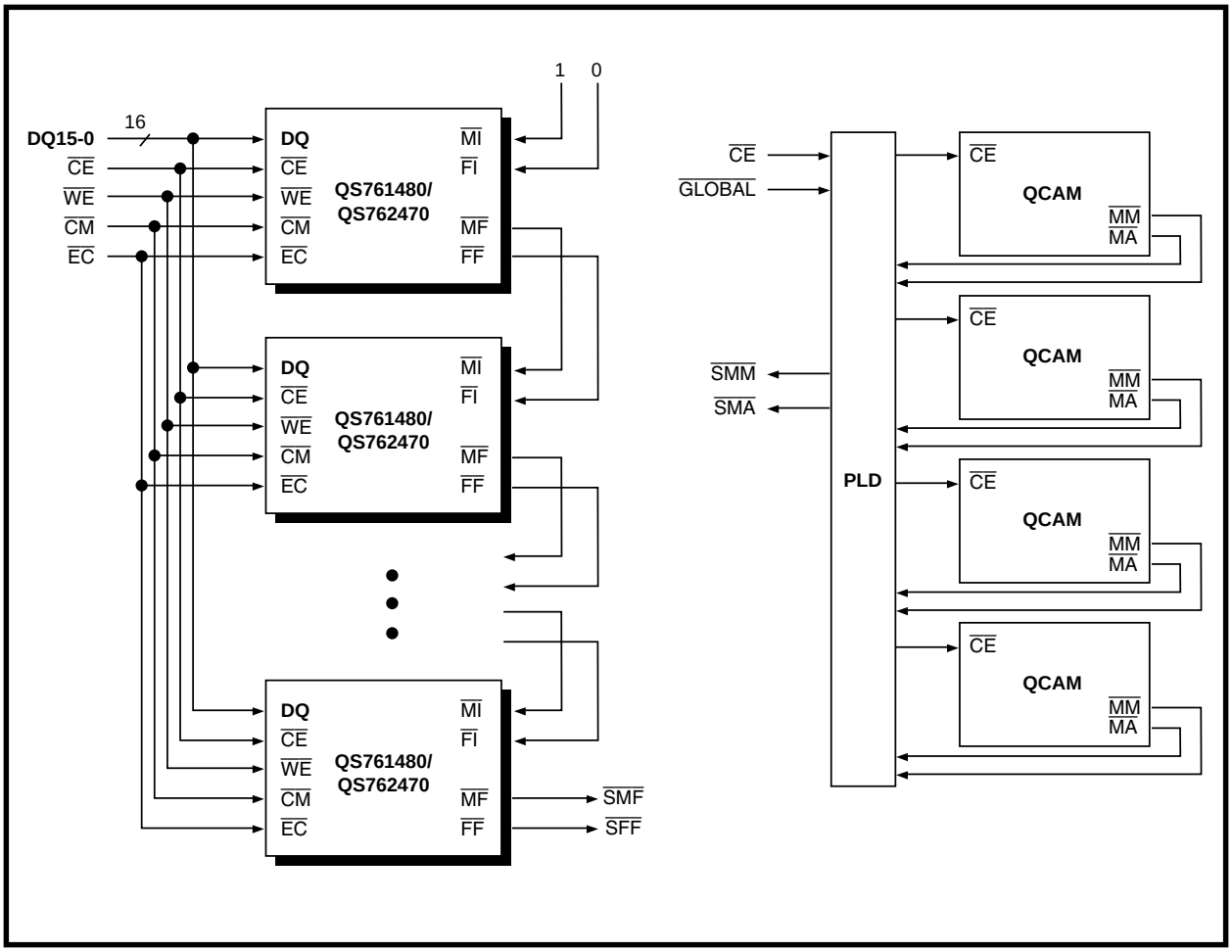
The daisy-chaining also gives a system-match indication. When the end device of the chain has its $\overline{MF}$ LOW, the system has a match in one or more devices. The $\overline{MI}$ input of the first device in the chain is tied HIGH. The truth table for the Match flag cascading is shown in Table 17.

Table 17. Match Flag Cascading Logic

$\overline{MI}$	Match	$\overline{MF}$	Access Status Reg.?
LOW	NO	LOW	NO
LOW	YES	LOW	NO
HIGH	NO	HIGH	NO
HIGH	YES	LOW	YES

Indication of the match condition within the system takes some time to establish itself once a comparand is loaded. The compare time in each device operating in parallel is added to the ripple delay through the daisy-chain. Before reading the results of a comparison, either through the Status Register or the system match flag, the daisy-chain must be given time to settle to a valid state. The $\overline{CE}$ HIGH time must be larger than the time for $\overline{MF}$ to assert plus the sum of the $\overline{MI}$-to-$\overline{MF}$ ripple-through, so that only one device with a match in a daisy-chain will respond. If there are N devices depth-expanded in a system, and the time to get a valid output on $\overline{MF}$ is $t_{\overline{MF}}$, and the time for the flag to ripple through a device from

Figure 5. Depth Cascaded QCAMs



$\overline{MI}$ valid to $\overline{MF}$ valid is $t_{\overline{MI}\text{-to-}\overline{MF}}$, then the time t_{DC} for the daisy-chain to develop a valid output condition is:

$$t_{DC} = t_{\overline{MF}} + (N–1) \bullet t_{\overline{MI}\text{-to-}\overline{MF}}$$

To assist in accessing the results of a daisy-chained comparison, and overriding the control the daisy-chain exerts on the system, the $\overline{EC}$ control input enables and disables the $\overline{MF}$ outputs in a special way. When $\overline{EC}$ is HIGH at the falling edge of $\overline{CE}$ at the beginning of any cycle, the $\overline{MF}$ output is forced HIGH, regardless of the match conditions in the device. When $\overline{EC}$ is LOW at the beginning of a cycle, it enables the $\overline{MF}$ output to respond to the $\overline{MI}$ input, the $\overline{MF}$ enable/disable control, and the match conditions in the device. The captured state of the $\overline{EC}$ input remains in effect after the end of the cycle until it changes to another state at the beginning of a subsequent cycle. The $\overline{EC}$ timing ensures that there are no false transitions on the $\overline{MF}$ line prior to establishing local match conditions.

$\overline{EC}$ allows the comparison and daisy-chain rippling to take place between device cycles. If, for example, a 48-bit comparand is broadcast to all the QS761480/QS762470s in a daisy-chained system, the $\overline{EC}$ line is driven HIGH during the writing of the first two segments. During the writing of the third segment, the $\overline{EC}$ line is driven LOW, and the flags are valid at the end of the last load. Now the associated data or Status Register can be read as a function of the highest-priority match within the system, as long as sufficient time is allowed for the daisy-chain ripple to complete. The $\overline{EC}$ line is captured internally on each

CAM device, enabling the daisy-chain to remain locked while the devices are not being accessed. Figure 5 also shows prioritizing scheme to resolve highest priority $\overline{MA}$ and $\overline{MM}$ signals by using $\overline{CE}$ and $\overline{GLOBAL}$ signals in a PLD.

Depth-Expansion System Initialization

In a depth-expanded system, the user can set the contents of individual Page Address Registers for subsequent local access by using the page address initialization mechanism. This process obviates the need for external decoding. The Page Address Register initialization works through the full flag cascading feature. The $\overline{FF}$ output of one device is connected to the $\overline{FI}$ input of the next-lower-priority device in the daisy-chain. The highest-priority device has its $\overline{FI}$ input tied LOW. While a device's $\overline{FI}$ input is LOW, and the device is not full ($\overline{FF}$ is HIGH), it responds to write-at-next-free-address cycles. Once full, the $\overline{FF}$ flag goes LOW, pulling $\overline{FI}$ of the next-lower priority device LOW, thereby allowing that device to respond to write-at-next-free-address cycles.

The instruction Full flag set forces the $\overline{FF}$ output LOW in the currently writing device. The Page Address Register of the first device can be loaded, its $\overline{FF}$ can then be forced LOW by this instruction, and the Page Address Register of the next-lower-priority device can be loaded. This process continues until all of the Page Address Registers have been loaded. Note that the writes to the Page Address Register are never broadcast. They take place only in the device whose $\overline{FI}$ input is LOW, and whose $\overline{FF}$ output is HIGH. Once all Page Address Registers are initialized, a software reset command is issued that forces all the $\overline{FF}$ outputs HIGH. Note that this software reset command does not alter the contents of the Page Address Register (see Table 5).

Random Access for Depth-Expanded Systems

The Device Select Register allows random access to a single device in the daisy-chain once the Page Address Registers have been initialized. Random access into a daisy-chained system works by sending a device select value to all the Device Select Registers that corresponds to the page address of the target device using the temporary command override (TCO) instruction.

Access to all resources of a given device is conditioned by the Device Select Register of that device. Only the device which has a match between its Page Address Register and its Device Select Register will respond to access cycles. The effects of the Device Select Register can be switched off by loading a special value, FFFFH. When this value is loaded into the Device Select Register, the comparison with the contents of the Page Address Register is inhibited. Write cycles to the Registers and memory of devices within a daisy-chained system are then broadcast, and all devices receive the data, such as when an instruction is sent to the CAM array.

When access to a specific device is required, the page address of that device is broadcast to all the Device Select Registers using a TCO DS, command write instruction sequence. Now only the device with a match between the contents of the Page Address and Device Select Registers will respond to subsequent command and data read and write cycles, until the value FFFFH is broadcast to the Device Select Registers of all the devices in the system. This ability to switch on and off the device select function allows local or global transactions within the system.

All random access and Register reads are inhibited for data and command read cycles when global access is enabled (by loading the Device Select Registers with the value FFFFH) to prevent bus contention from multiple devices presenting the requested data simultaneously. All associative reads resulting from a match being detected during a compare operation are allowed because the internal priority encoders and the daisy-chaining of the match flag signal allow only access to a single device at a time.

Each Page Address Register must contain a unique value to prevent the potential for bus contention. This situation is analogous to a RAM memory system where more than one select line is activated. An error like this should be removed in debugging the design. An application programmer should not have access to such low-level system functions as the loading of Page Address Registers. That task will be implemented in or controlled by the firmware that initializes the depth-expanded QCAM system. The implications to the user of being able to select between local and global access are far-reaching.

This facility makes possible run-time switching into a context-specific mode.

IEEE 802.3/802.5 Format Mapping

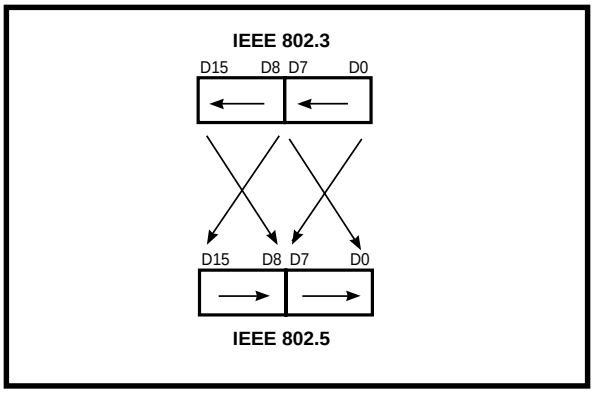
To support the symmetrical mapping between the address formats of IEEE 802.3 and IEEE 802.5, the QS761480/QS762470 provides a bit translation facility in the control space. Formally expressed, the nth input bit, D(n), maps to the xth output bit, Q(x), through the following expression:

$$D(n) = Q(7–n) \text{ for } 0 < n < 7, \text{ and}$$

$$D(n) = Q(23–n) \text{ for } 8 < n < 15$$

Setting Control Register bits 10 and 9 selects whether to persistently translate, or persistently not to translate, the data written onto the 64-bit internal bus. The default condition on power-up and after a Reset command is not to translate the incoming data. Figure 6 shows the bit mapping between the two formats.

Figure 6. Bit Mapping Between IEEE 802.3 and IEEE 802.5



Initializing the QCAM

Since the QS761480/QS762470 is controlled by a combination of input signals and instructions, some initialization is required to configure the device. Every effort has been made to make the default configuration of the device on power-up and after a reset operation as useful as possible. However, since applications for this device vary widely, the default states will not be suitable for all applications. Refer back to Table 5 for the device's control states after a reset operation.

Table 18 shows an example of code that initializes a depth-expanded string of QCAM devices. This example is illustrative only and may not represent the most efficient way to perform an initialization, nor what a particular application would find most useful. Each system designer should plan his or her own routine to initialize the device(s), based on the particular application. The initialization example shows how to set the Page Address Registers of each of the devices in the chain through the use of the set full flag instruction, and how the Control Registers and segment counters of all the QCAM devices are set to load 48-bit addresses. The first command write of 0000H is provided to take care of the situation of an anomalous power-up state caused by a too slow rise of the voltage on $\overline{CE}$ relative to V_{CC}, and will place the device in a known initial state by resetting the internal two-cycle state machines.

For normal filtering operation, network data are loaded into the Comparand Registers of all the devices in a string simultaneously by setting DS=FFFFH. Reading is prohibited when DS=FFFFH except for the device with a match. For a diagnostic operation you need to select a specific device by setting DS=PA for the desired device to be able to read from it. Refer to Table 15 for preconditions for reading and writing.

Table 18. Example Initialization Routine

CycleType	Opcode or Data on Data Bus	Control Bus $\overline{CE}$	$\overline{CM}$	$\overline{WE}$	$\overline{EC}$	Comments	Notes
Command Write	0000H	L	L	L	H	Accounts for power-up anomalies	
Command Write	TCO DS	L	L	L	H	Target device select register to disable local device selection	
Command Write	FFFFH	L	L	L	H	Disables device select feature	
Command Write	TCO CT	L	L	L	H	Target control register for reset	1
Command Write	0000H	L	L	L	H	Causes reset	1
Command Write	TCO PA	L	L	L	H	Target page address register to set page for cascaded operation	
Command Write	nnnnH	L	L	L	H	Page address value	
Command Write	SFF	L	L	L	H	Set full flag; allows access to next device (repeat previous 2 instructions plus this one for each device in chain)	2
Command Write	TCO CT	L	L	L	H	Target control register for reset of full flags, but not page address.	1
Command Write	0000H	L	L	L	H	Causes reset	1
Command Write	TCO CT	L	L	L	H	Target control register for initial values	3
Command Write	8040H	L	L	L	H	Control register value	3
Command Write	TCO SC	L	L	L	H	Target segment counter control register	
Command Write	39C9H	L	L	L	H	Set both segment counters to load segments 1, 2, and 3 (48 bits), starting with segment 1.	

Notes:
1. The TCO CT immediate field-bit assignments translate to 0000H for the reset operation. The default power-up condition generates the same effect, but good programming practice dictates a software reset for initialization to account for all possible conditions.
2. This instruction may be omitted for a single QS761480/QS762470 application. The last SFF will cause the MF pin in the last chip in a daisy chain to go LOW. In a daisy chain, DS needs to be set equal to PA to read out of a particular chip prior to a match condition.
3. Typical QCAM control environment:
   Enable match flag
   Enable full flag
   Input not translated
   48 CAM bits, 16 RAM bits
   Disable comparison masking (can be changed as required)
   Enable address increment
   This example translates to 8040H. See Table 6 for control register bit assignments.

Table 18a. Instruction Cycle Lengths

Cycle Length	Command Write	Command Read	Data Write	Data Read
Short	MOV reg, reg TCO reg (except CT) SPS SPD NOP		Comparand register (Not last segment) Mask register (not last segment)	
Medium	MOV reg, mem TCO CT(reset) VBC	Status register or 16-bit register		Command register Mask register
Long	MOV mem, reg TCO CT (non reset) CMP SFF		Memory array Comparand register (Last segment) Mask register (last segment)	Memory array

Note: The Instruction cycle times are specified in the AC characteristics table. For two cycle command writes (TCO reg or any instruction requiring an immediate address) the first cycle is a short and the second cycle will be the length given

QCAM INSTRUCTION SET

Instruction Format

The I/O operations of the QS761480/QS762470 are controlled primarily by the control bus ($\overline{CE}$, $\overline{CM}$, $\overline{WE}$, and $\overline{EC}$). The secondary control mechanism of the device is via instructions loaded into the Instruction Register which set up persistent and temporary operation states within the device and control internal data moves. The desired instruction is loaded from the DQ15-DQ0 bus into the Instruction Register during a command write cycle ($\overline{CM}$ and $\overline{WE}$ are LOW). The instruction is captured on the falling edge of $\overline{CE}$.

The instruction word is subdivided into fields which define the operation to be performed. The upper four Instruction Register bits, IR15-lR12, are ignored by the QS761480/QS762470 and are zeros. Instruction Register bit IR11 is the address flag which indicates whether or not the instruction has an address field to be loaded on the next cycle. Instruction Register bits IR8-lR0 define the instruction type: select persistent source, select persistent destination, temporary command override, move, validity bit control, compare, and special instructions. Instruction Register bits IR7 and IR6 define the masking condition, IR5-lR3 define the destination for data transfer, and IR2-lR0 define the source of a data transfer or the validity condition to be set when writing to a memory location. The instruction format is shown below. Using these field and bit definitions, the instruction word has the following structure:

0 : 0 : 0 : 0	**f**	**i : i : i**	**m : m**	**d : d : d**	**s : s : s**

where:

f represents the address flag indicating whether or not the instruction requires an appended address field to be loaded on the next cycle

i : i : i represents the instruction type

m : m represents the Mask Register select for data writes and moves

d : d : d represents the destination for data transfers

s : s : s represents the source of data transfers or the validity bit setting for data transfers to memory.

Throughout the following description of the instructions, mnemonics are defined in an assembly language format. All the instructions have a common structure:

INS dst,src[msk],val

INS: instruction mnemonic
dst: destination of the data
src: source of the data
msk: Mask Register used
val: validity condition set at the location written

Instruction Set Description

Instruction: Select Persistent Source (SPS)

Binary Op Code:	**0000 f000 0000 0sss**
f	**address field flag**
sss	**selected source**

Description

This instruction selects a persistent source for data reads. The selected source remains the source for data reads until another SPS instruction or a reset occurs. The default persistent source after power-up or reset is the Status Register in command mode ($\overline{CM}$ is LOW) and is the Comparand Register for a data read cycle ($\overline{CM}$ is HIGH). If f=1, the Address Register is updated to the aaaH value in the second cycle of the instruction. If the SPS is M@[AR], after the number of data reads specified in the Segment Control Register, the Address Register is incremented or decremented according to the setting of bits CT2 and CT3 in the Control Register.

Condition	Operation	Mnemonic	Op Code
f			
0	if source is memory at address, or is at address reg		
1	if source is not memory at address		
sss			
000	Comparand Register	SPS CR	0000H
001	Mask Register 1	SPS MR1	0001H
010	Mask Register2	SPS MR2	0002H
011	reserved		
100	memory array at Address Register	SPS M@[AR]	0004H
100	(f=1)memory array at address	SPS M@aaaH	0804H
101	memory at highest-priority match	SPS M@HM	0005H

Instruction: Select Persistent Destination (SPD)

Binary Op Code:	**0000 f001 mmdd dvvv**
f	**address flag**
mm	**Mask Register select**
ddd	**selected destination**
vvv	**validity setting (if destination is a memory location)**

Description

This instruction selects a persistent destination for data writes. The selected destination remains the destination for data writes until another SPD instruction or a reset occurs. The Comparand Register is the default destination for data writes after power-up or reset.

When the destination is the Comparand Register or the memory array, the writing of data may be masked by either Mask Register 1 or Mask Register 2. During a masked data write, those bits in the destination that correspond to bits containing zeros in the selected Mask Register will be modified, while bits in the destination corresponding to bits containing ones in the selected Mask Register will not.

Writing to the Comparand Register or a Mask Register causes a comparison to occur when the last segment is written, while writing to the memory array does not. The next free address is generated when executing instructions that could potentially affect the validity bits. If f=1, the Address Register is updated to the aaaH value in the second cycle of the instruction. If the SPD is M@[AR], after the number of data writes specified in the Segment Control Register, the Address Register is incremented or decremented according to the setting of bit CT2 and CT3 in the Control Register.

Condition	Operation	Mnemonic	Op Code
f			
0	if destination is memory at address , or is at address reg		
1	if destination is not memory at address		
mm			
00	no mask		
01	mask write with Mask Register 1		
10	mask write with Mask Register 2		
11	reserved		
vvv			
100	set valid		
101	set empty		
110	set skip		
111	set random access location		

Instruction: Select Persistent Destination (SPD) (continued)

Condition	Operation	Mnemonic	Op Code
ddd			
000	Comparand Register	SPD CR	0100H
	masked by MR1	SPD CR[MR1]	0140H
	masked by MR2	SPD CR[MR2]	0180H
001	Mask Register 1	SPD MR1	0108H
010	Mask Register 2	SPD MR2	0110H
011	reserved		
100	memory at address reg set valid	SPD M@[AR],V	0124H
	masked by MR2	SPD M@[AR][MR2],V	01A4H
100	memory at address reg set empty	SPD M@[AR],E	0125H
	masked by MR1	SPD M@[AR][MR1],E	0165H
	masked by MR2	SPD M@[AR][MR2],E	01A5H
100	memory at address reg set skip	SPD M@[AR],S	0126H
	masked by MR1	SPD M@[AR][MR1],S	0166H
	masked by MR2	SPD M@[AR][MR2],S	01A6H
100	memory at address reg set random	SPD M@[AR],R	0127H
	masked by MR1	SPD M@[AR][MR1],R	0167H
	masked by MR2	SPD M@[AR][MR2],R	01A7H
100	(f=1) memory at address set valid	SPD M@aaaH,V	0924H
	masked by MR1	SPD M@aaaH[MR1],V	0964H
	masked by MR2	SPD M@aaaH[MR2],V	09A4H
100	(f=1) memory at address set empty	SPD M@aaaH,E	0925H
	masked by MR1	SPD M@aaaH[MR1],E	0965H
	masked by MR2	SPD M@aaaH[MR2],E	09A5H
100	(f=1) memory at address set skip	SPD M@aaaH,S	0926H
	masked by MR1	SPD M@aaaH[MR1],S	0966H
	masked by MR2	SPD M@aaaH[MR2],S	09A6H
100	(f=1) memory at address set random access	SPD M@aaaH,R	0927H
	masked by MR1	SPD M@aaaH[MR1],R	0967H
	masked by MR2	SPD M@aaaH[MR2],R	09A7H
101	memory at highest-priority match,valid	SPD M@HM,V	012CH
	masked by MR1	SPD M@HM[MR1],V	016CH
	masked by MR2	SPD M@HM[MR2],V	01ACH
101	memory at highest-priority match, empty	SPD M@HM,E	012DH
	masked by MR1	SPD M@HM[MR1],E	016DH
	masked by MR2	SPD M@HM[MR2],E	01ADH
101	memory at highest-priority match, skip	SPD M@HM,S	012EH
	masked by MR1	SPD M@HM[MR1],S	016EH
	masked by MR2	SPD M@HM[MR2],S	01AEH
101	memory at high-priority match, random	SPD M@HM,R	012FH
	masked by MR1	SPD M@HM[MR1],R	016FH
	masked by MR2	SPD M@HM[MR2],R	01AFH
110	memory at next vree address, valid	SPD M@NF,V	0134H
	masked by MR1	SPD M@NF[MR1],V	0174H
	masked by MR2	SPD M@NF[MR2],V	01B4H
110	memory at next free address, empty	SPD M@NF,E	0135H
	masked by MR1	SPD M@NF[MR1],E	0175H
	masked by MR2	SPD M@NF[MR2],E	01B5H
110	memory at next free address, skip	SPD M@NF,S	0136H
	masked by MR1	SPD M@NF[MR1],S	0176H
	masked by MR2	SPD M@NF[MR2],S	01B6H
110	memory at next free address, random	SPD M@NF,R	0137H
	masked by MR1	SPD M@NF[MR1],R	0177H
	masked by MR2	SPD M@NF[MR2],R	01B7H
111	reserved		

Instruction: Temporary Command Override (TCO)

Binary Op Code:	**0000 0010 00dd d000**
ddd	**Register selected as source or destination for only the next command read or write cycle.**

Description

The TCO instruction temporarily selects a Register to become the source or destination for only the next command read or write cycle. After either of those cycles, subsequent command read or write cycles revert to reading the Status Register and writing the Instruction Register.

The TCO PS and TCO PD instructions are two-cycle instructions that allow the user to read which persistent source or destination has been selected. If the next instruction is a command read cycle, the "sss" value of the last SPS instruction will be output in bits 2-0, or the "mmdddvvv" value of the last SPD instruction will be output in bits 7-0. If either TCO PS or TCO PD are followed by a command write cycle, no action occurs. The TCO AR instruction permits access to the Address Register for diagnostic purposes. The Next-Free-Address Register is read only. Writes to the Page Address Register invalidate the contents of the Status Register.

Condition	Operation	Mnemonic	Op Code
ddd			
000	Control Register	TCO CT	0200H
001	Page Address Register	TCO PA	0208H
010	Segment Control Register	TCO SC	0210H
011	read next free address	TCO NF	0218H
100	Address Register	TCO AR	0220H
101	Device Select Register	TCO DS	0228H
110	read persistent source	TCO PS	0230H
111	read persistent destination	TCO PD	0238H

Instruction: Data Move (MOV)

Binary Op Code:	**0000 f011 mmdd dsss or 0000 f011 mmdd dvss**
f	**address Field Flag**
mm	**Mask Register select**
ddd	**destination of data**
sss	**source of data**
v	**validity setting if destination is a memory location**

Description

The MOV instruction transfers the data in the selected source to the selected destination. Data transfers between the memory array and the Comparand Register may be masked by either Mask Register 1 or Mask Register 2. If the transfer is masked, only those bits in the destination that correspond to bits containing zeros in the selected Mask Register will be altered, while destination bits which correspond to bits containing ones in the selected Mask Register will not.

The validity bits of a memory location used as a destination for a MOV instruction will be set to the valid state or left unchanged, depending on the nature of the operation. If the source and destination are selected to be the same register in register-to-register operations, no net change to the state of the QCAM occurs (a NOP).

If f=1, the Address Register is updated to the aaaH value in the second cycle of the instruction. After a MOV [AR] instruction, the Address Register is incremented or decremented according to the setting of bits CT2 and CT3 in the Control Register.

f	
0	if source or destination is not memory at address, or is at Address Register
1	if source or destination is memory at address
mm	
00	no mask
01	mask write with Mask Register 1
10	mask write with Mask Register 2
11	reserved
v	
0	no change to validity condition
1	set valid: skip=0, empty=0

Condition			Operation	Mnemonic	Op Code
ddd	**sss**				
000			Comparand Register from:		
	000		no operation	NOP	0300H
	001		Mask Register 1	MOV CR,MR1	0301H
	010		Mask Register 2	MOV CR,MR2	0302H
	011		reserved		
	100		memory at Address Register	MOV CR,[AR]	0304H
			masked by MR1	MOV CR,[AR][MR1]	0344H
			masked by MR2	MOV CR,[AR][MR2]	0384H
		(f=1)	memory at address	MOV CR,aaaH	0B04H
			masked by MR1	MOV CR,aaaH[MR1]	0B44H
			masked by MR2	MOV CR,aaaH[MR2]	0B84H
	101		memory at highest-priority match	MOV CR,HM	0305H
			masked by MR1	MOV CR,HM[MR1]	0345H
			masked by MR2	MOV CR,HM[MR2]	0385H
	110		reserved		
	111		reserved		
001			Mask Register 1 from:		
	000		Comparand Register	MOV MR1,CR	0308H
	001		no operation	NOP	0309H
	010		Mask Register 2	MOV MR1,MR2	030AH
	011		reserved		
	100		memory at Address Register	MOV MR1,[AR]	030CH
	100	(f=1)	memory at address	MOV MR1,aaaH	0B0CH
	101		memory at highest-priority match	MOV MR1,HM	030DH
	110		reserved		
	111		reserved		
010			Mask Register 2 from:		
	000		Comparand Register	MOV MR2,CR	0310H
	001		Mask Register 1	MOV MR2,MR1	0311H
	010		no operation	NOP	0312H
	011		reserved		
	100		memory at Address Register	MOV MR2,[AR]	0314H
	100	(f=1)	memory at address	MOV MR2,aaaH	0B14H
	101		memory at highest-priority match	MOV MR2,HM	0315H
	110		reserved		
	111		reserved		
	011		reserved		
100			memory at Address Register, no change to validity bits, from:		
	000		Comparand Register	MOV [AR],CR	0320H
			masked by MR1	MOV [AR],CR[MR1]	0360H
			masked by MR2	MOV [AR],CR[MR2]	03A0H
	001		Mask Register 1	MOV [AR],MR1	0321H
	010		Mask Register 2	MOV [AR],MR2	0322H
	011		reserved		
100			memory at Address Register, location set valid, from:		
	100		Comparand Register	MOV [AR],CR,V	0324H
			masked by MR1	MOV [AR],CR[MR1],V	0364H
			masked by MR2	MOV [AR],CR[MR2],V	03A4H
	101		Mask Register 1	MOV [AR],MR1,V	0325H
	110		Mask Register 2	MOV [AR],MR2,V	0326H
	111		reserved		
100	(f=1)		memory at address, no change to validity bits, from:		
	000		Comparand Register	MOV aaaH,CR	0B20H
			masked by MR1	MOV aaaH,CR[MR1]	0B60H
			masked by MR2	MOVaaaH,CR[MR2]	0BA0H

Condition		Operation	Mnemonic	Op Code
ddd	**sss**			
	001	Mask Register 1	MOV aaaH,MR1	0B21H
	010	Mask Register 2	MOV aaaH,MR2	0B22H
	011	reserved		
100		(f=1)memory at address, location set valid, from:		
	100	Comparand Register	MOV aaaH,CR,V	0B24H
		masked by MR1	MOV aaaH,CR[MR1],V	0B64H
		masked by MR2	MOV aaaH,CR[MR2],V	0BA4H
	101	Mask Register 1	MOV aaaH,MR1,V	0B25H
	110	Mask Register 2	MOV aaaH,MR2,V	0B26H
	111	reserved		
101		memory at highest-priority match, no change to validity bits, from:		
	000	Comparand Register	MOV HM,CR	0328H
		masked by MR1	MOV HM,CR[MR1]	0368H
		masked by MR2	MOV HM,CR[MR2]	03A8H
	001	Mask Register 1	MOV HM,MR1	0329H
	010	Mask Register 2	MOV HM,MR2	032AH
	011	reserved		
101		memory at highest-priority match, location set valid, from:		
	100	Comparand Register	MOV HM,CR,V	032CH
		masked by MR1	MOV HM,CR[MR1],V	036CH
		masked by MR2	MOV HM,CR[MR2],V	03ACH
	101	Mask Register 1	MOV HM,MR1,V	032DH
	110	Mask Register 2	MOV HM,MR2,V	032EH
	111	reserved		
110		memory at next free address, no change to validity bits, from:		
	000	Comparand Register	MOV NF,CR	0330H
		masked by MR1	MOV NF,CR[MR1]	0370H
		masked by MR2	MOV NF,CR[MR2]	03B0H
	001	Mask Register 1	MOV NF,MR1	0331H
	010	Mask Register 2	MOV NF,MR2	0332H
	011	reserved		
110		memory at next free address, location set valid, from:		
	100	Comparand Register	MOV NF,CR,V	0334H
		masked by MR1	MOV NF,CR[MR1],V	0374H
		masked by MR2	MOV NF,CR[MR2],V	03B4H
	101	Mask Register 1	MOV NF,MR1,V	0335H
	110	Mask Register 2	MOV NF,MR2,V	0336H
	111	reserved		
111		reserved		

Instruction: Validity Bit Control (VBC)

Binary Op Code:	**0000 f100 00dd dvvv**
f	**address field flag**
ddd	**destinationof data**
vvv	**validity setting for memory location**

Description

The VBC instruction sets the validity bits to the selected state at the selected memory location. Validity bits can be accessed randomly or associatively. VBC can be used in conjunction with the appropriate compare instruction to compare on any validity condition. Hence, skipped locations can be returned to the valid state after processing multiple matches by repeating the compare operation using the skip condition as the validity field-search criterion. If f=1, the address register is updated to the aaaH value in the second cycle of the instruction. After a VBC [AR] instruction, the address register is incremented or decremented according to the settings of the CT2 and CT3 bits in the Control Register.

Condition	Operation	Mnemonic	Op Code
f			
0	if source or destination is not memory at address, or is at address register		
1	if source or destination is memory at address		
ddd	**vvv**		
000	reserved		
001	reserved		
010	reserved		
011	reserved		
	000 reserved for all **ddd**		
	001 reserved for all **ddd**		
	010 reserved for all **ddd**		
	011 reserved for all **ddd**		
100	set validity bits at address register		
	100 set valid	VBC [AR],V	0424H
	101 set empty	VBC [AR],E	0425H
	110 set skip	VBC [AR],S	0426H
	111 set random access	VBC [AR],R	0427H
100	(f=1) set validity bits at address		
	100 set valid	VBC aaaH,V	0C24H
	101 set empty	VBC aaaH,E	0C25H
	110 set skip	VBC aaaH,S	0C26H
	111 set random access	VBC aaaH,R	0C27H
101	set validity bits at highest-priority match		
	100 set valid	VBC HM,V	042CH
	101 set empty	VBC HM,E	042DH
	110 set skip	VBC HM,S	042EH
	111 set random access	VBC HM,R	042FH

Instruction: Validity Bit Control (VBC) (continued)

Condition	Operation	Mnemonic	Op Code
110	reserved		
111	set validity bits at all matching locations		
100	set valid	VBC ALM,V	043CH
101	set empty	VBC ALM,E	043DH
110	set skip	VBC ALM,S	043EH
111	set random access	VBC ALM,R	043FH

Instruction: Compare (CMP)

Binary Op Code	**0000 01010000 0vvv**
vvv	**validity condition**

Description

A CMP V, S, or R instruction forces a comparison of valid, skipped, or random entries against the value in the Comparand Register through a Mask Register, if one is selected in the Control Register. During a CMP E instruction, the comparison is done only on the validity bits, and all 64 data bits are automatically masked.

Condition	Operation	Mnemonic	Op Code
vvv			
000	reserved		
001	reserved		
010	reserved		
011	reserved		
100	compare valid locations	CMP V	0504H
101	compare empty locations	CMP E	0505H
110	compare skipped locations	CMP S	0506H
111	compare random access locations	CMP R	0507H

Instruction: set Full Flag (SFF)

Binary Op Code:	**0000 01110000 0000**

Description

The SFF instruction is a special instruction used to force the full flag LOW for a device whose $\overline{FI}$ input is LOW, but whose FF output is HIGH. SFF is used in depth-expanded systems for selecting each device in turn to initialize its Page Address Register.

Condition	Operation	Mnemonic	Op Code
	set full flag	SFF	0700H

Instruction: No Operation (NOP)

Binary Op Code:	**0000 00110000 0000**

Description

The NOP (no-op) belongs to the MOV instructions, where a register is moved to itself. No change occurs within the device. This instruction is useful in unlocking the daisy-chain.

Condition	Operation	Mnemonic	Op Code
	no operation	NOP	0300H

Table 19. Absolute Maximum Ratings(1)

Supply Voltage to Ground	–0.5 to 7.0V
DC Output Voltage V_{OUT}	–0.5 to Vcc + 0.5V(2)
DC Output Current	20mA(3)
T_{BIAS} Temperature Under Bias	–40°C to 85°C
T_{STG} StorageTemperature	–55°C to 25°C

Notes:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device, resulting in functional- or reliability-type failures.
2. –2.0V for 10ns, measured at the 50% point.
3. Per output, one at a time, one second duration.

Table 20. DC Electrical Characteristics Over Operating Range

(Commercial: T_A = 0°C to 70°C, V_{CC} = 5.0V ±5%)

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IH}	Input HIGH Voltage	Logic HIGH for all Inputs	2.2	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage	Logic LOW for all Inputs(1), (2)	–0.5	0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = –2mA, V_{CC} = Min.	2.4	–	V
V_{OL}	Output LOW Voltage	I_{OL} = 4mA, V_{CC} = Min.	–	0.4	V
$\| I_{IL} \|$	Input Leakage	V_{CC} = 5.25V; GND ≤ V_{IN} ≤ V_{CC}(3)	–2	2	µA
$\| I_{OL} \|$	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC}	–10	10	µA

Notes:
1. –1V for a duration of 10ns measured at 50% amplitude points for input-only lines (Fig. 9).
2. Common I/O lines are clamped so that signal transients cannot fall below –0.5V.
3. The $\overline{\text{RESET}}$ pin has an internal pull-up resistor of 5kΩ-25kΩ

Table 21A. Power Supply Characteristics, QS761480

Symbol	Parameter	Test Conditions	–55 Max	–70 Max	–90 Max	Units
I_{CC}	Operating Current	t_{CYC} = t_{CYC} (Min.)(1)	330	260	210	mA
I_{SB}	Standby Current	$\overline{CE}$ = HIGH	10	10	10	mA

Table 21B. Power Supply Characteristics, QS762470

Symbol	Parameter	Test Conditions	–55 Max	–70 Max	–90 Max	Units
I_{CC}	Operating Current	t_{CYC} = t_{CYC} (Min)(1)	330	260	210	mA
I_{SB}	Standby Current	$\overline{CE}$ = HIGH	10	10	10	mA

Notes for Tables 21A and 21B:
1. With Output and I/O pins unloaded.

Table 22. Capacitance
(T_A = 25°C, f = 1.0MHz)

Name	Description	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V, F = 1MHz	—	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, F = 1MHz	—	8	pF

Note: Capacitance is guaranteed but not tested.

Table 23. AC Test Conditions

Input Pulse Levels	0V to 3.0V
Input Rise/Fall Times	< 3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V

Figure 7. Test Load A

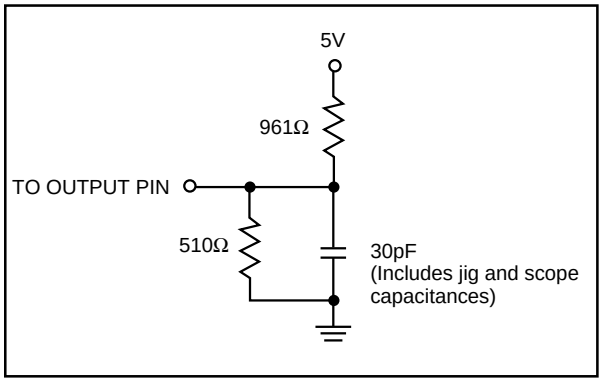


Figure 8. Test Load B

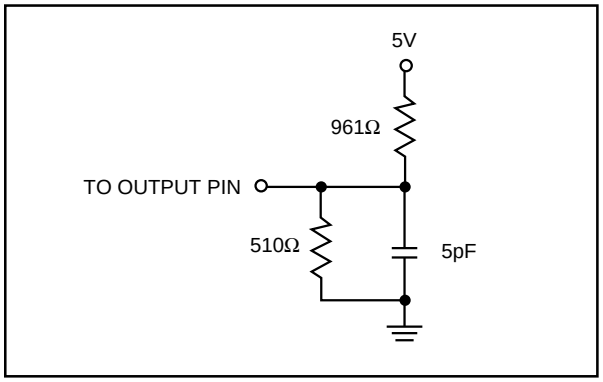


Figure 9. Input signal waveform

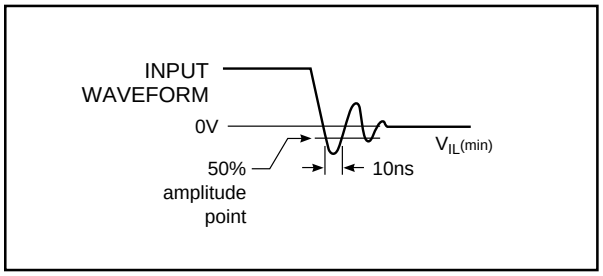


Table 24. AC Switching Characteristics(1)

No	Symbol	Description	–55		–70		–90		Unit	Notes
			Min	Max	Min	Max	Min	Max		
1	t_{CYC}	Chip Enable Compare Cycle Time	55		70		90		ns	
2	t_{CEL}	Chip Enable LOW Pulse Width								
		Short Cycle	15		15		25		ns	
		Medium Cycle	30		35		50		ns	2
		Long Cycle	42.5		55		75		ns	
3	t_{CEH}	Chip Enable HIGH Pulse Width	12.5		15		15		ns	
4	t_{SCE}	Control Input to Chip Enable LOW Setup Time	0		0		0		ns	3
5	t_{HCE}	Control Input to Chip Enable LOW Hold Time	10		10		10		ns	3
6	t_{CEO}	Chip Enable LOW to Output Active	3		3		3		ns	4
7	t_{CED}	Chip Enable LOW to Data Valid (Medium Cycle)		27.5		30		50	ns	2,4
	t_{CED}	Chip Enable LOW to Data Valid (Long Cycle)		42.5		52		75	ns	2, 4
8	t_{CEZ}	Chip Enable HIGH to Outputs High-Z	3	15	3	17	3	20	ns	5
9	t_{SDE}	Data to Chip Enable LOW Setup Time	0		0		0		ns	
10	t_{HDE}	Data to Chip Enable LOW Hold Time	10		10		15		ns	
11	t_{SFI}	Full In Valid to Chip Enable LOW Setup Time	0		0		0		ns	
12	t_{FIF}	Full In Valid to Full Flag Valid		5		7		8	ns	
13	t_{ELF}	Chip Enable LOW to Full Flag Valid		40		50		75	ns	
14	t_{SMC}	Match In Valid to Chip Enable Low Set-Up Time	0		0		0		ns	
15	t_{EMI}	Chip Enable HIGH to $\overline{MF}$, $\overline{MA}$, $\overline{MM}$ Invalid	0		0		0		ns	
16	t_{MIM}	Match In Valid to $\overline{MF}$ Valid		5		7		8	ns	
17	t_{EMFV}	Chip Enable HIGH to $\overline{MF}$ Valid		16		16		25	ns	
18	t_{EMXV}	Chip Enable HIGH to $\overline{MA}$, $\overline{MM}$ Valid		18		18		25	ns	
19	t_{RLP}	Reset LOW Pulse Width	20		20		20		ns	6
20	t_{CEHR}	$\overline{CE}$ HIGH to $\overline{RESET}$ LOW Setup Time	0		0		0		ns	
21	t_{RCEL}	$\overline{RESET}$ HIGH to $\overline{CE}$ LOW Setup Time	0		0		0		ns	

Notes:
1. Over the operating temperature and voltage ranges.
2. See Table 18A.
3. Control signals are $\overline{WE}$, $\overline{CM}$, and $\overline{EC}$.
4. With load specified in Figure 7.
5. With load specified in Figure 8.
6. $\overline{CE}$ must be HIGH during this period to ensure accurate default values in the configuration registers.

Figure 10. Reset Timing

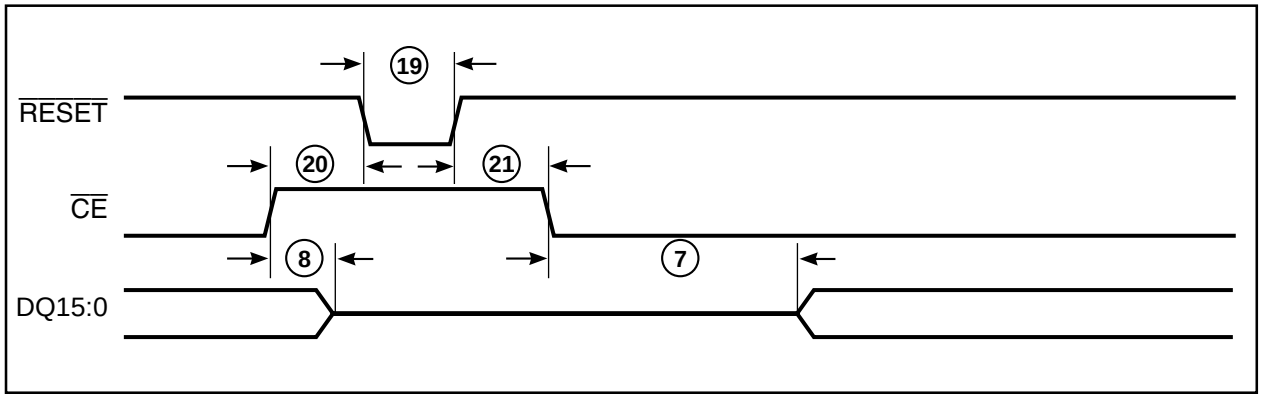


Figure 11. Read Cycle Timing

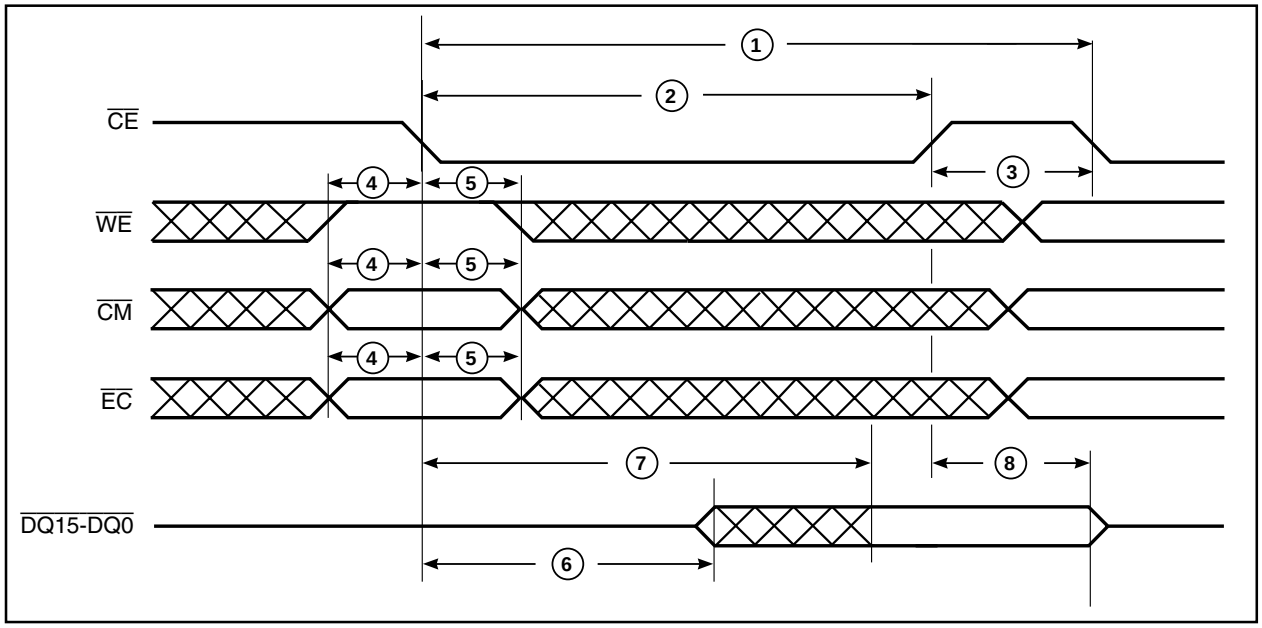


Figure 12. Write Cycle Timing

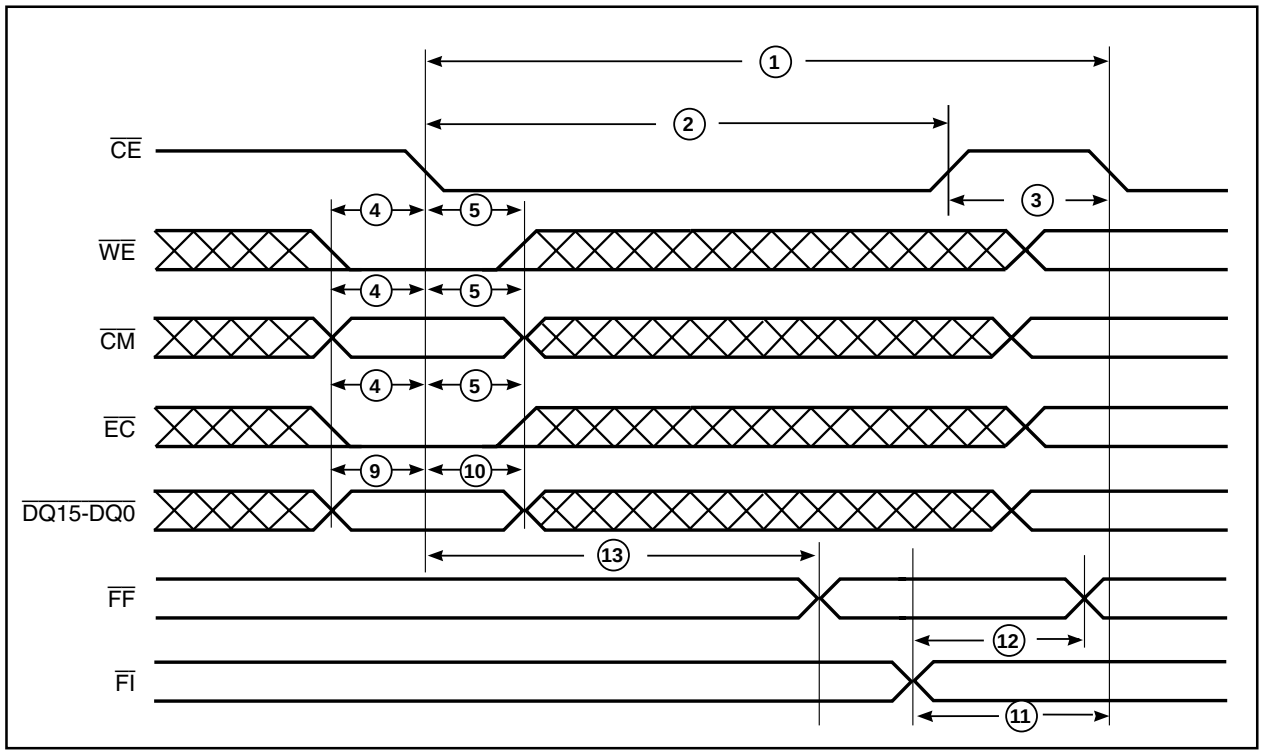


Figure 13. Match-Cycle Timing: Stand-Alone Mode

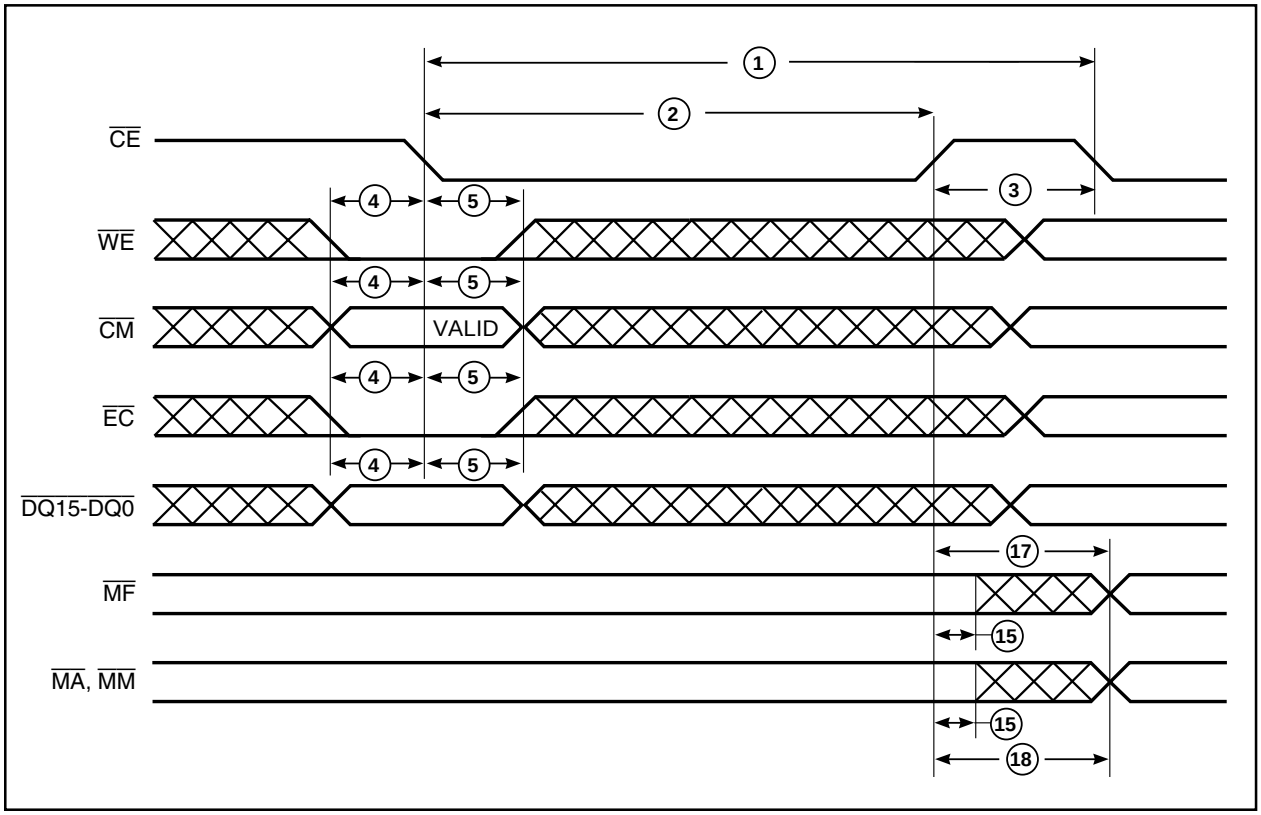
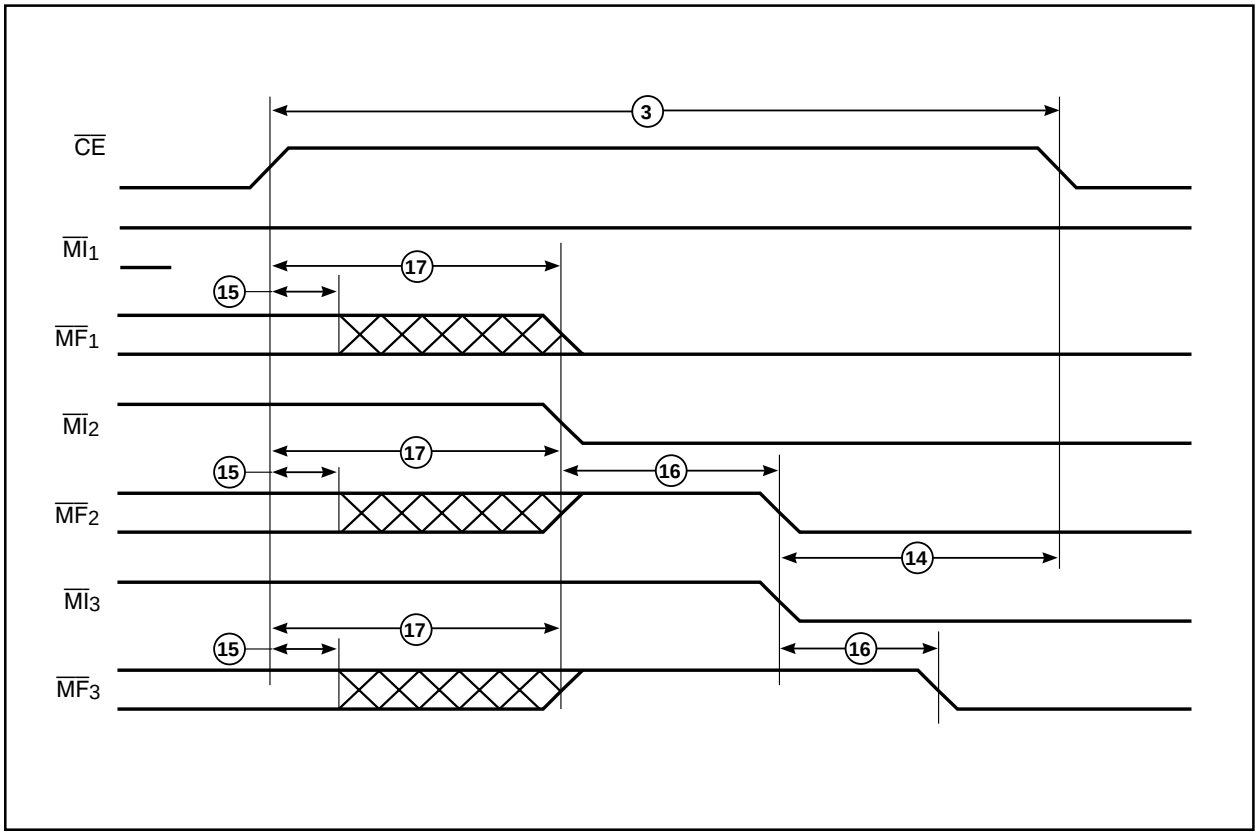
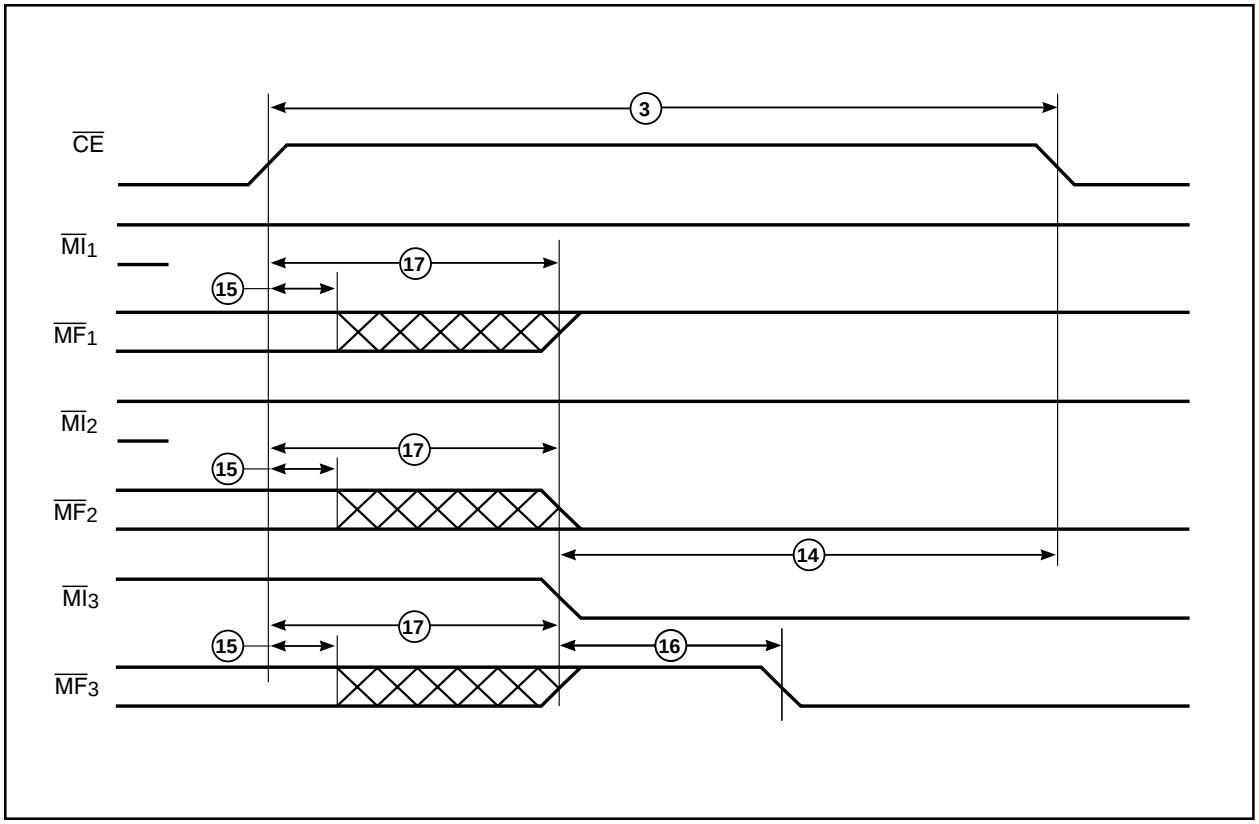


Figure 14. Match Cycle Timing: 3 Daisy-Chained QCAMS, Match in QCAM 1 Only



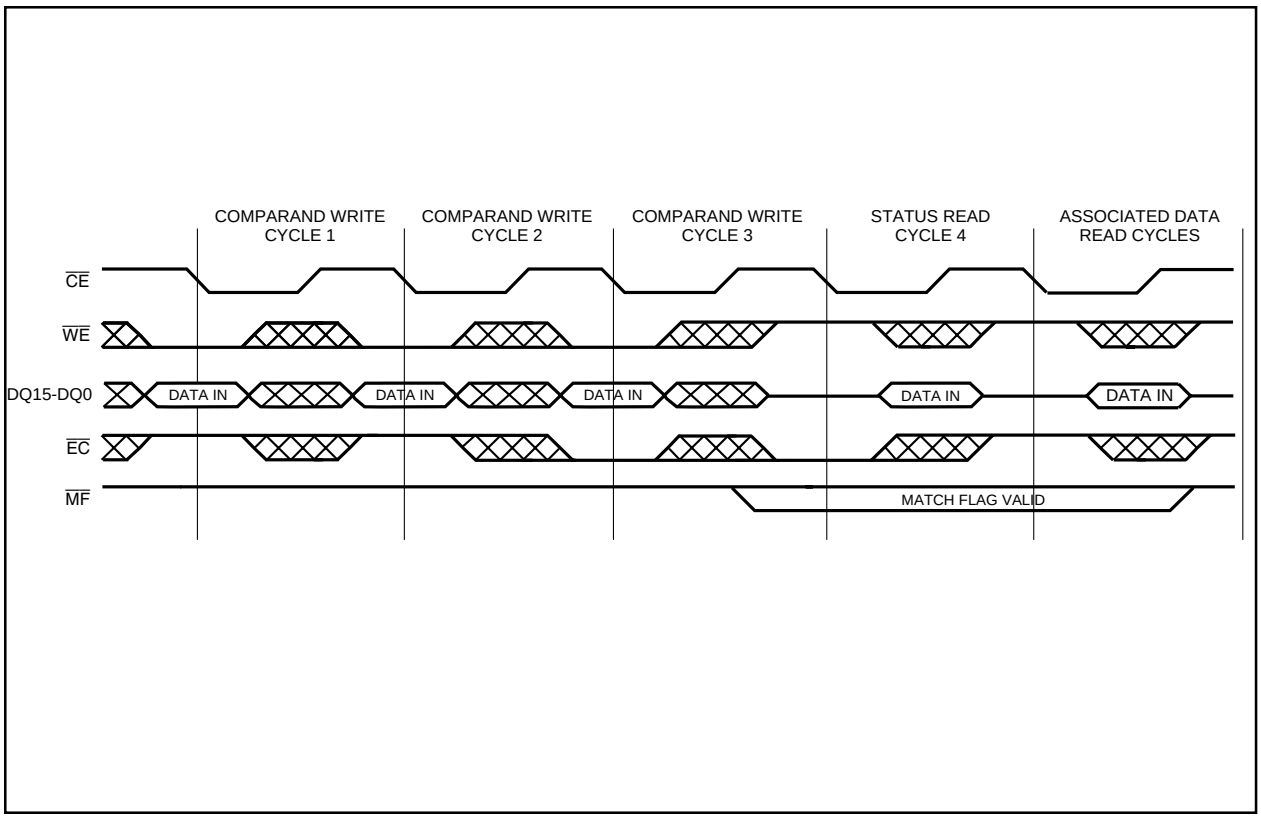
Note: Assume EC is held LOW during the previous falling edge of CE.

Figure 15. Match Cycle Timing: 3 Daisy-Chained QCAMS, Match in QCAM 2 Only



Note: Assume $\overline{EC}$ is held LOW during the previous falling edge of $\overline{CE}$.

Figure 16. Cycle-to-Cycle Timing



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