HM-6617

March 1997

2K x 8 CMOS PROM

Features

- **Low Power Standby and Operating Power**
  - **ICCSB 100μA**
  - **ICCOP . . . . . .20mA at 1MHz**
- **Fast Access Time. 90/120ns**
- **Industry Standard Pinout**
- **Single 5.0V Supply**
- **CMOS/TTL Compatible Inputs**
- **High Output Drive . . . . . 12 LSTTL Loads**
- **Synchronous Operation**
- **On-Chip Address Latches**
- **Separate Output Enable**

Ordering Information

PACKAGE	TEMP. RANGE	90ns	120ns	PKG. NO.
SBDIP	-40°C to +85°C	HM1-6617B-9	HM1-6617-9	D24.6
SMD#	-55°C to +125°C	5962-8954002JA	5962-8954001JA	D24.6
SLIM SBDIP	-40°C to +85°C	HM6-6617B-9	HM6-6617-9	D24.3
SMD#	-55°C to +125°C	5962-8954002LA	5962-8954001LA	D24.3
CLCC	-40°C to +85°C	HM4-6617B-9	HM4-6617-9	J32.A
SMD#	-55°C to +125°C	5962-8954002XA	5962-8954001XA	J32.A

Description

The HM-6617 is a 16,384 bit fuse link CMOS PROM in a 2K word by 8-bit/word format with “Three-State” outputs. This PROM is available in the standard 0.600 inch wide 24 pin SBDIP, the 0.300 inch wide slimline SBDIP, and the JEDEC standard 32 pad CLCC.

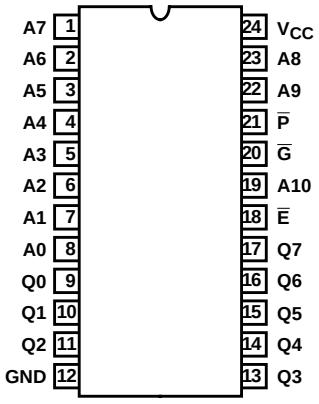
The HM-6617 utilizes a synchronous design technique. This includes on-chip address latches and a separate output enable control which makes this device ideal for applications utilizing recent generation microprocessors. This design technique, combined with the Intersil advanced self-aligned silicon gate CMOS process technology offers ultra-low standby current. Low ICCSB is ideal for battery applications or other systems with low power requirements.

The Intersil NiCr fuse link technology is utilized on this and other Intersil CMOS PROMs. This gives the user a PROM with permanent, stable storage characteristics over the full industrial and military temperature voltage ranges. NiCr fuse technology combined with the low power characteristics of CMOS provides an excellent alternative to standard bipolar PROMs or NMOS EPROMs.

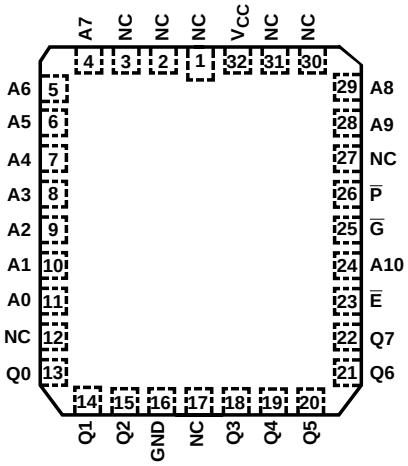
All bits are manufactured storing a logical “0” and can be selectively programmed for a logical “1” at any bit location.

Pinouts

HM-6617 (SBDIP)
TOP VIEW



HM-6617 (CLCC)
TOP VIEW



PIN DESCRIPTION

PIN	DESCRIPTION
NC	No Connect
A0-A10	Address Inputs
$\overline{E}$	Chip Enable
Q	Data Output
V_{CC}	Power (+5V)
$\overline{G}$	Output Enable
$\overline{P}$ (Note)	Output Enable

NOTE: $\overline{P}$ should be hardwired to V_{CC} except during programming.

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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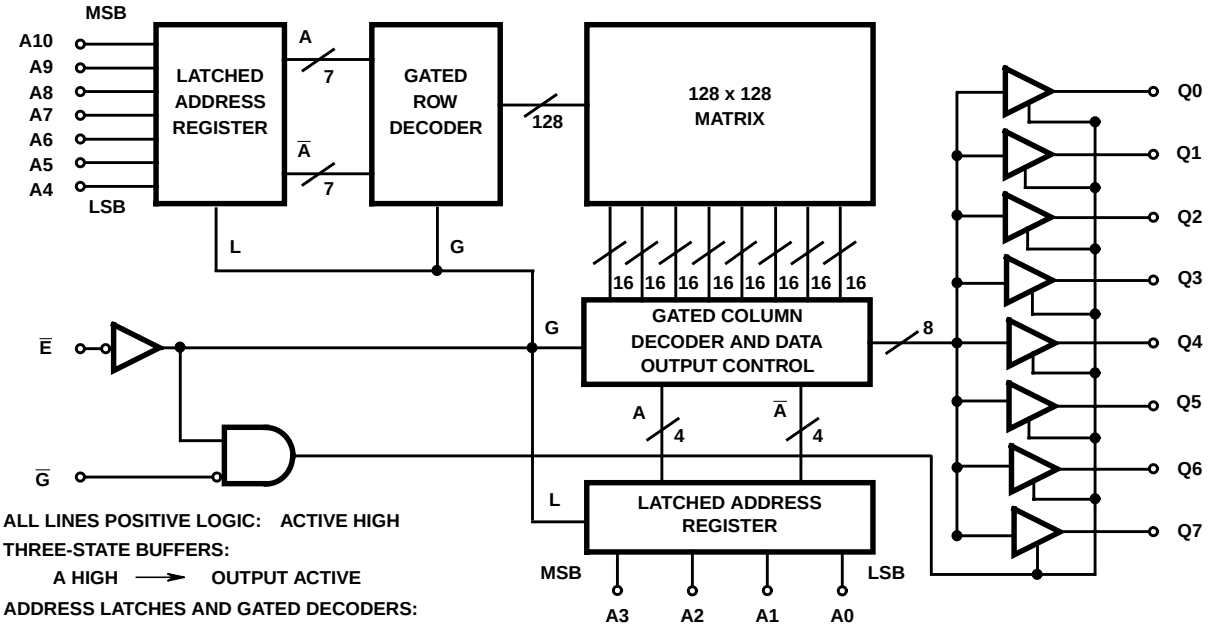
File Number **3017.1**

Functional Diagram



ALL LINES POSITIVE LOGIC: ACTIVE HIGH

THREE-STATE BUFFERS:

A HIGH → OUTPUT ACTIVE

ADDRESS LATCHES AND GATED DECODERS:

LATCH ON FALLING EDGE OF $\overline{E}$

GATE ON FALLING EDGE OF $\overline{G}$

Background Information Programming Algorithm

The HM-6617 CMOS PROM is manufactured with all bits containing a logical zero (output low). Any bit can be programmed selectively to a logical one (output high) state by following the procedure shown below. To accomplish this, a programmer can be built that meets the specifications shown, or any of the approved commercial programmers can be used.

Programming Sequence Of Events

1. Apply a voltage of V_{CC1} to V_{CC} of the PROM.
2. Read all fuse locations to verify that the PROM is blank (output low).
3. Place the PROM in the initial state for programming: $\overline{E}$ = V_{IH}, $\overline{P}$ = V_{IH}, $\overline{G}$ = V_{IL}.
4. Apply the correct binary address for the word to be programmed. No inputs should be left open circuit.
5. After a delay of tD, apply voltage of V_{IL} to $\overline{E}$ (pin 18) to access the addressed word.
6. The address may be held through the cycle, but must be held valid at least for a time equal to tD after the falling edge of $\overline{E}$. None of the inputs should be allowed to float to an invalid logic level.
7. After a delay of tD, disable the outputs by applying a voltage of V_{IH} to $\overline{G}$ (pin 20).
8. After a delay of tD, apply voltage of V_{IL} to $\overline{P}$ (pin 21).
9. After delay of tD, raise V_{CC} (pin 24) to VCCPROG with a rise time of tR. All outputs at V_{IH} should track V_{CC} with V_{CC} -2.0V to V_{CC} +0.3V. This could be accomplished by pulling outputs at V_{IH} to V_{CC} through pull-up resistors of value Rn.
10. After a delay of tD, pull the output which corresponds to the bit to be programmed to V_{IL}. Only one bit should be programmed at a time.
11. After a delay of tPW, allow the output to be pulled to V_{IH} through pull-up resistor Rn.
12. After a delay of tD, reduce V_{CC} (pin 24) to V_{CC1} with a fall time of tF. All outputs at V_{IH} should track V_{CC} with V_{CC} 2.0V to V_{CC} +0.3V. This could be accomplished by pulling outputs at V_{IH} to V_{CC} through pull-up resistors of value Rn.
13. Apply a voltage of V_{IH} to $\overline{P}$ (pin 21).
14. After a delay of tD, apply a voltage of V_{IL} to $\overline{G}$ (pin 20).
15. After a delay of tD, examine the outputs for correct data. If any location verifies incorrectly, repeat steps 4 through 14 (attempting to program only those bits in the word which verified incorrectly) up to a maximum of eight attempts for a given word. If a word does not program within eight attempts, it should be considered a programming reject.
16. Repeat steps 3 through 15 for all other bits to be programmed in the PROM.

Post-Programming Verification

17. Place the PROM in the post-programming verification mode: $\overline{E}$ = V_{IH}, $\overline{G}$ = V_{IL}, $\overline{P}$ = V_{IH}, V_{CC} (pin 24) = V_{CC1}.
18. Apply the correct binary address of the word to be verified to the PROM.
19. After a delay of tD, apply a voltage of V_{IL} to $\overline{E}$ (pin 18).
20. After a delay of tD, examine the outputs for correct data. If any location fails to verify correctly, the PROM should be considered a programming reject.
21. Repeat steps 17 through 20 for all possible programming locations

Post-Programming Read

22. Apply a voltage of V_{CC2} = 4.0V to V_{CC} (pin 24).
23. After a delay of tD, apply a voltage of V_{IH} to $\overline{E}$ (pin 18).
24. Apply the correct binary address of the word to be read.
25. After a delay of TAVEL, apply a voltage of V_{IL} to $\overline{E}$ (pin 18).
26. After a delay of TELQV, examine the outputs for correct data. If any location fails to verify correctly, the PROM should be considered a programming reject.
27. Repeat steps 23 through 26 for all address locations.
28. Apply a voltage of V_{CC2} = 6.0V to V_{CC} (pin 24).
29. Repeat steps 23 through 26 for all address locations.

Programming Cycle

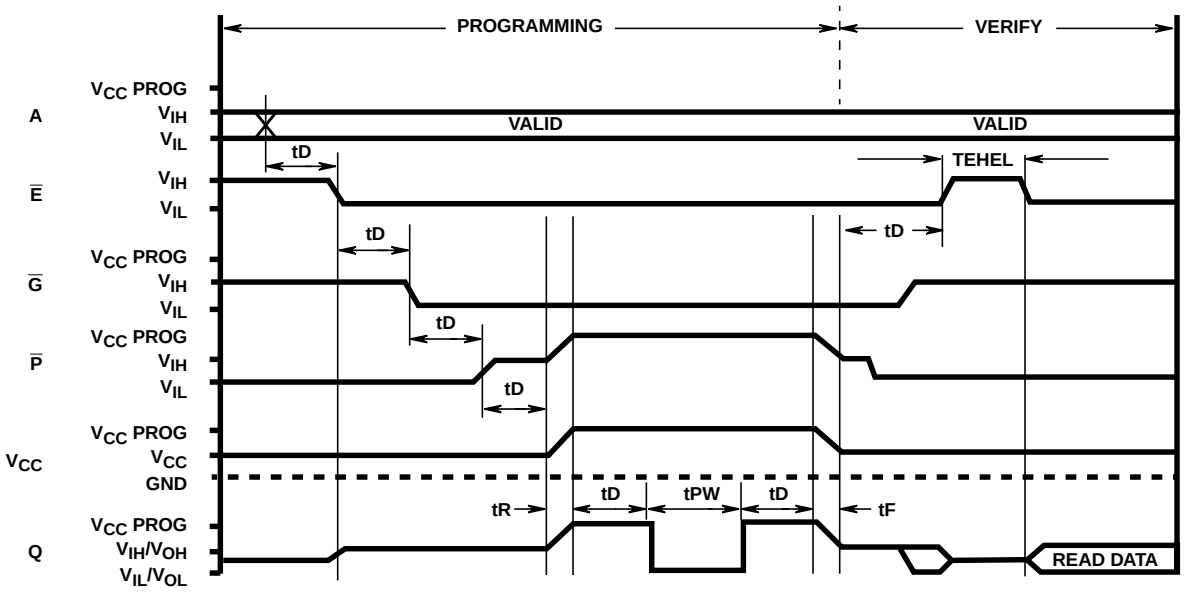


FIGURE 1. HM-6617 PROGRAMMING CYCLE

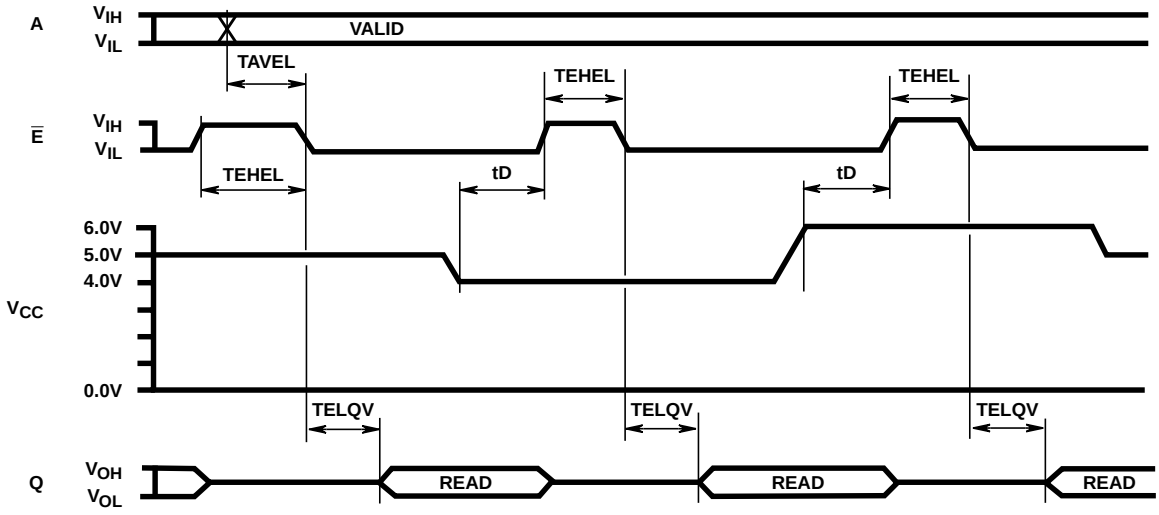


FIGURE 2. HM-6617 POST PROGRAMMING VERIFY CYCLE

Background Information HM-6617 Programming

Programming Specifications

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{IL}	Input “0”	0.0	0.2	0.8	V
V_{IH}	Voltage “1” (Note 6)	VCC-2	V_{CC}	VCC+0.3	V
VCCPROG	Programming V_{CC} (Note 2)	12.0	12.0	12.5	V
V_{CC1}	Operating V_{CC}	4.5	5.5	5.5	V
V_{CC2}	Special Verify V_{CC} (Note 3)	4.0	-	6.0	V
tD	Delay Time	1.0	1.0	-	µs
tR	Rise Time	1.0	10.0	10.0	µs
tF	Fall Time	1.0	10.0	10.0	µs
TEHEL	Chip Enable Pulse Width	50	-	-	ns
TAVEL	Address Valid to Chip Enable Low Time	20	-	-	ns
TELQV	Chip Enable Low to Output Valid Time	-	-	120	ns
tPW	Programming Pulse Width (Note 4)	90	100	110	µs
tIP	Input Leakage at V_{CC} = VCCPROG	-10	+1.0	10	µA
IOP	Data Output Current at V_{CC} = VCCPROG	-	-5.0	-10	mA
Rn	Output Pull-Up Resistor (Note 5)	5	10	15	kΩ
T_A	Ambient Temperature	-	25	-	^{o}C

NOTES:

1. All inputs must track V_{CC} (pin 24) within these limits.
2. VCCPROG must be capable of supplying 500mA.
3. See Steps 22 through 29 of the Programming Algorithm.
4. See Step 11 of the Programming Algorithm.
5. All outputs should be pulled up to V_{CC} through a resistor of value Rn.
6. Except during programming (See Programming Cycle Waveforms).

Absolute Maximum Ratings

Supply Voltage (All Voltages Reference to Device GND) . . . . . +7.0V
Input or Output Voltage Applied for All Grades . . . . . GND -0.3V to V_{CC} +0.3V
Typical Derating Factor . . . . . 5mA/MHz Increase in ICCOP
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range: HM-6617-9, B-9 . . . -40°C to +85°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA}	θ_{JC}
SBDIP Package	48°C/W	9°C/W
Slim SBDIP	65°C/W	14°C/W
CLCC Package	58°C/W	19°C/W

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Junction Temperature . . . . . +175°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C

Die Characteristics

Gate Count . . . . . 5473 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications V_{CC} = 5V ±10%; (HM-6617B-9, HM-6617-9)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical One Input Voltage	2.4	VCC+0.3	V	V_{CC} = 5.5V
V_{IL}	Logical Zero Input Voltage	-0.3	0.8	V	V_{CC} = 4.5V
VOH1	Logical One Output Voltage	2.4	-	V	I_{OH} = -2.0mA, V_{CC} = 4.5V
VOH2	Logical One Output Voltage (Note 2)	VCC-1.0	-	V	I_{OH} = -100µA, V_{CC} = 4.5V
VOL	Logical Zero Output Voltage	-	0.4	V	I_{OL} = +4.8mA, V_{CC} = 4.5V
II	Input Leakage	-1.0	+1.0	µA	V_{IN} = V_{CC} or GND, V_{CC} = 5.5V
IOZ	Output Leakage	-1.0	+1.0	µA	V_O = V_{CC} or GND, $\overline{G}$ = V_{CC}, V_{CC} = 5.5V
ICCSB	Standby Power Supply Current	-	100	µA	V_{IN} = V_{CC} or GND, V_{CC} = 5.5V, I_O = 0
ICCOP	Operating Power Supply Current (Note 3)	-	20	mA	f = 1MHz, V_{CC} = 5.5V, I_O = 0, V_{IN} = V_{CC} or GND

AC Electrical Specifications

SYMBOL		PARAMETER	HM-6617B-9		HM-6617-9		UNITS	TEST CONDITIONS
			MIN	MAX	MIN	MAX		
(1)	TAVQV	Address Access Time	-	105	-	140	ns	(Notes 1, 4)
(2)	TELQV	Chip Enable Access Time	-	90	-	120	ns	(Notes 1, 4)
(3)	TELQX	Chip Enable Time	5	-	5	-	ns	(Notes 2, 4)
(4)	TAVEL	Address Setup Time	15	-	20	-	ns	(Notes 1, 4)
(5)	TELAX	Address Hold Time	20	-	25	-	ns	(Notes 1, 4)
(6)	TELEH	Chip Enable Low Width	95	-	120	-	ns	(Notes 1, 4)
(7)	TEHEL	Chip Enable High Width	40	-	40	-	ns	(Notes 1, 4)
(8)	TELEL	Cycle Time	136	-	160	-	ns	(Notes 1, 4)
(9)	TGLQV	Output Access Time	-	40	-	50	ns	(Notes 1, 4)
(10)	TGLQX	Output Enable Time	5	-	5	-	ns	(Notes 2, 4)
(11)	TGHQZ	Output Disable Time	-	40	-	50	ns	(Notes 2, 4)
(12)	TEHQZ	Chip Enable Disable Time	-	45	-	50	ns	(Notes 2, 4)

Capacitance $T_A = +25^oC$

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CIN	Input Capacitance (Note 2)	10	pF	f = 1MHz, All Measurement are Referenced to Device GND
COUT	Output Capacitance (Note 2)	12	pF	f = 1MHz, All Measurement are Referenced to Device GND

NOTES:

1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent C_L = 50pF (min) - for C_L greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 5mA/MHz increase in ICCOP.
4. V_{CC} = 4.5V and 5.5V.

Switching Waveforms

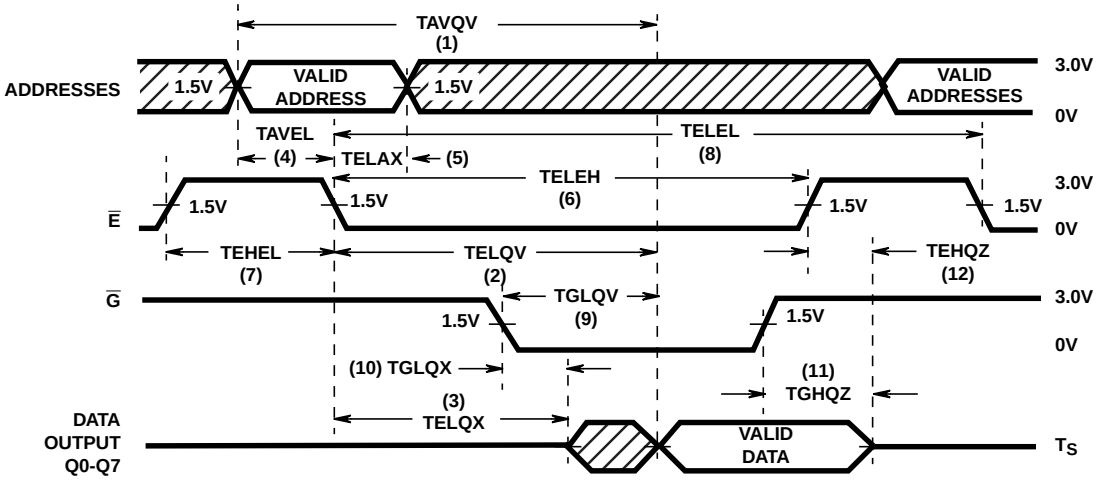


FIGURE 3. READ CYCLE

Test Circuit

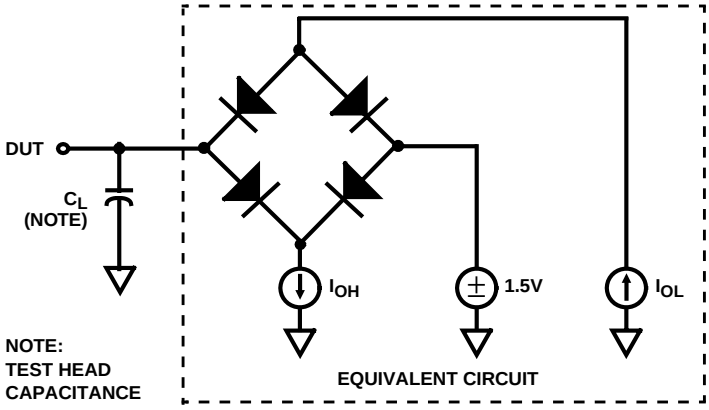


FIGURE 4. TEST CIRCUIT

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