128K x 8-Bit 3.3V Synchronous SRAM With ZBT™ and Pipelined Output

Preliminary
IDT71V508

Features

- **128K x 8 memory configuration**
- **High speed - 100 MHz (5 ns Clock-to-Data Access)**
- **Registered Output**
- **No dead cycles between Write and Read Cycles**
- **Low power deselect mode**
- **Single 3.3V power supply (±5%)**
- **Packaged in 44-lead SOJ**

Description

The IDT71V508 is a 3.3V high-speed 1,048,576-bit synchronous SRAM organized as 128K x 8. It is designed to eliminate dead cycles when turning the bus around between reads and writes, or writes and reads. Thus, it has been given the name ZBT™, or Zero Bus Turnaround.

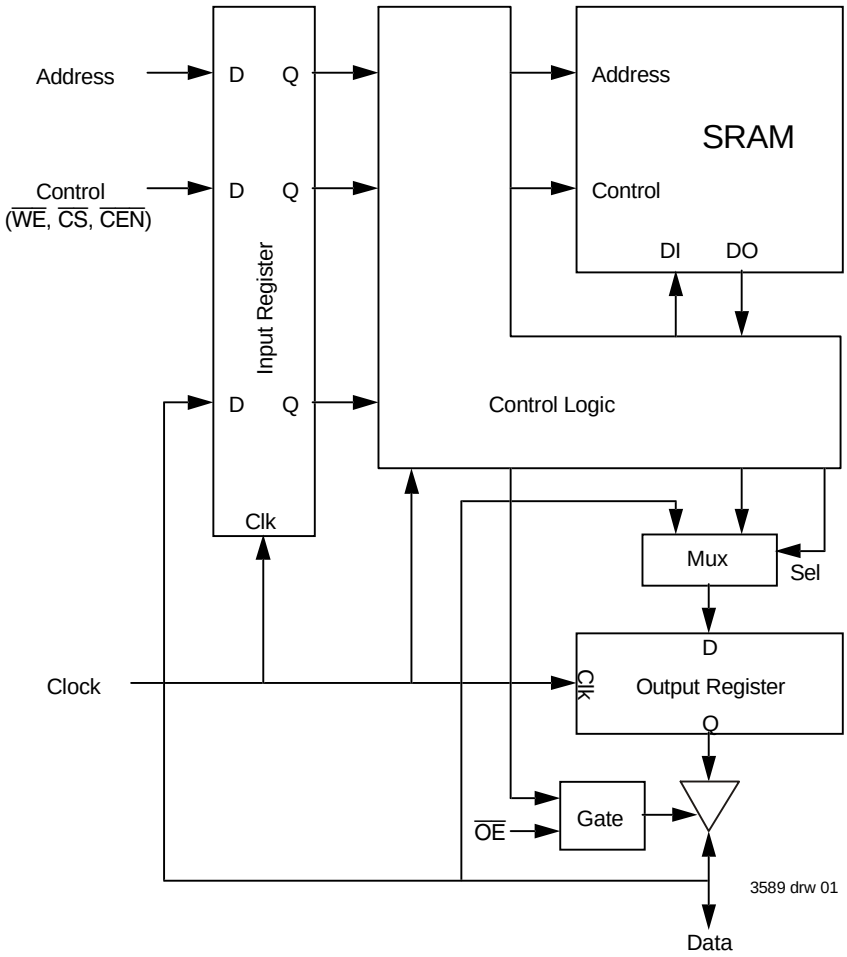
Addresses and control signals are applied to the SRAM during one clock cycle, and two clock cycles later its associated data cycle occurs, be it read or write.

The IDT71V508 contains data, address, and control signal registers. Output Enable is the only asynchronous signal, and can be used to disable the output at any time.

A Clock Enable ($\overline{CEN}$) pin allows operation of the IDT71V508 to be suspended as long as necessary. All synchronous inputs are ignored when $\overline{CEN}$ is high. A Chip Select ($\overline{CS}$) pin allows the user to deselect the device when desired. If $\overline{CS}$ is high, no new memory operation is initiated, but any pending data transfers (reads and writes) will still be completed.

The IDT71V508 utilizes IDT's high-performance 3.3V CMOS process, and is packaged in a JEDEC Standard 400-mil 44-lead small outline J-lead plastic package (SOJ) for high board density.

Functional Block Diagram



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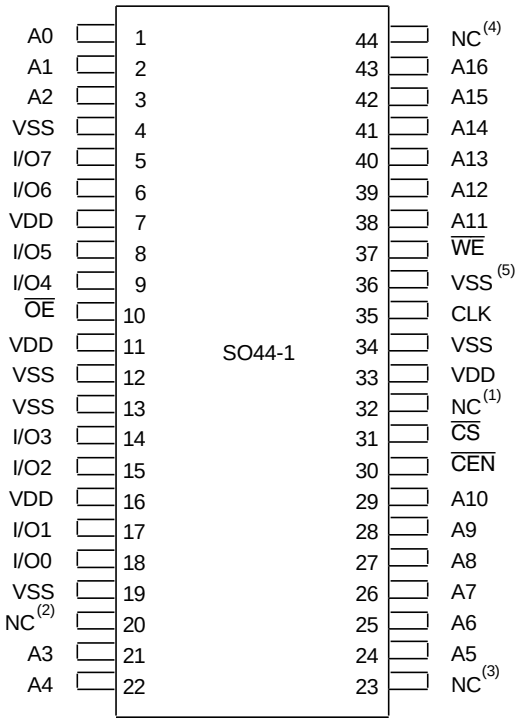
Pin Configuration



3589 drw 02

Top View

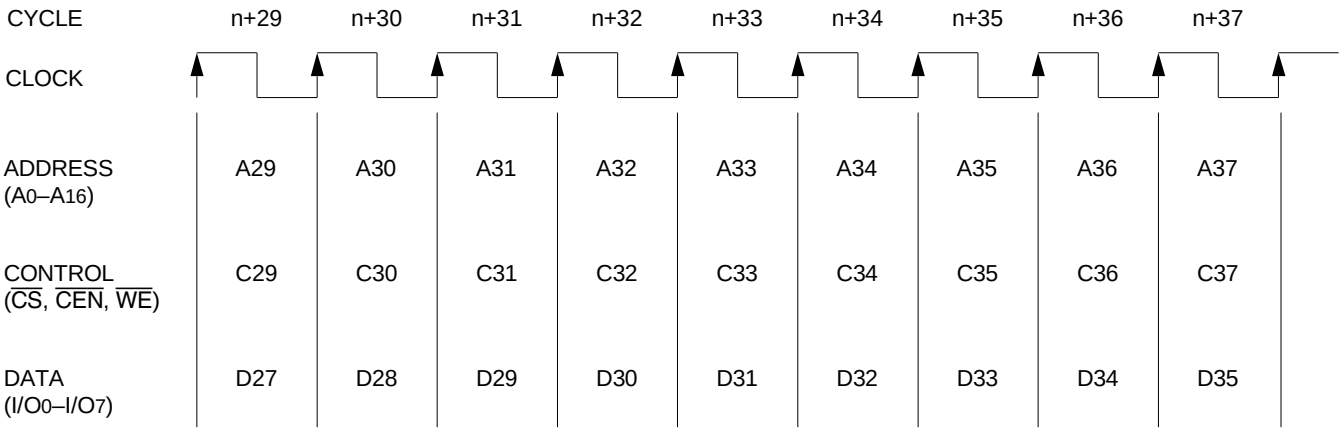
NOTES:
1. Pin 32: Future control input
2. Pin 20: Future I/O_8
3. Pin 23: Future A_{17}
4. Pin 44: Future A_{18}
5. Pin 36 does not need to to be connected directly to V_{SS}, as long as it is $\leq V_{IL}$.

Pin Definitions(1)

Symbol	Pin Function	I/O	Active	Description
A_0-A_{16}	Address Inputs	I	N/A	Synchronous Address inputs. The address is registered on every rising edge of CLK if $\overline{CEN}$ and $\overline{CS}$ are both low.
CLK	Clock	I	N/A	The clock input. Except for $\overline{OE}$, all input and output timing references for the device are with respect to the rising edge of CLK.
$\overline{CEN}$	Clock Enable	I	LOW	Synchronous clock enable input. When $\overline{CEN}$ is sampled high, the other synchronous inputs are ignored, and outputs remain unchanged. When $\overline{CEN}$ is sampled low, the IDT71V508 operates normally.
$\overline{CS}$	Chip Select	I	LOW	Synchronous chip select input. When $\overline{CS}$ is sampled low, the device operates normally. When $\overline{CS}$ is sampled high, no read or write operation is initiated, and the I/O bus is tri-stated the cycle after next. $\overline{CS}$ is ignored if $\overline{CEN}$ is high at the same rising edge of clock..
$\overline{WE}$	Write Enable	I	LOW	Synchronous write enable. If $\overline{WE}$ is sampled low, a write is initiated at the address that is registered at that time. If $\overline{WE}$ is sampled high, a read is initiated at the address that is registered at that time. $\overline{WE}$ is ignored when either $\overline{CEN}$ or $\overline{CS}$ is sampled high.
$\overline{OE}$	Output Enable	I	LOW	Asynchronous output enable. When $\overline{OE}$ is high, the I/O bus goes high impedance. $\overline{OE}$ must be low to read data from the IDT71V508.
I/O_0-I/O_7	Data Input/Output	I/O	N/A	Synchronous data input/output (I/O) pins. Both the data input path and data output path are registered and triggered by the rising edge of CLK.
V_{DD}	Power Supply	N/A	N/A	3.3V power supply pins.
V_{SS}	Ground	N/A	N/A	Ground pins.

3589 tbl 01

Functional Timing Diagram



3589 drw 03

Typical Operation — $\overline{CS}$ and $\overline{CEN}$ are Low

Cycle	Address	$\overline{WE}$	$\overline{CS}$	$\overline{CEN}$	$\overline{OE}$	I/O	Comments
n	A0	H	L	L	?	D-2	?
n+1	A1	L	L	L	?	D-1	?
n+2	A2	H	L	L	L	D0	Data Out
n+3	A3	L	L	L	X	D1	Data In
n+4	A4	H	L	L	L	D2	Data Out
n+5	A5	L	L	L	X	D3	Data In
n+6	A6	H	L	L	L	D4	Data Out
n+7	A7	L	L	L	X	D5	Data In
n+8	A8	H	L	L	L	D6	Data Out
n+9	A9	L	L	L	X	D7	Data In
n+10	A10	H	L	L	L	D8	Data Out
n+11	A11	H	L	L	X	D9	Data In
n+12	A12	L	L	L	L	D10	Data Out
n+13	A13	L	L	L	L	D11	Data Out
n+14	A14	H	L	L	X	D12	Data In
n+15	A15	H	L	L	X	D13	Data In
n+16	A16	H	L	L	L	D14	Data Out
n+17	A17	L	L	L	L	D15	Data Out
n+18	A18	L	L	L	L	D16	Data Out
n+19	A19	L	L	L	X	D17	Data In
n+20	A20	H	L	L	X	D18	Data In
n+21	A21	H	L	L	X	D19	Data In

3589 tbl 02

Read Operation(1)

Cycle	Address	$\overline{WE}$	$\overline{CS}$	$\overline{CEN}$	$\overline{OE}$	I/O	Comments
n	A0	H	L	L	X	X	Address and Control meet setup
n+1	X	X	X	L	X	X	Clock Setup Valid
n+2	X	X	X	X	L	D0	Contents of Address A0 Read Out

3589 tbl 03

NOTE:
1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance

Write Operation(1)

Cycle	Address	$\overline{WE}$	$\overline{CS}$	$\overline{CEN}$	$\overline{OE}$	I/O	Comments
n	A0	L	L	L	X	X	Address and Control meet setup
n+1	X	X	X	L	X	X	Clock Setup Valid
n+2	X	X	X	L	X	D0	New Data Drives SRAM Inputs

3589 tbl 04

NOTE:
1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance

Read Operation with Clock Enable Used(1)

Cycle	Address	$\overline{WE}$	$\overline{CS}$	$\overline{CEN}$	$\overline{OE}$	I/O	Comments
n	A0	H	L	L	X	X	Address and Control meet setup
n+1	X	X	X	H	X	X	Clock Ignored at n+1 to n+2 Low-to-High
n+2	A2	H	L	L	X	X	Clock Valid
n+3	X	X	X	H	L	D0	Contents of Address A0 Read Out
n+4	X	X	X	H	L	D0	Contents of Address A0 Read Out
n+5	A5	H	L	L	L	D0	Contents of Address A0 Read Out
n+6	A6	?	L	L	L	D2	Contents of Address A2 Read Out
n+7	A7	?	L	L	L	D5	Contents of Address A5 Read Out

3589 tbl 05

NOTE:
1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High ImpedanceH = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance

Write Operation with Clock Enable Used(2)

Cycle	Address	$\overline{WE}$	$\overline{CS}$	$\overline{CEN}$	$\overline{OE}$	I/O	Comments
n	A0	L	L	L	X	X	Address and Control meet setup
n+1	X	X	X	H	X	X	Clock Ignored at n+1 to n+2 Low-to-High
n+2	A2	L	L	L	X	X	Clock Valid
n+3	X	X	X	H	X	di(1)	Clock Ignored at n+3 to n+4 Low-to-High
n+4	X	X	X	H	X	di(1)	Clock Ignored at n+4 to n+5 Low-to-High
n+5	A5	L	L	L	X	D0	New Data Drives SRAM Inputs
n+6	A6	?	L	L	X	D2	New Data Drives SRAM Inputs
n+7	A7	?	L	L	X	D5	New Data Drives SRAM Inputs

3589 tbl 06

NOTES:
1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedancedi = Could be D0 if desired
2. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance

Read Operation with Chip Select Used(1)

Cycle	Address	$\overline{WE}$	$\overline{CS}$	$\overline{CEN}$	$\overline{OE}$	I/O	Comments
n	X	X	H	L	X	?	Deselected
n+1	X	X	H	L	X	?	Deselected
n+2	A2	H	L	L	X	Z	Address and Control meet setup
n+3	X	X	H	L	X	Z	Deselected
n+4	A4	H	L	L	L	D2	Address and Control meet setup, Contents of Address A2 Read Out
n+5	X	X	H	L	X	Z	Deselected
n+6	X	X	H	L	L	D4	Deselected, Contents of Address A4 Read Out
n+7	A7	H	L	L	X	Z	Address and Control meet setup
n+8	X	X	H	L	X	Z	
n+9	X	X	H	L	L	D7	Contents of Address A7 Read Out

3589 tbl 07

NOTE:
1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High ImpedanceH = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance

Write Operation with Chip Select Used(1)

Cycle	Address	$\overline{WE}$	$\overline{CS}$	$\overline{CEN}$	$\overline{OE}$	I/O	Comments
n	X	X	H	L	X	?	Deselected
n+1	X	X	H	L	X	?	Deselected
n+2	A2	L	L	L	X	Z	Address and Control meet setup
n+3	X	X	H	L	X	Z	Deselected
n+4	A4	L	L	L	X	D2	Address and Control meet setup, New Data Drives SRAM Inputs
n+5	X	X	H	L	X	Z	Deselected
n+6	X	X	H	L	X	D4	Deselected, New Data Drives SRAM Inputs
n+7	A7	L	L	L	X	Z	Address and Control meet setup
n+8	X	X	X	L	X	Z	
n+9	X	X	X	L	X	D7	New Data Drives SRAM Inputs

3589 tbl 08

NOTE:
1. H = High; L = Low; X = Don't Care; ? = Don't Know; Z = High ImpedanceH = High; L = Low; X = Don't Care; ? = Don't Know; Z = High Impedance

Absolute Maximum Ratings(1)

Symbol	Rating	Value	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	-0.5 to V_{DD}+0.5	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-55 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

3589 tbl 09

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{DD} and Input terminals only.
3. I/O terminals.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	3.135	3.3	3.465	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage - Inputs	2.0	—	4.6	V
V_{IH}	Input High Voltage - I/O	2.0	—	V_{DD} +0.3	V
V_{IL}	Input Low Voltage	-0.3(1)	—	0.8	V

3589 tbl 10

NOTE:
1. V_{IL} (min.) = –1.5V for pulse width less than 5 ns, once per cycle.

Capacitance
(T_A = +25°C, f = 1.0MHz, SOJ Package)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	6	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 3dV	7	pF

3589 tbl 11

NOTE:
1. This parameter is guaranteed by device characterization, but not production tested.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 3.3V ±5%)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{DD} = Max., V_{IN} = 0V to V_{DD}	—	5	
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS} \geq V_{IH}$, V_{OUT} = 0V to V_{DD}, V_{DD} = Max.	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 5mA, V_{DD} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -5mA, V_{DD} = Min.	2.4	—	V

3589 tbl 12

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(1) (V_{DD} = 3.3V ±5%, V_{HD} = V_{DD} - 0.2V, V_{LD} = 0.2V)

Symbol	Parameter	Test Conditions	71V508S100	71V508S80	Unit
I_{DD}	Operating Power Supply Current	$\overline{CS} \leq V_{IL}$, Outputs Open, V_{DD} = Max., $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$, f = f_{MAX}(2)	220	180	mA
I_{SB}	Standby Power Supply Current	$\overline{CS} \geq V_{IH}$, Outputs Open, V_{DD} = Max., $V_{IN} \geq V_{IH}$ or $\leq V_{IL}$, f = f_{MAX}(2)	80	75	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS} \geq V_{HD}$, Outputs Open, V_{DD} = Max., $V_{IN} \geq V_{HD}$ or $\leq V_{LD}$, f = 0(2)	25	25	mA

3589 tbl 13

NOTES:
1. All values are maximum guaranteed values.
2. At f = f_{MAX}, address inputs are switching at 1/t_{CYC} and CLK is cycling at 1/t_{CYC}; f=0 means no input signals are changing.

AC Electrical Characteristics (V_{DD} = 3.3V ±5%, T_A = 0 to 70°C)

Symbol	Parameter	IDT71V508S100		IDT71V508S80		Unit
		Min.	Max.	Min.	Max.	
Clock Parameters						
f_{MAX}	Clock Frequency	—	100	—	80	MHz
t_{CYC}	Clock Cycle Time	10	—	12.5	—	ns
t_{CH}	Clock High Pulse Width	4	—	4	—	ns
t_{CL}	Clock Low Pulse Width	4	—	4	—	ns
Output Parameters						
t_{CD}	Clock High to Valid Data	—	5	—	7	ns
t_{CDC}	Clock High to Data Change	2	—	2	—	ns
t_{CLZ}[1]	Clock High to Output Active	2	—	2	—	ns
t_{CHZ}[1]	Clock High to Data High-Z	2	4	2	5	ns
t_{OE}	Output Enable Access Time	—	5	—	6	ns
t_{OLZ}[1]	Output Enable Low to Data Active	0	—	0	—	ns
t_{OHZ}[1]	Output Enable High to Data High-Z	—	5	—	6	ns
Setup Times						
t_{SE}	Clock Enable Setup Time	2	—	2	—	ns
t_{SA}	Address Setup Time	1.5	—	2	—	ns
t_{SD}	Data in Setup Time	1.5	—	2	—	ns
t_{SW}	Write Enable Setup Time	1.5	—	2	—	ns
t_{SC}	Chip Select Setup Time	1.5	—	2	—	ns
Hold Times						
t_{HE}	Clock Enable Hold Time	1	—	1	—	ns
t_{HA}	Address Hold Time	2.5	—	2.5	—	ns
t_{HD}	Data in Hold Time	1	—	1	—	ns
t_{HW}	Write Enable Hold Time	1	—	1	—	ns
t_{HC}	Chip Select Hold Time	1	—	1	—	ns

3589 tbl 14

NOTE:
1. Transition is measured ±200mV from steady-state.

AC Test Conditions

Input Pulse Levels	0 to 3.0V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

3589 tbl 15

AC Test Loads

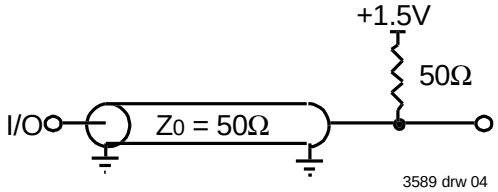
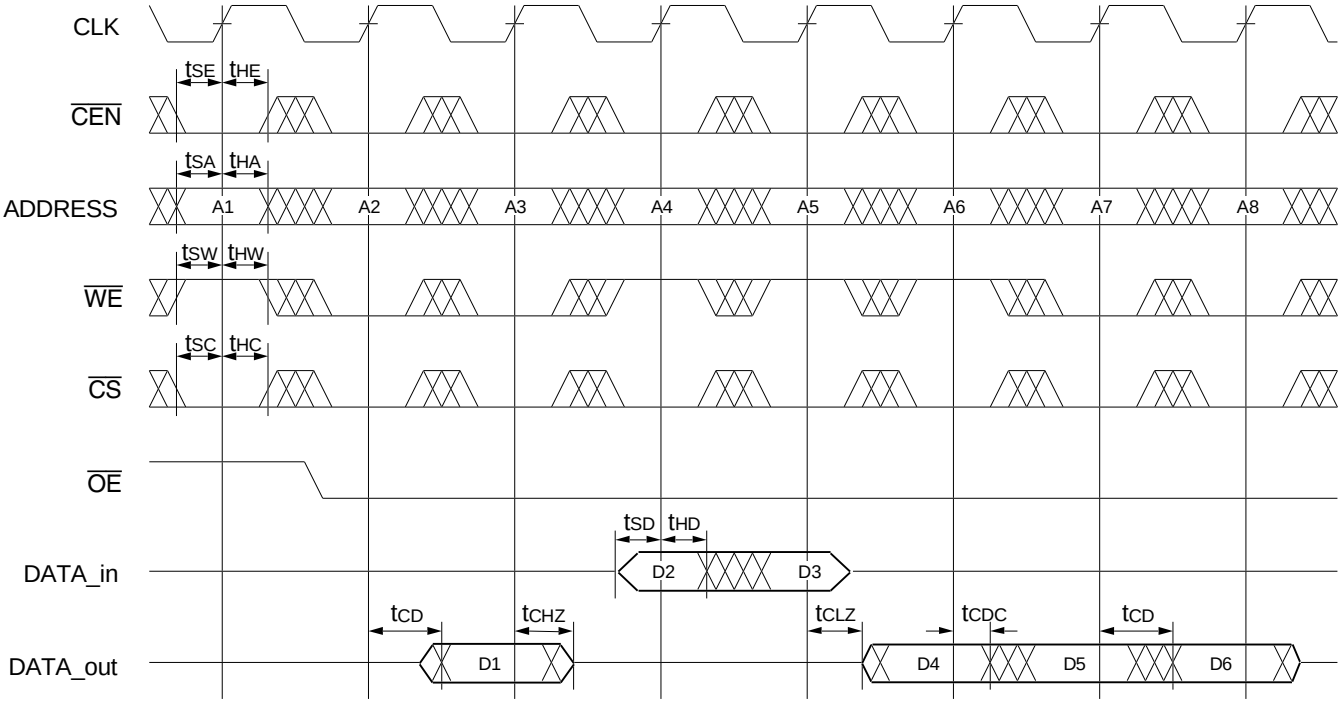


Figure 1. AC Test Load

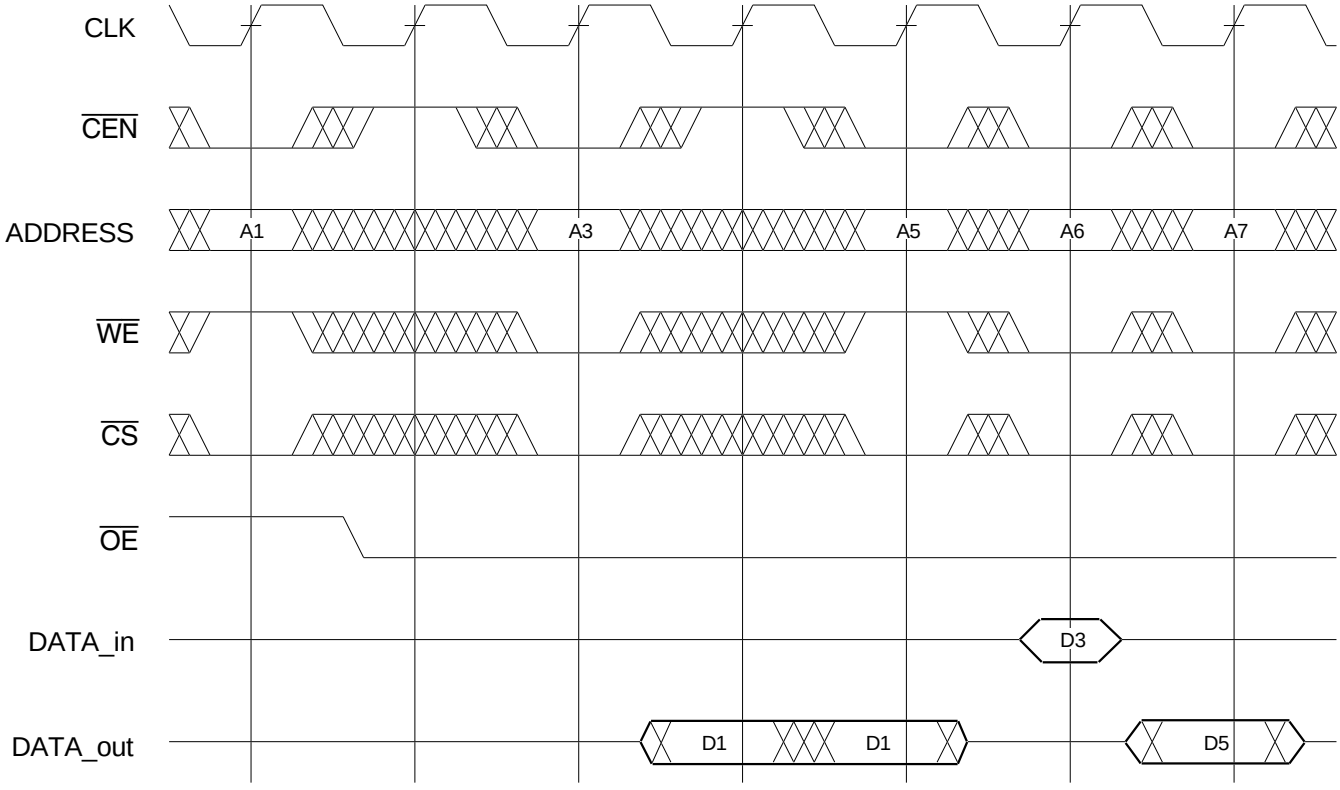
Timing Waveform of Read and Write Cycles(1)



3589 drw 05

NOTES:
1. Dx represents the data for address Ax.
2. DATA_in and DATA_out together represent I/O(7:0).

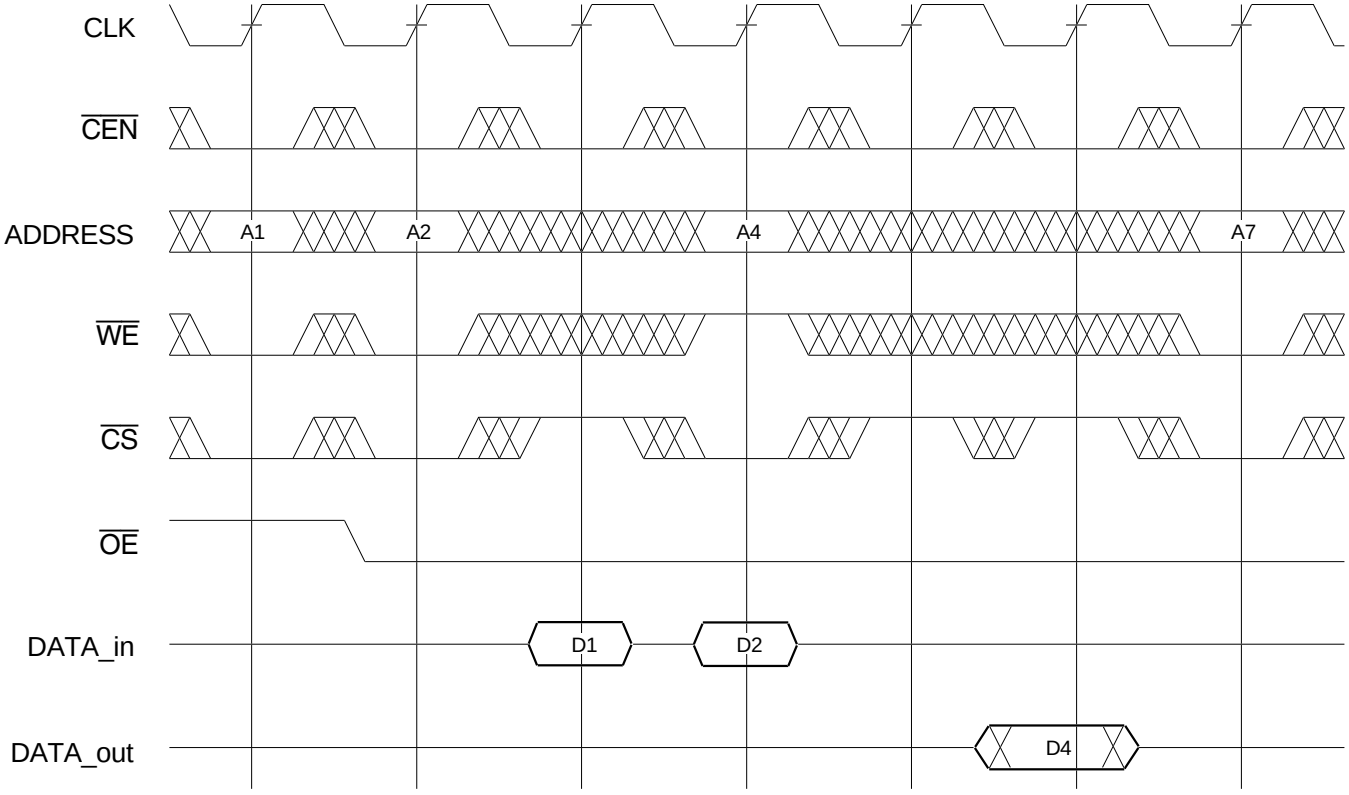
Timing Waveform of $\overline{\text{CEN}}$ Operation(1)



3589 drw 06

NOTES:
1. Dx represents the data for address Ax.
2. DATA_in and DATA_out together represent I/O(7:0).

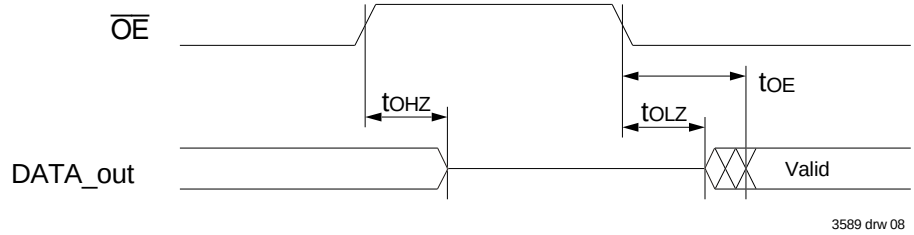
Timing Waveform of $\overline{CS}$ Operation(1)



3589 drw 07

NOTES:
1. Dx represents the data for address Ax.
2. DATA_in and DATA_out together represent I/O(7:0).

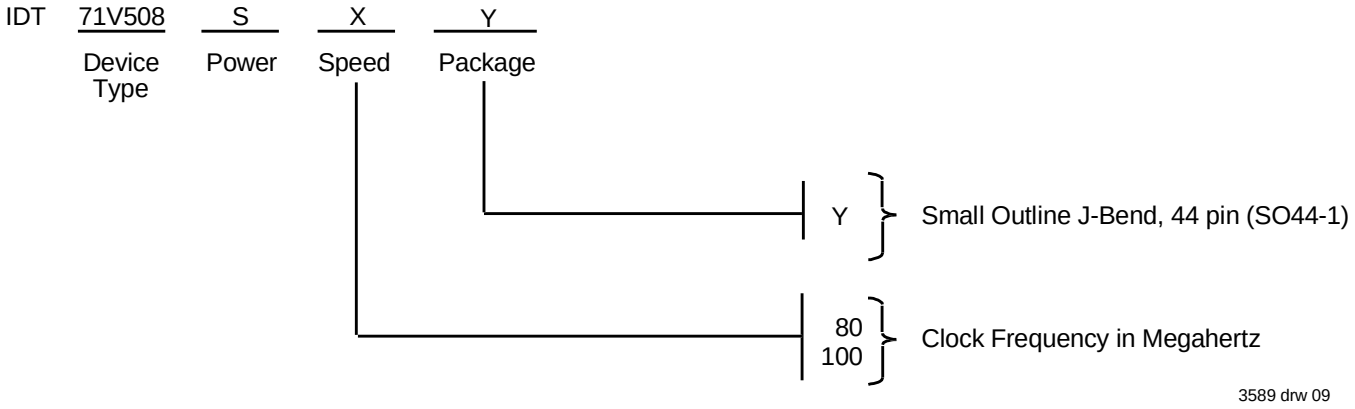
Timing Waveform of $\overline{OE}$ Operation



3589 drw 08

NOTE:
1. A read operation is assumed to be in progress.

Ordering Information



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