80C286/883

High Performance Microprocessor with Memory Management and Protection

March 1997

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Compatible with NMOS 80286/883**
- **Static CMOS Design for Low Power Operation**
  - **ICCSB = 5mA Maximum**
  - **ICCOP = 185mA Maximum (80C286-10/883)**
  - **ICCOP = 220mA Maximum (80C286-12/883)**
- **Large Address Space**
  - **16 Megabytes Physical**
  - **1 Gigabyte Virtual per Task**
- **Integrated Memory Management, Four-Level Memory Protection and Support for Virtual Memory and Operating Systems**
- **Two 80C86 Upward Compatible Operating Modes**
  - **80C286/883 Real Address Mode**
  - **Protected Virtual Address Mode**
- **Compatible with 80287 Numeric Data Co-Processor**

Description

The Intersil 80C286/883 is a static CMOS version of the NMOS 80286 microprocessor. The 80C286/883 is an advanced, high-performance microprocessor with specially optimized capabilities for multiple user and multi-tasking systems. The 80C286/883 has built-in memory protection that supports operating system and task isolation as well as program and data privacy within tasks. The 80C286/883 includes memory management capabilities that map 230 (one gigabyte) of virtual address space per task into 2^{24} bytes (16 megabytes) of physical memory.

The 80C286/883 is upwardly compatible with 80C86 and 80C88 software (the 80C286/883 instruction set is a superset of the 80C86/80C88 instruction set). Using the 80C286/883 real address mode, the 80C286/883 is object code compatible with existing 80C86 and 80C88 software. In protected virtual address mode, the 80C286/883 is source code compatible with 80C86 and 80C88 software but may require upgrading to use virtual address as supported by the 80C286/883's integrated memory management and protection mechanism. Both modes operate at full 80C286/883 performance and execute a superset of the 80C86 and 80C88 instructions.

The 80C286/883 provides special operations to support the efficient implementation and execution of operating systems. For example, one instruction can end execution of one task, save its state, switch to a new task, load its state, and start execution of the new task. The segment-not-present exception and restartable instructions.

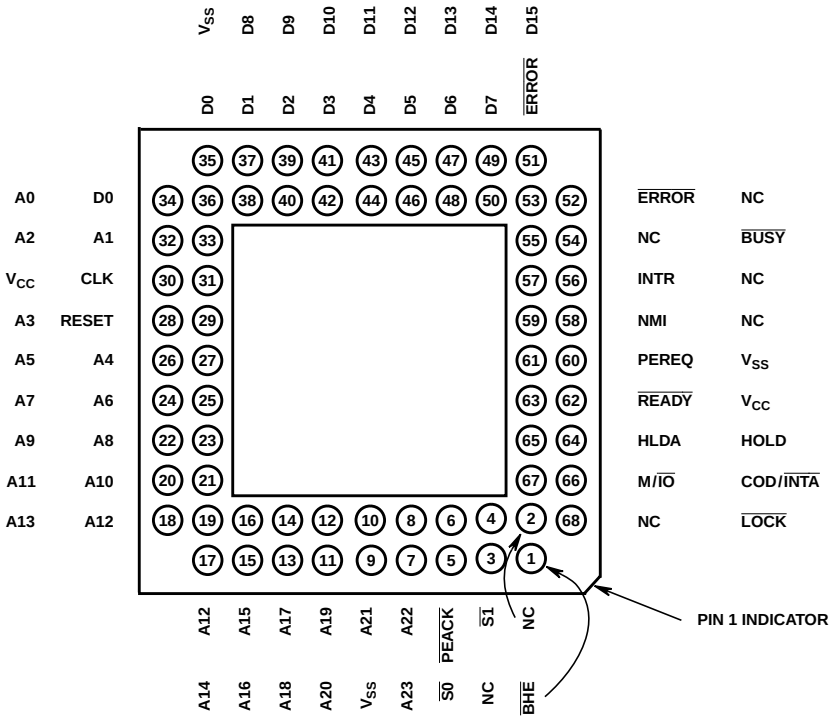
Ordering Information

PACKAGE	TEMP. RANGE	10MHz	12.5MHz	16MHz	20MHz	25MHz	PKG. NO.
68 Pin PGA	0^oC to $+70^oC$	-	CG80C286-12	CG80C286-16	CG80C286-20	-	G68.B
	-40^oC to $+85^oC$	IG80C286-10	IG80C286-12	-	-	-	G68.B
	-55^oC to $+125^oC$	MG80C286-10/883	MG80C286-12/883	-	-	-	G68.B
		5962-9067801MXC	5962-9067802MXC	-	-	-	G68.B

Pinout

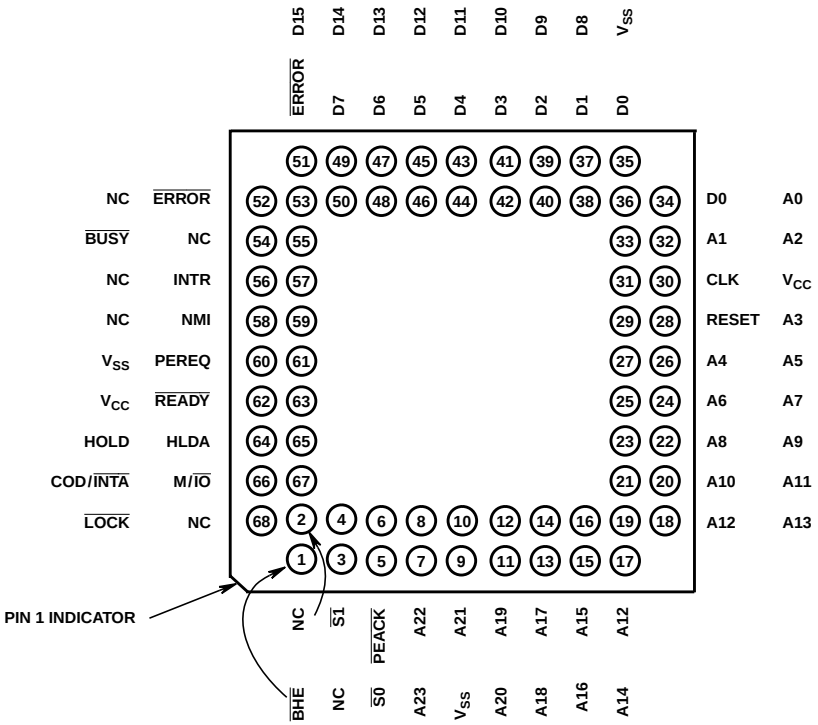
68 LEAD PGA, COMPONENT PAD VIEW

As viewed from underside of the component when mounted on the board.



P.C. BOARD VIEW

As viewed from the component side of the P.C. board.



Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage Applied . . . . . GND -1.0V to V_{CC} +1.0V
Storage Temperature Range . . . . . -65^oC to $+150^oC$
Junction Temperature . . . . . $+175^oC$
Lead Temperature (Soldering 10s) . . . . . $+300^oC$
ESD Classification . . . . . Class 1

Thermal Information

Thermal Resistance (Typical)	θ_{JA}	θ_{JC}
PGA Package	$35^oC/W$	$6^oC/W$

Gate Count . . . . . 22,500 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range . . . . . -55^oC to $+125^oC$
System Clock (CLK) RISE Time (From 1.0V to 3.6V . . . . 8ns (Max)
System Clock (CLK) FALL Time (from 3.6V to 1.0V) . . . . 8ns (Max)
Input RISE and FALL Time (From 0.8V to 2.0V
80C286-10/883 . . . . . 10ns (Max)
80C286-12/883 . . . . . 8ns (Max)

TABLE 1. 80C286/883 D.C. ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input LOW Voltage	V_{IL}	V_{CC} = 4.5V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-0.5	0.8	V
Input HIGH Voltage	V_{IH}	V_{CC} = 5.5V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	2.0	V_{CC} +0.5	V
CLK Input LOW Voltage	V_{ILC}	V_{CC} = 4.5V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-0.5	1.0	V
CLK Input HIGH Voltage	V_{IHC}	V_{CC} = 5.5V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	3.6	V_{CC} +0.5	V
Output LOW Voltage	V_{OL}	I_{OL} = 2.0mA, V_{CC} = 4.5V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	0.4	V
Output HIGH Voltage	V_{OH}	I_{OH} = -2.0mA, V_{CC} = 4.5V	1, 2, 3	$-55^oC \le T_A \le +125^oC$	3.0	-	V
		I_{OH} = -100µA, V_{CC} = 4.5V			V_{CC} -0.4	-	V
Input Leakage Current	I_I	V_{IN} = GND or V_{CC}, V_{CC} = 5.5V, Pins 29, 31, 57, 59, 61, 63-64	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-10	10	µA
Input Sustaining Current LOW	I_{BHL}	V_{CC} = 4.5V and 5.5V, V_{IN} = 1.0V, Note 1	1, 2, 3	$-55^oC \le T_A \le +125^oC$	38	200	µA
Input Sustaining Current HIGH	I_{BHH}	V_{CC} = 4.5V and 5.5V, V_{IN} = 3.0V, Note 2	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-50	-400	µA
Input Sustaining Current on $\overline{BUSY}$ and $\overline{ERROR}$ Pins	I_{SH}	V_{CC} = 4.5V and 5.5V V_{IN} = GND, Note 5	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-30	-500	µA
Output Leakage Current	I_O	V_O = GND or V_{CC} V_{CC} = 5.5V, Pins 1, 7-8, 10-28, 32-34	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-10	10	µA
Active Power Supply Current	I_{CCOP}	80C286-10/883, Note 4	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	185	mA
		80C286-12/883, Note 4			-	220	mA
Standby Power Supply Current	I_{CCSB}	V_{CC} = 5.5V, Note 3	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	5	mA

NOTES:

2. I_{BHL} should be measured after lowering V_{IN} to GND and then raising to 1.0V on the following pins: 36-51, 66, 67.
3. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering to 3.0V on the following pins: 4-6, 36-51, 66-68.
4. I_{CCSB} should be tested with the clock stopped in phase two of the processor clock cycle. V_{IN} = V_{CC} or GND, V_{CC} = 5.5V, outputs unloaded.
5. I_{CCOP} measured at 10MHz for the 80C286-10/883 and 12.5MHz for the 80C286-12/883. V_{IN} = 2.4V or 0.4V, V_{CC} = 5.5V, outputs unloaded.
6. I_{SH} should be measured after raising V_{IN} to V_{CC} and then lowering to 0V on pins 53 and 54.

TABLE 2. 80C286/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS

AC Timings are Referenced to 0.8V and 2.0V Points of the Signals as Illustrated in Datasheet Waveforms, Unless Otherwise Noted. Device Guaranteed and 100% Tested.

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	80C286/883				UNITS
					10MHz		12.5MHz		
					MIN	MAX	MIN	MAX	
System Clock (CLK) Period	1	V_{CC} = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	50	-	40	-	ns
System Clock (CLK) Low Time	2	V_{CC} = 4.5V and 5.5V at 1.0V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	12	-	11	-	ns
System Clock (CLK) High Time	3	V_{CC} = 4.5V and 5.5V at 3.6V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	16	-	13	-	ns
Asynchronous Inputs SETUP Time (Note 1)	4	V_{CC} = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	20	-	15	-	ns
Asynchronous Inputs HOLD Time (Note 1)	5	V_{CC} = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	20	-	15	-	ns
RESET SETUP Time	6	V_{CC} = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	19	-	10	-	ns
RESET HOLD Time	7	V_{CC} = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	ns
Read Data SETUP Time	8	V_{CC} = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	8	-	5	-	ns
Read Data HOLD Time	9	V_{CC} = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	4	-	4	-	ns
$\overline{\text{READY}}$ SETUP Time	10	V_{CC} = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	26	-	20	-	ns
$\overline{\text{READY}}$ HOLD Time	11	V_{CC} = 4.5V and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	25	-	20	-	ns
Status/$\overline{\text{PEACK}}$ Active Delay, (Note 4)	12A	V_{CC} = 4.5V and 5.5V, C_L = 100pF I_L = |2mA|	9, 10, 11	$-55^oC \le T_A \le +125^oC$	1	22	1	21	ns
Status/$\overline{\text{PEACK}}$ Inactive Delay (Note 3)	12B	V_{CC} = 4.5V and 5.5V, C_L = 100pF I_L = |2mA|	9, 10, 11	$-55^oC \le T_A \le +125^oC$	1	30	1	24	ns
Address Valid Delay (Note 2)	13	V_{CC} = 4.5V and 5.5V, C_L = 100pF I_L = |2mA|	9, 10, 11	$-55^oC \le T_A \le +125^oC$	1	35	1	32	ns
Write Data Valid Delay, (Note 2)	14	V_{CC} = 4.5V and 5.5V, C_L = 100pF I_L = |2mA|	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	40	0	31	ns

TABLE 2. 80C286/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS (Continued)

AC Timings are Referenced to 0.8V and 2.0V Points of the Signals as Illustrated in Datasheet Waveforms, Unless Otherwise Noted. Device Guaranteed and 100% Tested.

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	80C286/883				UNITS
					10MHz		12.5MHz		
					MIN	MAX	MIN	MAX	
HLDA Valid Delay (Note 5)	15	V_{CC} = 4.5V and 5.5V, C_L = 100pF IL = |2mA|	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	47	0	25	ns

NOTES:

1. Asynchronous inputs are INTR, NMI, HOLD, PEREQ, ERROR, and BUSY. This specification is given only for testing purposes, to assure recognition at a specific CLK edge.
2. Delay from 1.0V on the CLK to 0.8V or 2.0V.
3. Delay from 1.0V on the CLK to 0.8V for Min (HOLD time) and to 2.0V for Max (inactive delay).
4. Delay from 1.0V on the CLK to 2.0V for Min (HOLD time) and to 0.8V for Max (active delay).
5. Delay from 1.0V on the CLK to 2.0V.

TABLE 3. 80C286/883 ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	80C286/883				UNITS
					10MHz		12.5MHz		
					MIN	MAX	MIN	MAX	
CLK Input Capacitance	C_{CLK}	FREQ = 1MHz	5	$T_A = +25^oC$	-	10	-	10	pF
Other Input Capacitance	C_{IN}	FREQ = 1MH	5	$T_A = +25^oC$	-	10	-	10	pF
I/O Capacitance	$C_{I/O}$	FREQ = 1MH	5	$T_A = +25^oC$	-	10	-	10	pF
Address/Status/Data Float Delay	15		1, 3, 4, 5	$-55^oC \le T_A \le +125^oC$	0	47	0	32	ns
Address Valid to Status SETUP Time	19	I_L = |2.0mA|	1, 2, 5	$-55^oC \le T_A \le +125^oC$	27	-	20	-	ns

NOTES:

1. Output Load: C_L = 100pF.
2. Delay measured from address either reaching 0.8V or 2.0V (valid) to status going active reaching 0.8V or status going inactive reaching 2.0V.
3. Delay from 1.0V on the CLK to Float (no current drive) condition.
4. I_L = -6mA (V_{OH} to Float), I_L = 8mA (V_{OL} to Float).
5. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group C & D	Samples/5005	1, 7, 9

AC Electrical Specifications

82C284 and 82C288 Timing Specifications Are Given For Reference Only, And No Guarantee is Implied.

82C284 Timing

SYMBOL	PARAMETER	10MHz		12.5MHz		UNIT	TEST CONDITION
		MIN	MAX	MIN	MAX		
TIMING REQUIREMENTS							
11	$\overline{SRDY}$/$\overline{SRDYEN}$ Setup Time	15	-	15	-	ns	
12	$\overline{SRDY}$/$\overline{SRDYEN}$ Hold Time	2	-	2	-	ns	
13	$\overline{ARDY}$/$\overline{ARDYEN}$ Setup Time	5	-	5	-	ns	(Note 1)
14	$\overline{ARDY}$/$\overline{ARDYEN}$ Hold Time	30	-	25	-	ns	(Note 1)
TIMING RESPONSES							
19	PCLK Delay	0	20	0	16	ns	C_L = 75pF, I_{OL} = 5mA, I_{OH} = -1mA

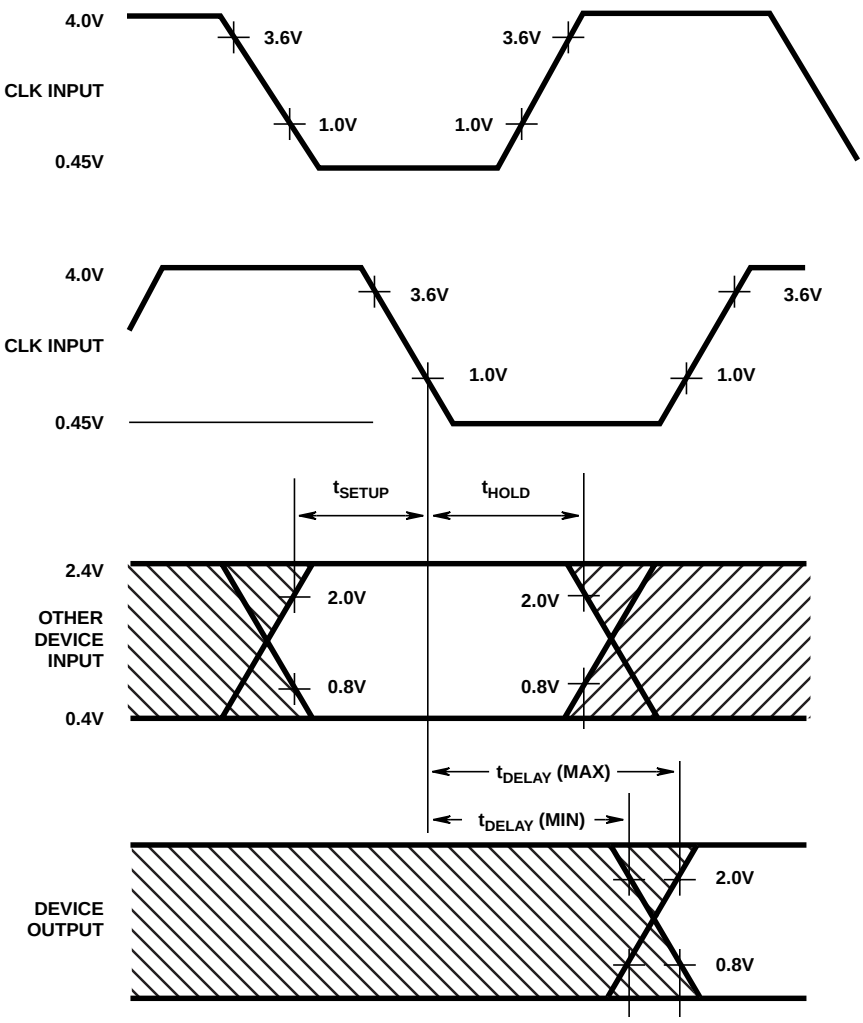
NOTE:

1. These times are given for testing purposes to ensure a predetermined action.

82C288 Timing

SYMBOL	PARAMETER	10MHz		12.5MHz		UNIT	TEST CONDITION
		MIN	MAX	MIN	MAX		
TIMING REQUIREMENTS							
12	CMDLY Setup Time	15	-	15	-	ns	
13	CMDLY Hold Time	1	-	1	-	ns	
TIMING RESPONSES							
16	ALE Active Delay	1	16	1	16	ns	
17	ALE Inactive Delay	-	19	-	19	ns	
19	DT/$\overline{R}$ Read Active Delay	-	23	-	23	ns	C_L = 150pF
20	DEN Read Active Delay	0	21	0	21	ns	I_{OL} = 16mA Max
21	DEN Read Inactive Delay	3	23	3	21	ns	I_{OH} = -1mA Max
22	DT/$\overline{R}$ Read Inactive Delay	5	24	5	18	ns	
23	DEN Write Active Delay	-	23	-	23	ns	
24	DEN Write Inactive Delay	3	23	3	23	ns	
29	Command Active Delay from CLK	3	21	3	21	ns	C_L = 300pF
30	Command Inactive Delay from CLK	3	20	3	20	ns	I_{OL} = 32mA Max

AC Specifications

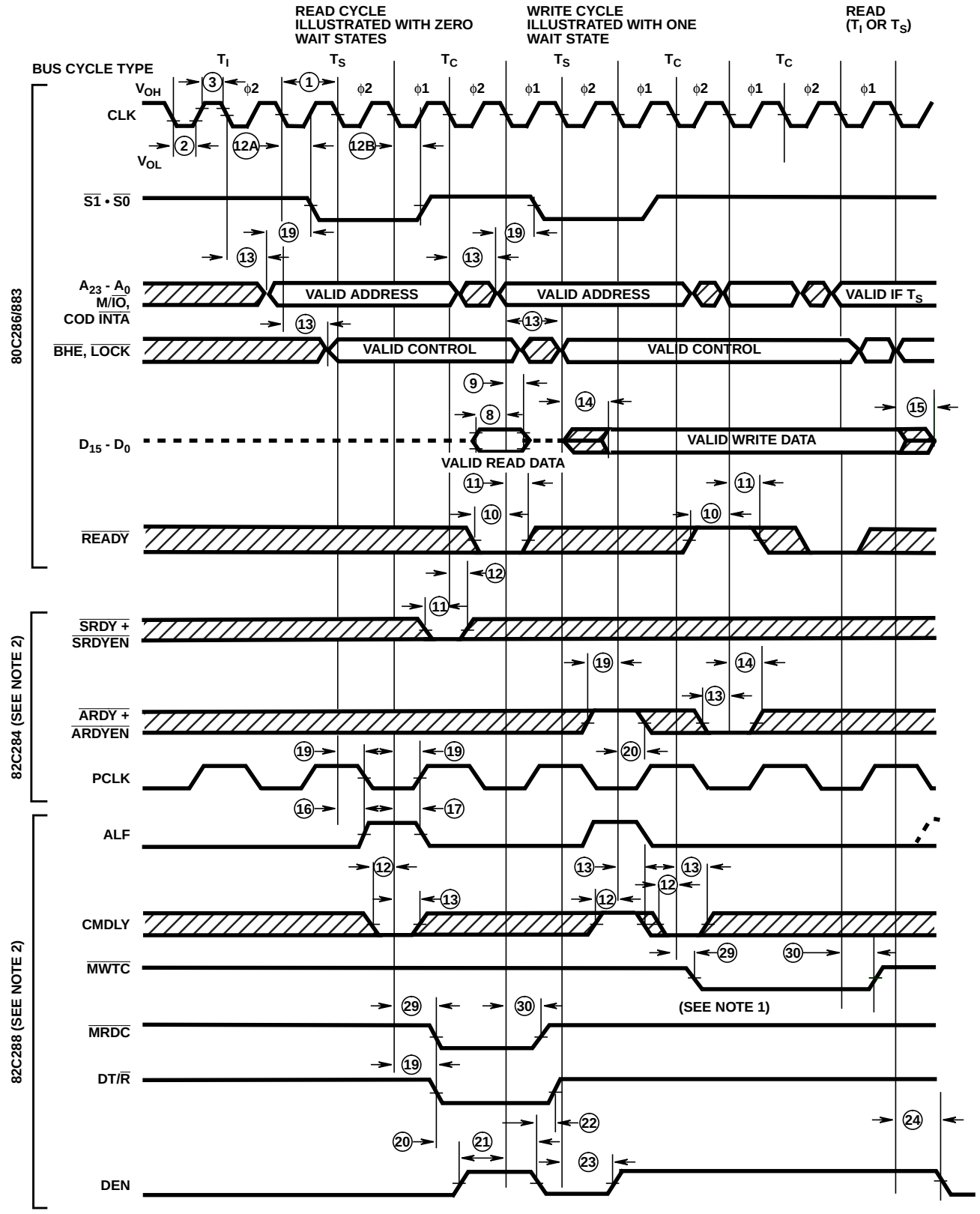


NOTE:

1. For AC testing, input rise and fall times are driven at 1ns per volt.

FIGURE 1. AC DRIVE AND MEASURE POINTS - CLK INPUT

Waveforms

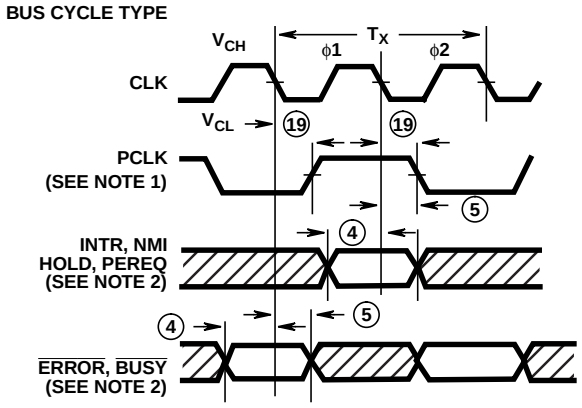


NOTES:

1. The modified timing is due to the CMDLY signal being active.
2. 82C254 and 82C288 Timing Waveforms are shown for reference only, and no guarantee is inplied.

FIGURE 2. MAJOR CYCLE TIMING

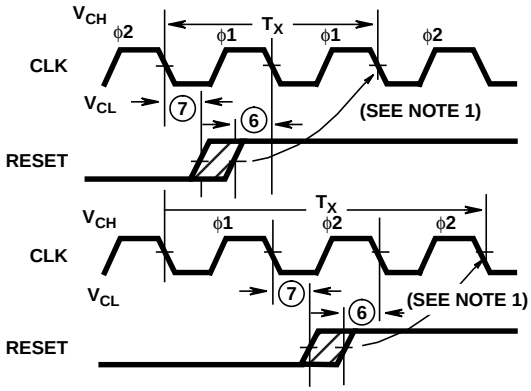
Waveforms (Continued)



NOTES:

1. PCLK indicates which processor cycle phase will occur on the next CLK. PCLK may not indicate the correct phase until the first cycle is performed.
2. These inputs are asynchronous. The setup and hold times shown assure recognition for testing purposes.

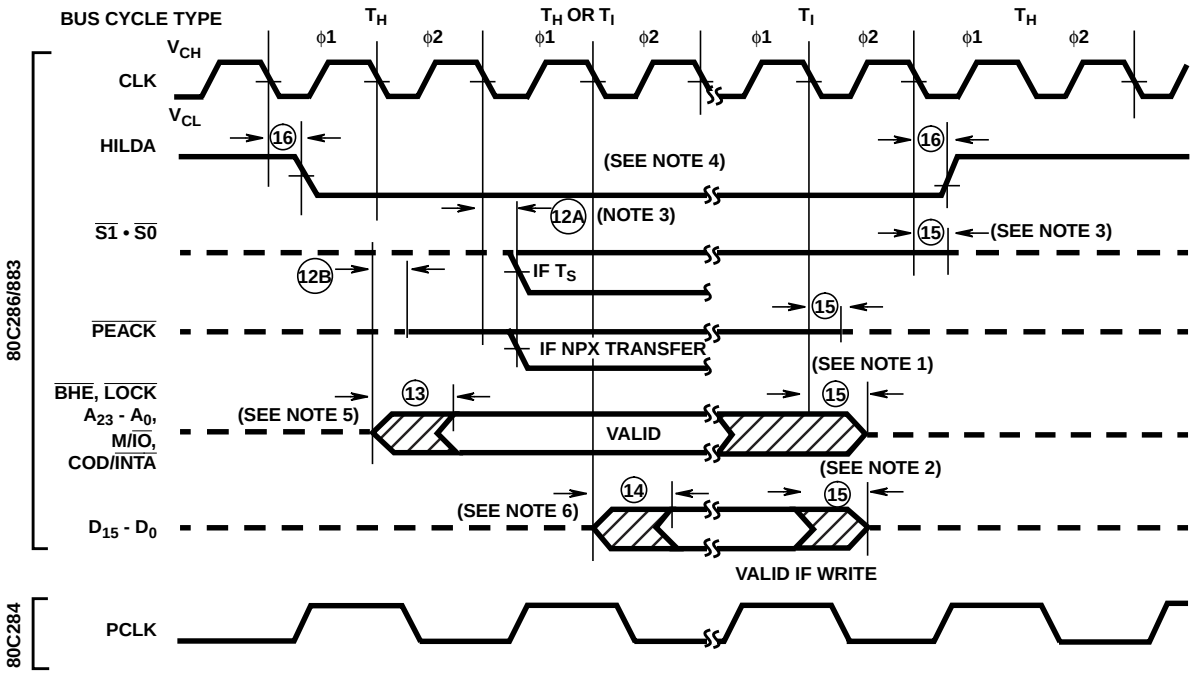
FIGURE 3. 80C286/883 ASYNCHRONOUS INPUT SIGNAL TIMING



NOTE:

1. When RESET meets the setup time shown, the next CLK will start or repeat $\phi1$ of a processor cycle.

FIGURE 4. 80C286/883 RESET INPUT TIMING AND SUBSEQUENT PROCESSOR CYCLE PHASE

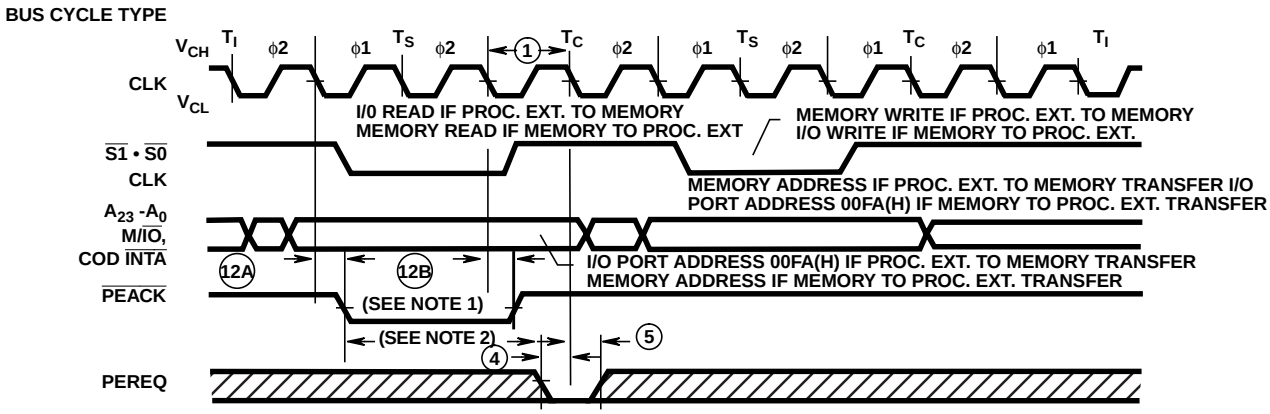


NOTES:

1. These signals may not be driven by the 80C286/883 during the time shown. The worst case in terms of latest float time is shown.
2. The data bus will be driven as shown if the last cycle before T_I in the diagram was a write T_C.
3. The 80C286/883 puts its status pins in a high impedance logic one state during T_H.
4. For HOLD request set up to HLDA, refer to Figure 8.
5. $\overline{BHE}$ and $\overline{LOCK}$ are driven at this time but will not become valid until T_S.
6. The data bus will remain in a high impedance state if a read cycle is performed.

FIGURE 5. EXITING AND ENTERING HOLD

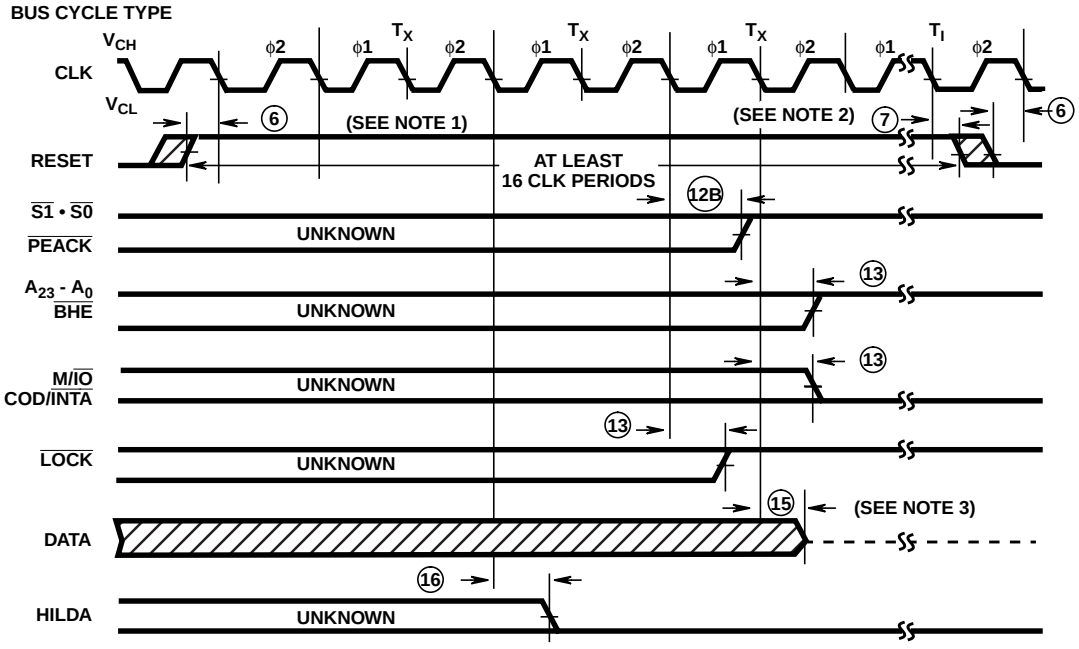
Waveforms (Continued)



NOTES:

1. $\overline{PEACK}$ always goes active during the first bus operation of a processor extension data operand transfer sequence. The first bus operation will be either a memory read at operand address or I/O read at port address 00FA(H).
2. To prevent a second processor extension data operand transfer, the worst case maximum time (shown above) is 3 x (1) - $12A_{MAX}$ -$(4)_{MIN}$ The actual, configuration dependent, maximum time is: 3 x (1) - $12A_{MAX}$ - $^{(4)}_{MIN}$ +N x 2 x $^{(1)}$. N is the number of extra T_C states added to either the first or second bus operation of the processor extension data operand transfer sequence.

FIGURE 6. 80C286/883 PEREQ/PEACK TIMING FOR ONE TRANSFER ONLY

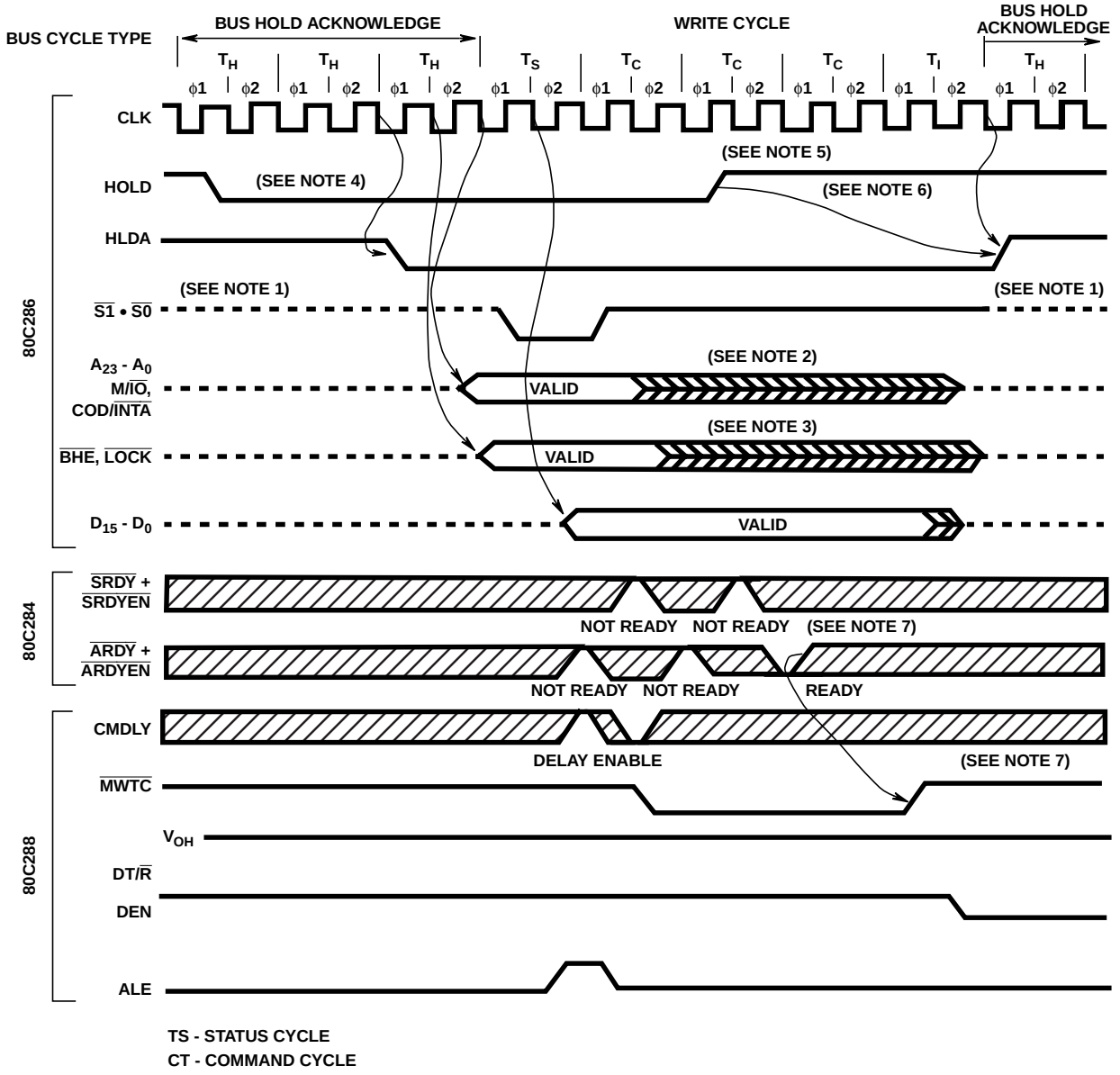


NOTES:

1. Setup time for RESET ↑ may be violated with the consideration that $\phi1$ of the processor clock may begin one system CLK period later.
2. Setup and hold times for RESET ↓ must be met for proper operation, but RESET ↓ may occur during $\phi1$ or $\phi2$.
3. The data bus is only guaranteed to be in a high impedance state at the time shown.

FIGURE 7. INITIAL 80C286/883 PIN STATE DURING RESET

Waveforms (Continued)

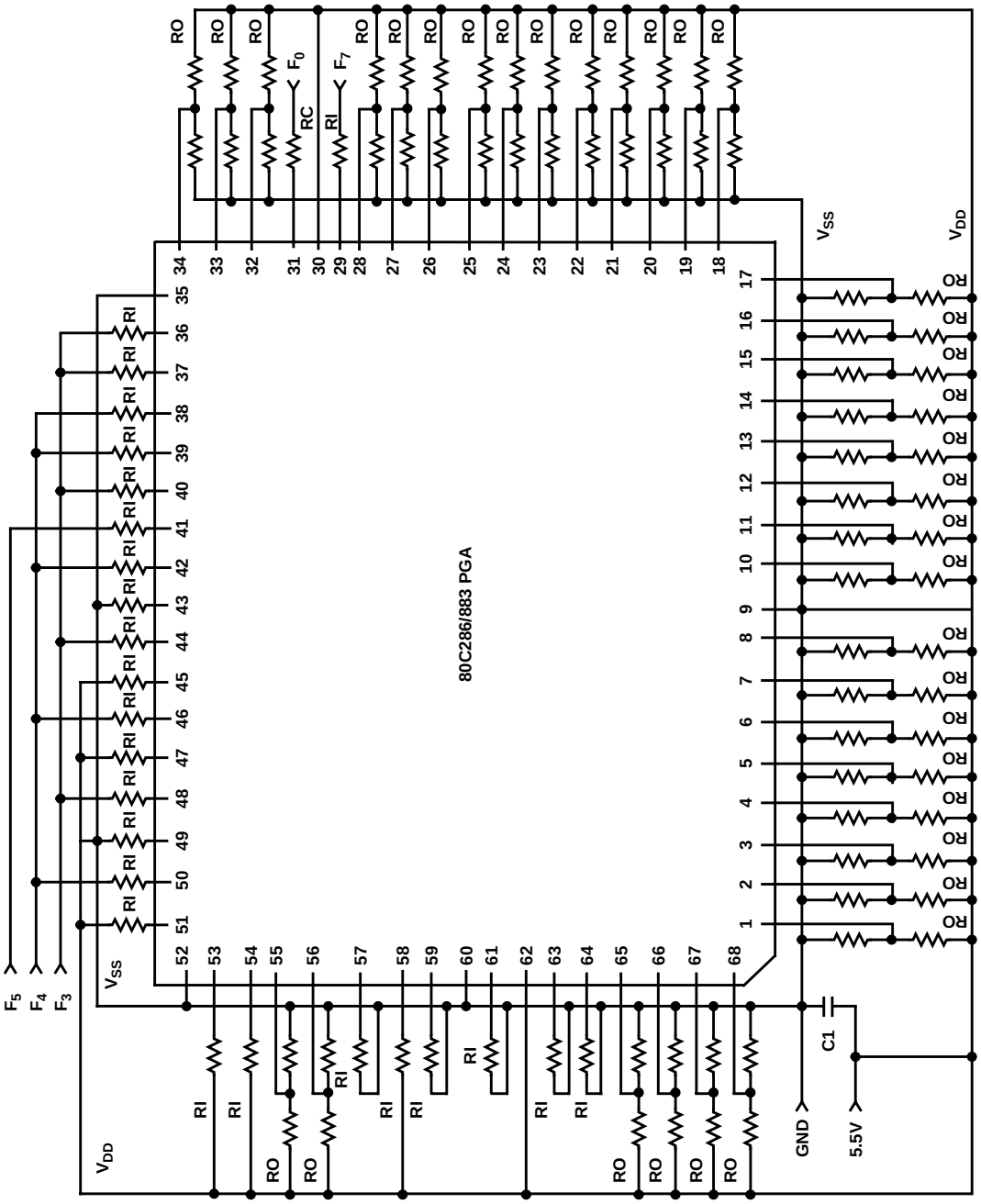


NOTES:

1. Status lines are held at a high impedance logic one by the 80C286 during a HOLD state.
2. Address, M/$\overline{IO}$ and COD/$\overline{INTA}$ may start floating during any T_C depending on when internal 80C286 bus arbiter decides to release bus to external HOLD. The float starts in $\phi 2$ of T_C.
3. $\overline{BHE}$ and $\overline{LOCK}$ may start floating after the end of any T_C depending on when internal 80C286 bus arbiter decides to release bus to external HOLD. The float starts in $\phi 1$ of T_C.
4. The minimum HOLD to HLDA time is shown. Maximum is one T_H longer.
5. The earliest HOLD time is shown. It will always allow a subsequent memory cycle if pending is shown.
6. The minimum HOLD to HLDA time is shown. Maximum is a function of the instruction, type of bus cycle and other machine state (i.e., Interrupts, Waits, Lock, etc.).
7. Asynchronous ready allows termination of the cycle. Synchronous ready does not signal ready in this example. Synchronous ready state is ignored after ready is signaled via the asynchronous input.

FIGURE 8. MULTIBUS WRITE TERMINATED BY ASYNCHRONOUS READY WITH BUS HOLD

Burn-In Circuit



NOTES:

8. Supply Voltage: V_{DD} = 5.5V, V_{SS} = 0.0V.
9. Input Voltage Limits: V_{IL} (Maximum) = 0.8V, V_{IH} (Minimum) = 2.0V
10. Component Values: RC = 1kΩ ±5%, RI = 10kΩ ±5%, RO = Two Series 2.7kΩ ±5%
11. Capacitor Values: C1 = 0.1 Microfarads
12. Oven Type and Frequency Requirements: Wakefield Oven Board f_0 = 100kHz, f_3 = 12.5kHz, f_4 = 6.25kHz, f_5 = 3.125kHz, f_7 = 781.25Hz.
13. Special Requirements: (a) ELECTROSTATIC DISCHARGE SENSITIVE. Proper Precautions Must be Used When Handling Units. (b) All Power Supplies Must be at Zero Volts When the Boards are Inserted into the Ovens. (c) When Powering Up, the Inputs Must be Held Below the V_{DD} Voltage. (d) If an Excessive Current is Indicated at Final Inspection, Check to See if a Part is Inserted Backwards or is Latched Up.

Die Characteristics

DIE DIMENSIONS:
286 x 283 x 19 ±1mils

METALLIZATION:
Type: Si-Al
Thickness: 8kÅ

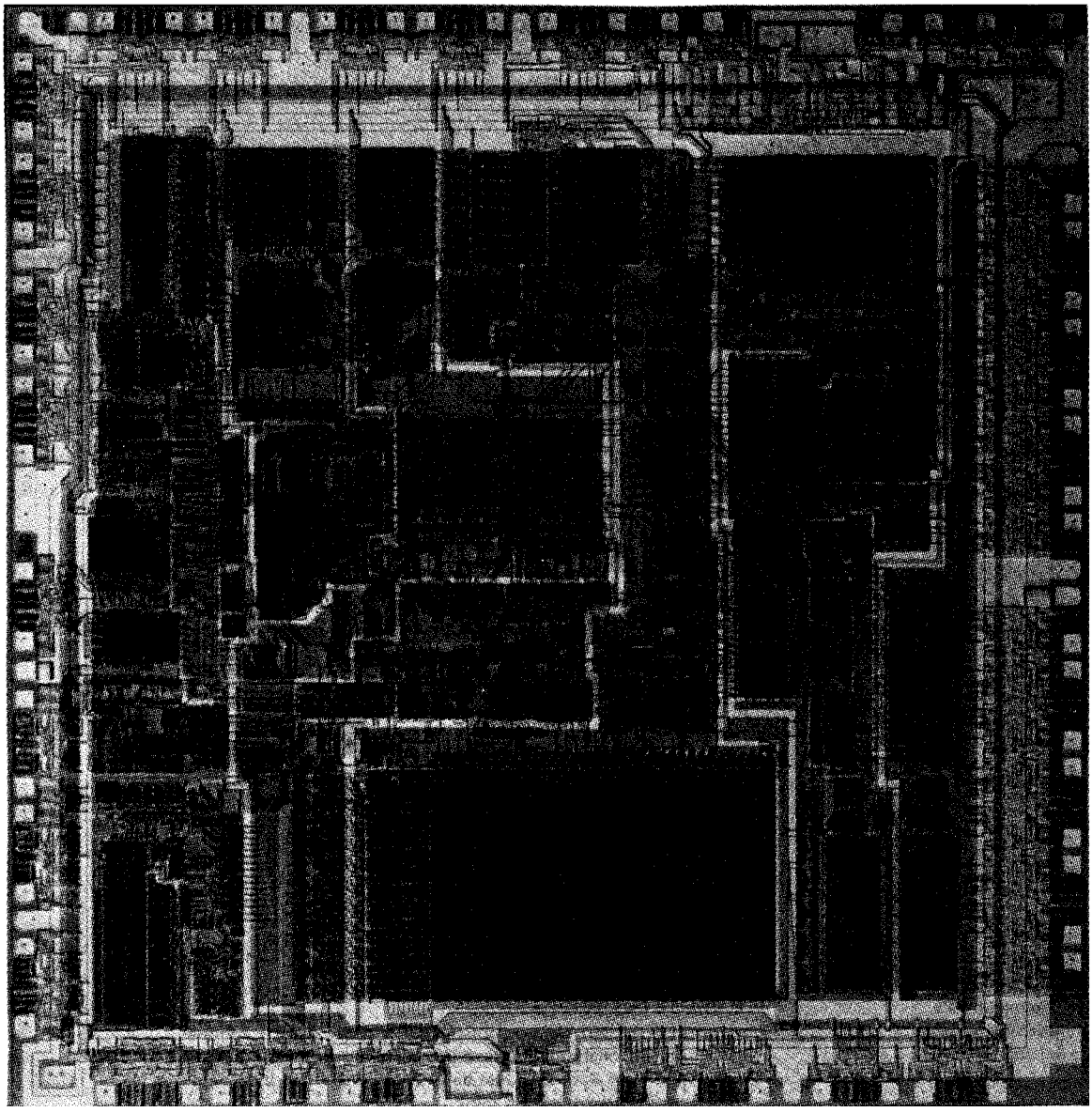
GLASSIVATION:
Type: Nitrox
Thickness: 10kÅ

WORST CASE CURRENT DENSITY: $2 \times 10^5 A/cm^2$

LEAD TEMPERATURE: (10s Soldering): $\leq 300^oC$

Metallization Mask Layout

80C286/883



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.