TOSHIBA

TC35821F 155 Mbps SONET/SDH ATM Framer

Features

- SONET STS-3c and STS-1/SDH STM-1
- 155.52Mbps PECL Serial Network Interface
- On-chip Clock Recovery
- Transmit Clock Synthesis
  – 19.44MHz to 155.52 MHz
- UTOPIA Level-1 & 2 Interface
- 144-pin PQFP
- 0.6 micron CMOS, 5 volts

Description

The TC35821F is a single-chip 155.52 Megabits per second (Mbps) framer chip for asynchronous transfer mode (ATM) physical layer application. It can be used for network interface card (NIC), switch and router applications.

The TC35821F offers cost-effective physical layer controller solutions. In NIC applications, an ATM framer chip used in conjunction with a transceiver on one side and a segmentation and reassembly (SAR) chip on the other provides a complete ATM solution. The interface to the SAR device is via the industry standard UTOPIA (Universal Test and Operations Physical Layer Interface for ATM) level one or two interface. Toshiba's TC35856F 155Mbps PCI-SAR and TC35853F 155 Mbps SAR are examples of SARs which can be used with the TC35821F.

The TC35821F supports SONET standards STS-1 and STS-3C. It contains a 155.52 megahertz (MHz) pseudo emitter coupled logic serial line interface to the transceiver chips. The device offers programmable section overhead (SOH)/ path overhead (POH) handling and operates internally at 19.44MHz/6.48MHz with a maximum 40 MHz cell-interface operation. The TC35821F is designed in 0.6 micron CMOS technology and operates on a single +5.0 volt power supply.

The TC35821F 155Mbps framer contains clock recovery circuits, byte alignment and frame synchronization, frame descrambling, frame overhead analysis, ATM cell synchronization, ATM cell header error correction and ATM cell payload descramble functions. Its transmit functions include ATM cell payload scramble, ATM header error correction (HEC) generation, frame overhead generation, frame assembly and frame scrambling. In addition, access to the chip registers from the central processing unit is available for configuration, status, diagnostics error counter and cell counter.

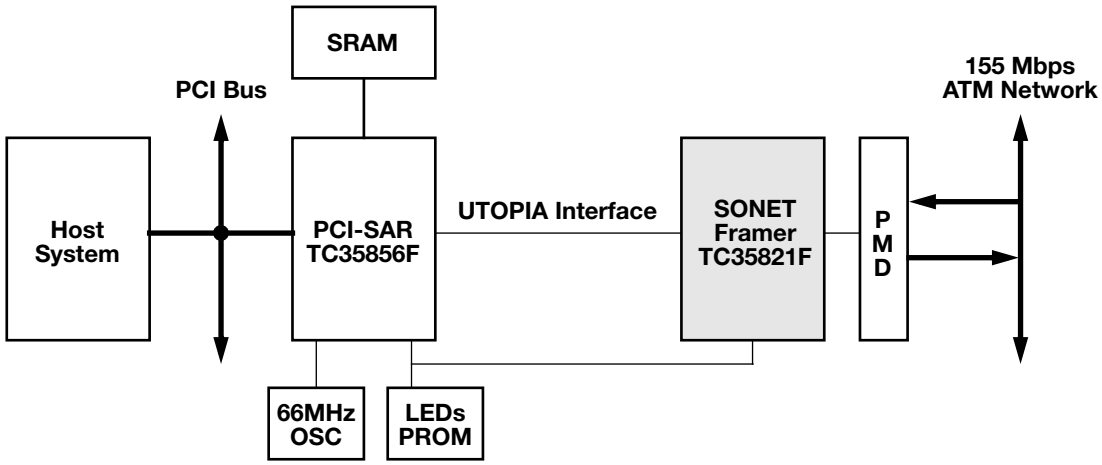

Figure 1. 155 Mbps System Block Diagram (Including SAR and Framer)

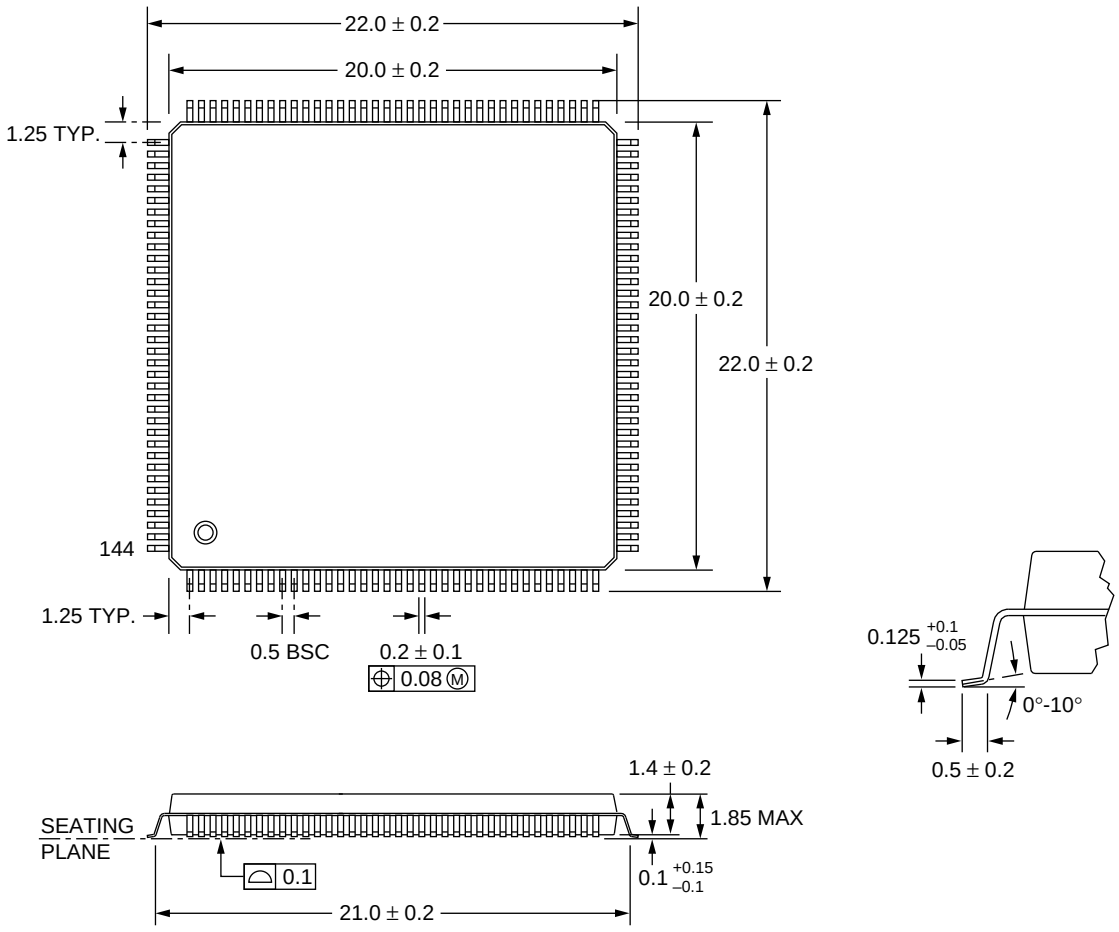

Figure 2. LQFP144-P-2020-0.50A [144-Pin LQFD (Thin Quad Flat Package – 1.4mm)] Unit: mm

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