HARRIS SEMICONDUCTOR

CDP68HC05J4

ADVANCE INFORMATION

March 1996

8-Bit Microcontroller Series

Features

The following are some of the hardware and software highlights of the CDP68HC05J4 family of HCMOS Microcomputers.

HARDWARE FEATURES

- **HCMOS Technology**
- **8-Bit Architecture**
- **Power-Saving STOP, WAIT, and Data Retention Modes**
- **Fully Static Operation**
- **On-Chip Memory**
  - **4,160 Bytes of ROM**
  - **176 Bytes of RAM**
- **14 Bidirectional I/O Lines**
  - **2 High Current Outputs (PC6 and PC7)**
  - **6 Interruptible Inputs (with Pull-Up Resistors) - Port A**
  - **Schmitt Trigger Inputs on Port A**
- **Internal 16-Bit Timer**
  - **1 Timer Capture**
  - **1 Timer Compare**
- **Interrupts - External, Port A, and Timer**
- **Master Reset and Power-On Reset**
- **On-Chip Oscillator with RC or Crystal Mask Options**
- **CDP68HC05J4**
  - **4.2MHz Operating Frequency (2.1MHz Internal Bus Frequency) at 5V; 2MHz at 3.0V**
  - **Single 3.0V to 6.0V Supply (2.0V Data Retention)**
- **CDP68HCL05J4**
  - **Lower Supply Current, I_{DD}, In RUN, WAIT and STOP Modes at 5.5V, 3.3V and 2.4V**
  - **Single 2.4V to 6.0V Supply (2.0V Data Retention)**
- **CDP68HSC05J4**
  - **8.0MHz Operating Frequency (4.0MHz Internal Bus Frequency) at 5.0V; 4.2MHz at 3.3V**
  - **Single 3.0V to 6.0V Supply (2.0V Data Retention)**
- **20 Lead or 28 Lead Dual-In-Line or Small Outline Packages**

SOFTWARE FEATURES

- **Supports Full CDP68HC05 Instruction Set**
- **8 x 8 Unsigned Multiply Instruction**
- **True Bit-Manipulation**
- **Two Power Saving Standby Modes**
- **Efficient Use of Program Space**
- **Memory Mapped I/O**

Description

The CDP68HC05J4 HCMOS Microcomputer is a member of the CDP68HC05 family of single chip microcomputers. This 8-bit microcomputer unit (MCU) contains a CPU, 176 bytes of RAM, 4,160 bytes of masked ROM, a flexible 16-bit timer, 14 bidirectional I/O lines (two high current outputs and six programmable as interruptible inputs), and an on-chip oscillator. The fully static design allows operation at frequencies down to DC, further reducing the already low power consumption.

As a mask programming option the six Port A lines can individually be “wire OR’ed” with the IRQ interrupt to provide an additional source for interrupts. The mask option also includes the addition of pull-up resistors at Port A input pads. Therefore, Port A inputs combined with outputs from Port C can provide a convenient means for switch scanning. For improved noise immunity, Schmitt trigger action is provided on all Port A inputs.

A Port A interrupt (active low) can also be used to exit the power down modes.

Timer capture (TCAP) and timer compare (TCMP) functions are available as mask programmable options at PC0 and PC1 respectively.

Two high current, 15mA, sink outputs are available at PC6 and PC7.

The CDP68HCL05J4 MCU device is a low power version of the CDP68HC05J4 with low power consumption in the RUN, WAIT, and STOP modes; and low voltage operation down to 2.4V.

The CDP68HSC05J4 MCU device is a high-speed version of the CDP68HC05J4 with up to 8.0MHz operation.

The CDP68HC05J4 family supports the full CDP68HC05 instruction set. Development can be performed with tools supplied by Harris or offered by numerous third party vendors. Available tools include assemblers and C compilers.

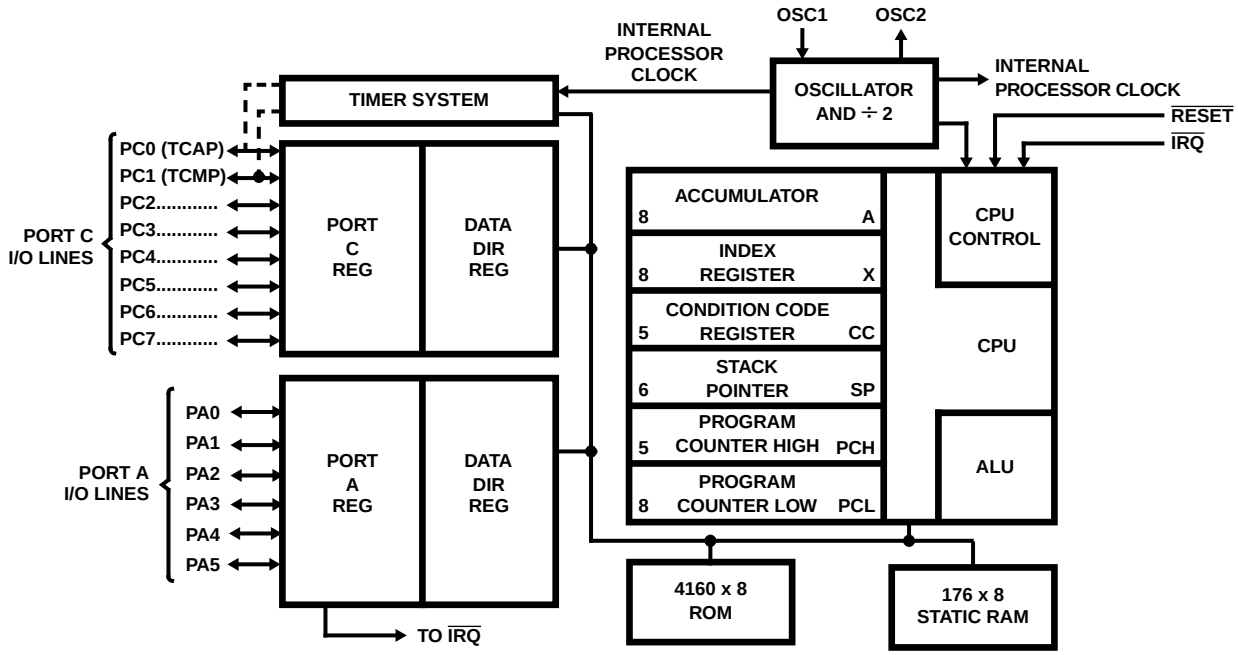
Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
CDP68HC05J4E20	-40 to +85	20 Ld PDIP	E20.3
CDP68HC05J4M20	-40 to +85	20 Ld SOIC	M20.3
CDP68HC05J4E28	-40 to +85	28 Ld PDIP	E28.6
CDP68HC05J4M28	-40 to +85	28 Ld SOIC	M28.3

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

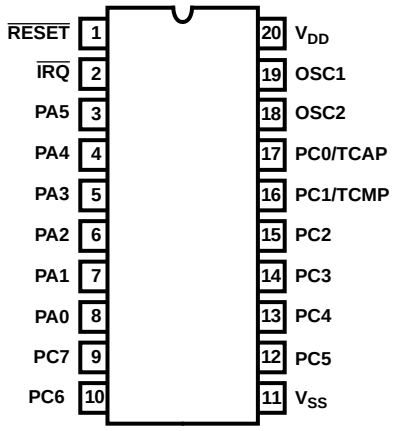
File Number **4058**

Block Diagram

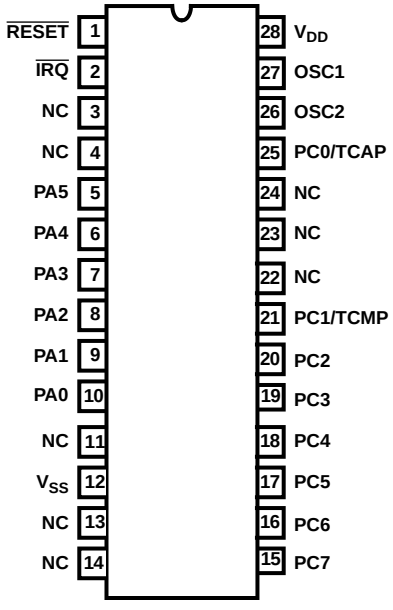


Pinouts

CDP68HC05J4 20 LEAD (SOIC, PDIP)
TOP VIEW



CDP68HC05J4 28 LEAD (SOIC, PDIP)
TOP VIEW



NC - No Connection to the IC

Absolute Maximum Ratings

Supply Voltage (V_{DD}) . . . . . -0.5V to +7.0V
Input Voltage (V_{IN}) . . . . . V_{SS} -0.3V to V_{DD} +0.3V
Self-Check Mode (V_{IN})
$\overline{IRQ}$ Pin Only . . . . . V_{SS} -0.3V to 2 x V_{DD} +0.3V
Current Drain Per Pin (I)
Excluding V_{DD} and V_{SS} 40mA

Thermal Information

Thermal Resistance (Typical) ^{o}C/W θ_{JA}
20 Ld PDIP . . . . . 75^{o}C/W
28 Ld PDIP . . . . . 60^{o}C/W
20 Ld SOIC . . . . . 110^{o}C/W
28 Ld SOIC . . . . . 75^{o}C/W
Maximum Junction Temperature . . . . . +150^{o}C
Storage Temperature Range (T_{STG}) . . . . . -65^{o}C to +150^{o}C
Lead Temperature (Soldering 10s) . . . . . +300^{o}C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range (T_A) . . . . . -40^{o}C to +85^{o}C
Operating Voltage Range . . . . . .2.0V to 6.0V
Input High Voltage . . . . . .(0.8•V_{DD}) to V_{DD}

DC Electrical Specifications

V_{DD} = 3.3V ±10%, V_{SS} = 0V, T_A = 0^{o}C to +70^{o}C, Unless Otherwise Specified

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	V_{OL}	I_{LOAD} ≤10µA	-	-	0.1	V
	V_{OH}		V_{DD} -0.1	-	-	V
Output High Voltage: PA0-5, PC0-5	V_{OH}	I_{LOAD} = -0.2mA	V_{DD} -0.3	-	-	V
Output Low Voltage: PA0-5, PC0-5	V_{OL}	I_{LOAD} = 0.4mA	-	-	0.3	V
Output High Voltage: PC6-7	V_{OH}	I_{LOAD} = -2.0mA	V_{DD} -0.3	-	-	V
Output Low Voltage: PC6-7	V_{OL}	I_{LOAD} = 6mA	-	-	0.3	V
Input High Voltage: PA0-5	V_{IH}		TBD	1.75	-	V
Input High Voltage: PC0-7	V_{IH}		0.7•V_{DD}	-	V_{DD}	V
Input High Voltage: $\overline{RESET}$, $\overline{IRQ}$, OSC1, TCAP,	V_{IH}		0.8•V_{DD}	-	V_{DD}	V
Input Low Voltage: PA0-5	V_{IL}		V_{SS}	1.25	TBD	V
Input Low Voltage: PC0-7	V_{IL}		V_{SS}	-	0.2•V_{DD}	V
Input Low Voltage: $\overline{RESET}$, $\overline{IRQ}$, OSC1, TCAP	V_{IL}		V_{SS}	-	0.3•V_{DD}	V
Input Source Current: PA0-5 Interrupts	I_{IH}	$V_{IN} \leq V_{IL}$ (Port A)	TBD	-	TBD	µA
		$V_{IN} \geq V_{IH}$ (Port A)	TBD	-	TBD	µA
Input Hysteresis Voltage: PA0-5	V_{HYS}		-	0.5	-	V
Input Hysteresis Voltage: $\overline{RESET}$, $\overline{IRQ}$, OSC1, TCAP	V_{HYS}		0.1•V_{DD}	1.0	0.5•V_{DD}	V
Data Retention Voltage	VRM		2	-	-	V
Supply Current (Notes 1, 2)						
RUN	I_{RUN}	f_{OSC} = 2.0MHz External Square Wave	-	1.2	2.4	mA
WAIT	I_{WAIT}		-	0.5	1.0	mA
STOP	I_{STOP}	T_A = 25^{o}C	-	10	20	µA
I/O Ports Hi-Z Leakage Current: PA0-5, PC0-7	I_{IL}		-	-	±10	µA
Input Current: $\overline{RESET}$, $\overline{IRQ}$, OSC1	I_{IN}		-	-	±1	µA
Capacitance: (Note 2)	C_{OUT}		-	-	12	pF
$\overline{RESET}$, $\overline{IRQ}$, OSC1	C_{IN}		-	-	8	pF

NOTES:

1. This device contains circuitry to protect the inputs against damage due to high static voltages of electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to the range $V_{SS} < (V_{IN}$ or $V_{OUT}) < V_{DD}$. Reliability of operation is enhanced if unused inputs except OSC2 are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).
2. Includes Ports used as Input/Output Pins; Ports used as Input only Pins; Ports used as Output only Pins.

Control Timing V_{DD} = 3.3V ±10%, V_{SS} = 0V, T_A = 0°C to +70°C Unless Otherwise Specified

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Of Operation						
Crystal Option	f_{OSC}		-	-	2.0	MHz
External Clock Option	f_{OSC}		DC	-	2.0	MHz
Internal Operating Frequency						
Crystal (f_{OSC} + 2)	f_{OP}		-	-	1.0	MHz
External Clock (f_{OSC} + 2)	f_{OP}		DC	-	1.0	MHz
Cycle Time	t_{CYC}		1000	-	-	ns
Crystal Oscillator Start-Up Time for AT-Cut Crystal	t_{OXOV}		-	-	100	ms
Stop Recovery Start-Up Time (AT-Cut Crystal Oscillator)	t_{ILCH}		-	-	100	ms
$\overline{\text{RESET}}$ Pulse Width	t_{RL}		1.5	-	-	t_{CYC}
Timer						
Resolution (Note 1)	t_{RES}		4.0	-	-	t_{CYC}
Input Capture Pulse Width	t_{TH}, t_{TL}		250	-	-	ns
Input Capture Pulse Period	t_{TLTL}		(Note 2)			t_{CYC}
Interrupt Pulse Width Low (Edge-Triggered)	t_{ILIH}		250	-	-	ns
Interrupt Pulse Period	t_{ILIH}		(Note 3)	-	-	t_{CYC}
OSC1 Pulse Width	t_{OH}, t_{OL}		200	-	-	ns

NOTES:

1. Since a 2-bit prescaler in the timer must count four internal cycles (t_{CYC}), this is the limiting minimum factor in determining the timer resolution.
2. The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{CYC}.
3. The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{CYC}.

DC Electrical Specifications V_{DD} = 5.0V ±10%, V_{SS} = 0V, T_A = 0°C to +70°C, Unless Otherwise Specified

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	V_{OL}	$I_{LOAD} \le 10\mu A$	-	-	0.1	V
	V_{OH}		V_{DD} -0.1	-	-	V
Output High Voltage: PA0-5, PC0-5	V_{OH}	I_{LOAD} = -0.8mA	V_{DD} -0.8	-	-	V
Output Low Voltage: PA0-5, PC0-5	V_{OL}	I_{LOAD} = 1.6mA	-	-	0.4	V
Output High Voltage: PC6-7	V_{OH}	I_{LOAD} = -5.0mA	V_{DD} -0.8	-	-	V
Output Low Voltage: PC6-7	V_{OL}	I_{LOAD} = 15mA	-	-	0.4	V
Input High Voltage: PA0-5	V_{IH}		TBD	2.75	-	V
Input High Voltage: PC0-7	V_{IH}		0.7•V_{DD}	0.5•V_{DD}	V_{DD}	V
Input High Voltage: $\overline{\text{RESET}}$, $\overline{\text{IRQ}}$, OSC1, TCAP	V_{IH}		0.8•V_{DD}	0.5•V_{DD}	V_{DD}	V
Input Low Voltage: PA0-5	V_{IL}		-	2.25	TBD	V
Input Low Voltage: PC0-7	V_{IL}		V_{SS}	0.5•V_{DD}	0.3•V_{DD}	V
Input Low Voltage: $\overline{\text{RESET}}$, $\overline{\text{IRQ}}$, OSC1, TCAP, PA0-5	V_{IL}		V_{SS}	-	0.2•V_{DD}	V
Input Source Current: PA0-5 Interrupts	I_{IH}	$V_{IN} \le V_{IL}$ (Port A)	TBD	-	TBD	µA
		$V_{IN} \ge V_{IH}$ (Port A)	TBD	-	TBD	µA

DC Electrical Specifications

V_{DD} = 5.0V ±10%, V_{SS} = 0V, T_A = 0°C to +70°C, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Hysteresis Voltage: PA0-5	V_{HYS}		-	0.5	-	V
Input Hysteresis Voltage: $\overline{RESET}$, $\overline{IRQ}$, OSC1, TCAP	V_{HYS}		0.1•V_{DD}	1.0	0.5•V_{DD}	V
Data Retention Voltage	V_{RM}		2	-	-	V
Supply Current (Notes 1, 2)						
RUN	I_{RUN}	f_{OSC} = 4.0MHz External Square Wave	-	2.0	4.0	mA
WAIT	I_{WAIT}		-	0.8	1.6	mA
STOP	I_{STOP}	T_A = 25°C	-	20	40	µA
I/O Ports Hi-Z Leakage Current: PA0-5, PC0-7	I_{IL}		-	-	±10	µA
Input Current: $\overline{RESET}$, $\overline{IRQ}$, OSC1	I_{IN}		-	-	±1	µA
Capacitance: (Note 2)	C_{OUT}		-	-	12	pF
$\overline{RESET}$, $\overline{IRQ}$, OSC1	C_{IN}		-	-	8	pF

NOTES:

1. This device contains circuitry to protect the inputs against damage due to high static voltages of electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to the range $V_{SS} < (V_{IN}$ or $V_{OUT}) < V_{DD}$. Reliability of operation is enhanced if unused inputs except OSC2 are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).
2. Includes Ports used as Input/Output Pins; Ports used as Input only Pins; Ports used as Output only Pins.

Control Timing

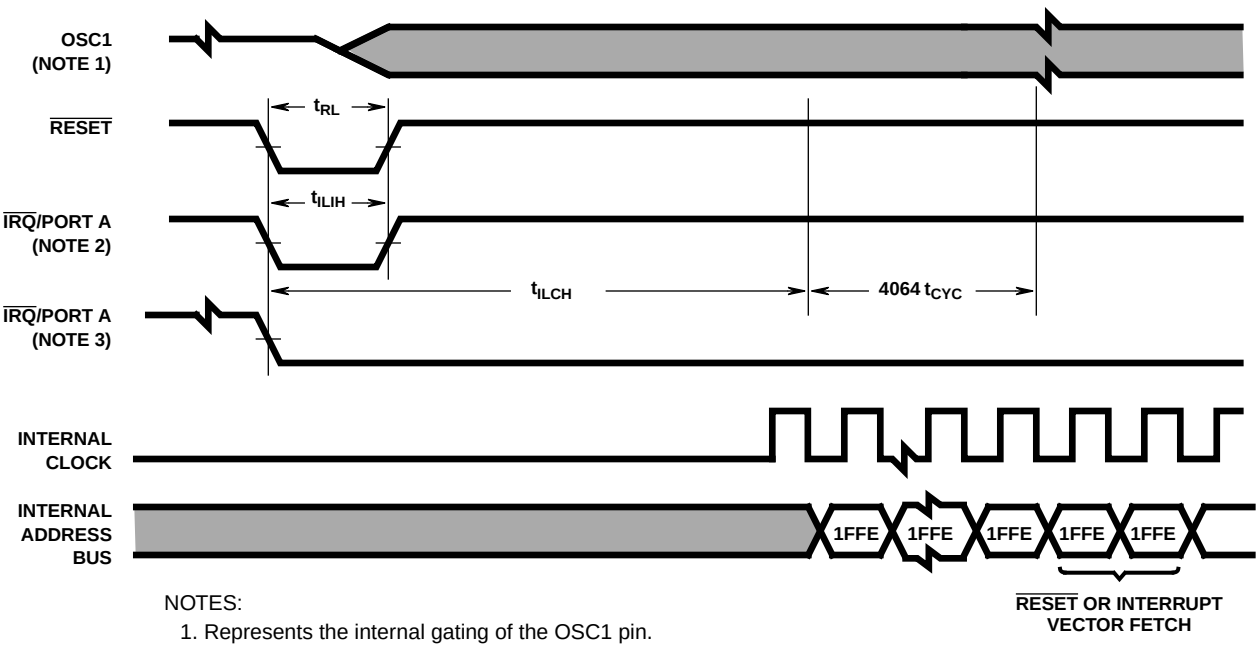
V_{DD} = 5.0V ±10%, V_{SS} = 0V, T_A = 0°C to +70°C Unless Otherwise Specified

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Of Operation						
Crystal Option	f_{OSC}		-	-	4.2	MHz
External Clock Option	f_{OSC}		DC	-	4.2	MHz
Internal Operating Frequency						
Crystal (f_{OSC} + 2)	f_{OP}		-	-	2.1	MHz
External Clock (f_{OSC} + 2)	f_{OP}		DC	-	2.1	MHz
Cycle Time	t_{CYC}		480	-	-	ns
Crystal Oscillator Start-Up Time for AT-Cut Crystal	t_{OXOV}		-	-	100	ms
Stop Recovery Start-Up Time (AT-Cut Crystal Oscillator)	t_{ILCH}		-	-	100	ms
$\overline{RESET}$ Pulse Width	t_{RL}		1.5	-	-	t_{CYC}
Timer						
Resolution (Note 1)	t_{RES}		4.0	-	-	t_{CYC}
Input Capture Pulse Width	t_{TH}, t_{TL}		125	-	-	ns
Input Capture Pulse Period	t_{TLTL}		(Note 2)	-	-	t_{CYC}
Interrupt Pulse Width Low (Edge-Triggered)	t_{ILIH}		250	-	-	ns
Interrupt Pulse Period	t_{ILIH}		(Note 3)	-	-	t_{CYC}
OSC1 Pulse Width	t_{OH}, t_{OL}		90	-	-	ns

NOTES:

1. Since a 2-bit prescaler in the timer must count four internal cycles (t_{CYC}), this is the limiting minimum factor in determining the timer resolution.
2. The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{CYC}.
3. The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{CYC}.

Control Timing Diagrams



NOTES:

1. Represents the internal gating of the OSC1 pin.
2. $\overline{IRQ}$/PORT A pin edge-sensitive mask option.
3. $\overline{IRQ}$/PORT A pin level and edge-sensitive mask option.

FIGURE 1. STOP RECOVERY TIMING DIAGRAM

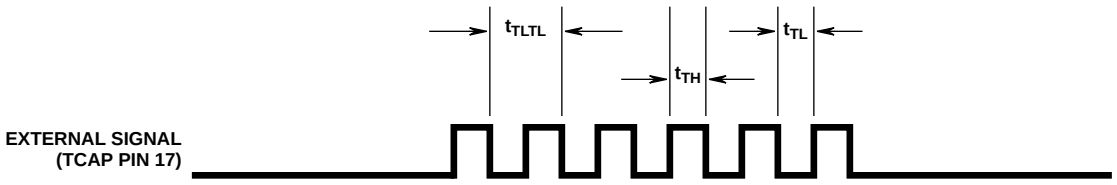


FIGURE 2. TIMER RELATIONSHIPS

Functional Pin Description, Input/Output Programming, Memory, and CPU Registers

This section provides a description of the functional pins, input/output programming, memory, CPU registers, and self-check features of the CDP68HC05J4. Pin references throughout this data sheet refer to the 20 lead version of the CDP68HC05J4 MCU.

FUNCTIONAL PIN DESCRIPTION

V_{DD} and V_{SS}

Power is supplied to the MCU using these two pins. V_{DD} is a positive voltage with respect to V_{SS} (ground).

$\overline{IRQ}$ / Port A (Maskable Interrupt Request)

As a mask programmable option two different choices of interrupt triggering sensitivity are available. These options are:

1. Negative edge-sensitive triggering only, or
2. Both negative edge-sensitive and level-sensitive triggering.

In the latter case, either type of input to the $\overline{IRQ}$ or Port A pin will produce an interrupt. The MCU completes the current instruction before it responds to the interrupt request. When the $\overline{IRQ}$ or Port A pin goes low for at least one t_{ILIH}, a logic one is latched internally to signify an interrupt has been requested. When the MCU completes its current instruction, the interrupt latch is tested. If the interrupt latch contains a logic one, and the interrupt mask bit (I-bit) in the condition code register is clear, the MCU then begins the interrupt sequence.

Schmitt trigger action is provided on the $\overline{IRQ}$ and Port A inputs pins to improve noise immunity.

If the option is selected to include level-sensitive triggering, then the $\overline{IRQ}$ input can be connected to V_{DD} via an external resistor to permit “wire ORed” operation. See INTERRUPTS for more detail concerning external interrupts and Input/Output Programming for description of Port A functions in this mode.

$\overline{RESET}$

The $\overline{RESET}$ input is not required for start-up but can be used to reset the MCU internal state and provide an orderly software start-up procedure. Refer to RESETS for a detailed description.

TCAP

TCAP input is available as a mask option at PC0 terminal. The TCAP input controls the input capture feature for the on-chip programmable timer system. PC0 functions are not disturbed by this option. Refer to Input Capture Register for additional information and Input/Output Programming for description of PC0 functions in this mode.

TCMP

TCMP output is available as a mask option at PC1 terminal. The TCMP pin provides an output for the output compare feature of the on-chip timer system. PC1 functions are not disturbed by this option. However, to avoid possible contention, the output from the PC1 data latch is disconnected from the terminal. Refer to Output Compare Register for additional information and Input/Output Programming for description of PC1 functions in this mode.

OSC1, OSC2

The CDP68HC05J4 family of MCUs can be configured, during device manufacturing, to accept either a crystal or an RC network to control the internal oscillator. The internal clocks are derived by a divide-by-two of the external oscillator frequency (f_{OSC}).

Crystal

The circuit shown in Figure 3C is recommended when using a crystal. The internal oscillator is designed to interface with an AT-Cut parallel resonant quartz crystal resonator in the frequency range specified for f_{OSC} in Control Timing. Use of an external CMOS oscillator is recommended when crystals outside the specified ranges are to be used. The crystal and components should be mounted as close as possible to the input pins to minimize output distortion and start-up stabilization time. Refer to Electrical Specifications for V_{DD} specifications.

	2MHz	4MHz	UNITS
R_S (Max)	400	75	Ω
C_0	5	7	pF
C_1	0.008	0.012	pF
C_{OSC1}	15-40	15-30	pF
C_{OSC2}	15-30	15-25	pF
R_P	10	10	MΩ
Q	30	40	K

FIGURE 3A. CRYSTAL RESONATOR PARAMETERS

Ceramic Resonator

A ceramic resonator may be used in place of the crystal in cost sensitive applications. The circuit in Figure 3C is recommended when using a ceramic resonator. Figure 3B lists the recommended capacitance and feedback resistance values. The manufacturer of the particular ceramic resonator being considered should be consulted for specific information.

	2MHz - 4MHz	UNITS
R_S (Typical)	10	Ω
C_0	40	pF
C_1	4.3	pF
C_{OSC1}	30	pF
C_{OSC2}	30	pF
R_P	1-10	MΩ
Q	1250	-

FIGURE 3B. CERAMIC RESONATOR PARAMETERS

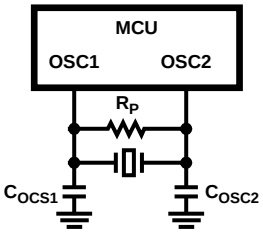


FIGURE 3C. CRYSTAL OSCILLATOR CONNECTIONS

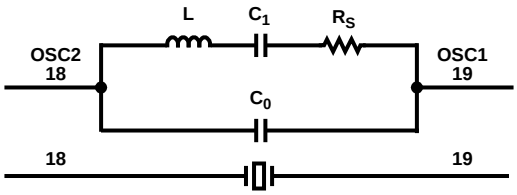


FIGURE 3D. EQUIVALENT CRYSTAL CIRCUIT

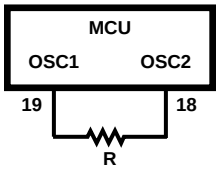


FIGURE 3E. RC OSCILLATOR CONNECTIONS

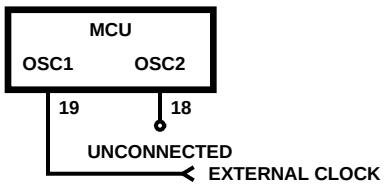


FIGURE 3F. EXTERNAL CLOCK SOURCE CONNECTIONS

FIGURE 3. OSCILLATOR CONNECTIONS

RC

If the RC oscillator option is selected, then a resistor is connected to the oscillator pins as shown in Figure 3E.

External Clock

An external clock should be applied to the OSC1 input with the OSC2 output not connected, as shown in Figure 3F. An external clock may be used with either the RC or crystal oscillator option. The t_{OXOV} or t_{ILCH} specifications do not apply when using an external clock input. The equivalent specification of the external clock source should be used in lieu of t_{OXOV} or t_{ILCH}.

PA0-PA5

These six I/O lines comprise Port A. The function of any pin is software programmable to be an input or an output. For improved noise immunity Schmitt trigger action is provided on all Port A inputs. Additionally, as a mask option, each pin's input signal can functionally be wire OR'ed with the IRQ interrupt input. The mask option also includes the addition of pull-up resistors at the input terminal. All Port A lines are configured as inputs during power-on or reset. Refer to Input/Output Programming for a detailed description of I/O programming.

PC0-PC7

These eight lines comprise Port C. The function of any pin is software programmable to be an input or an output. All Port C lines are configured as inputs during power-on or reset. PC6 and PC7 are higher current outputs. Refer to Input/Output Programming for a more detailed description of I/O programming.

INPUT/OUTPUT PROGRAMMING

Parallel Ports

The 14 I/O lines associated with ports A and C may be individually programmed as inputs or as outputs. The direction of each pin is determined by the state of the corresponding bit in the port data direction register (DDR). A port pin is configured as an output if its corresponding DDR bit is set to a logic one. A pin is configured as an input if its corresponding DDR bit is cleared to a logic zero. At power-on or RESET, all DDRs are cleared, which configures all port pins as inputs. The data direction registers are capable of being written to or read by the processor. Refer to Table 1. During the programmed output state, a read of the data register actually reads the value of the output latch and not the I/O pin. As an example, if a port bit is set to be a high output and it is pulled low by an external load, reading the port will provide a high reading for that bit.

TABLE 1. PORT A TRUTH TABLE

(NOTE 1) R/$\overline{W}$	DDR	I/O PIN FUNCTION
0	0	The I/O pin is in input mode. Data is written into the output data latch
0	1	Data is written into the output data latch and output to the I/O pin.
1	0	The state of the I/O pin is read.
1	1	The I/O pin is in output mode. The output data latch is read.

NOTE:

1. R/$\overline{W}$ is an internal signal.

Port A0-A5

The Port A Data Register (PORTA) is located at $0000 and the Port A Data Direction Register (DDRA) is located at $0004. In addition to data direction control provided by DDRA, Port A I/O pins can be mask programmed, individually, to generate an IRQ interrupt if the input signal is in the low state. Refer to Figure 4A for an illustration of a typical Port A bit. See INTERRUPTS for more information on operation of Port A interrupts.

All bits in DDRA are cleared by power-on and RESET. Bits in PORTA are unaffected by power-on and RESET. All unused bits in the Port A registers are read as 0's.

Port C0-C7

The Port C Data Register (PORTC) is located at $0002 and the Port C Data Direction Register (DDRC) is located at $0006.

As a mask programmable option terminals PC0 and PC1 can be connected to TCAP and TCMP. This has the following effects:

1. When PC0 is connected to TCAP its functions are not disabled and can be used to generate a TCAP input if DDRC bit 0 is set. Refer to Figure 4B.
2. When PC1 is connected to TCMP, the output from the Port C1 data latch will not be available at the terminal regardless of the state of its DDR. A Read of port C1 will provide the state of the I/O terminal (TCMP) if DDR C1 = 0 and the state of its data latch if DDR C1 = 1. Refer to Figure 4C.

The Port C DR is unaffected by powerup and RESET.

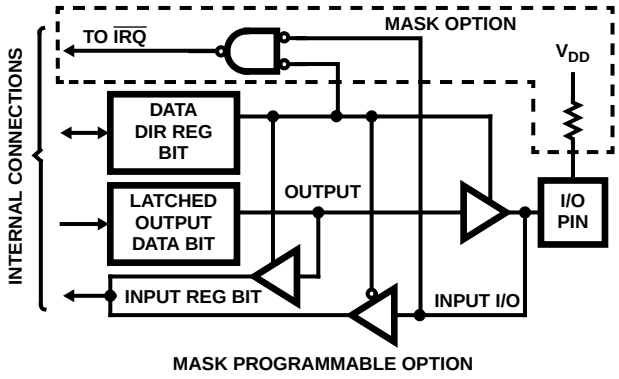


FIGURE 4A. PORT A CONFIGURATION

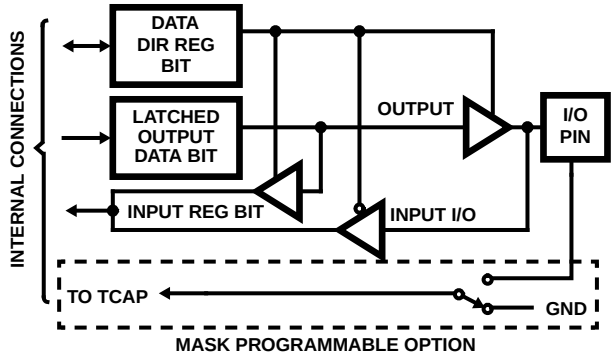


FIGURE 4B. PORT C0 CONFIGURATION

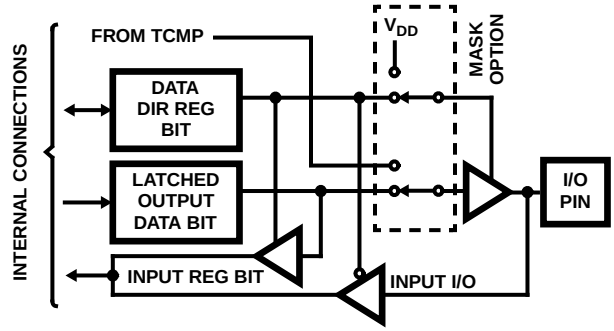


FIGURE 4C. PORT C1 CONFIGURATION

FIGURE 4.

MEMORY

Figure 5 illustrates the address map of the J4. As shown, the memory consists of 176 bytes of RAM between $0050 and $00FF. The upper 64 bytes of RAM is used for a system stack which grows from higher addresses towards lower addresses. Locations $0100 through $10FF contain 4096 bytes of ROM for user code.

CPU REGISTER MODEL

The CPU contains five registers, as shown in the programing model of Figure 6. The interrupt stacking order is shown in Figure 7.

NOTE: Since the Stack Pointer decrements during pushes, the PCL is stacked first, followed by PCH, etc. Pulling from the stack is in the reverse order.

Accumulator (A)

The accumulator is an 8-bit general purpose register used to hold operands, results of the arithmetic calculations, and data manipulations.

Index Register (X)

The X register is an 8-bit register which is used during the indexed modes of addressing. It provides an 8-bit value which is used to create an effective address. The index register is also used for data manipulations with the read-modify-write type of instructions and as a temporary storage register when not performing addressing operations.

Program Counter (PC)

The program counter is a 13-bit register that contains the address of the next instruction to be executed by the processor.

Stack Pointer (SP)

The stack pointer is a 13-bit register containing the address of the next free location on the pushdown/popup stack. When accessing memory, the most significant bits are permanently configured to 0000011. These bits are appended to the six least significant register bits to produce an address within the range of $00FF to $00C0. The stack area of RAM is used to store the return address on subroutine calls and the machine state during interrupts. During external or power-on reset, and during a reset stack pointer (RSP) instruction, the stack pointer is set to its upper limit ($00FF). Nested interrupt and/or subroutines may use up to 64 (decimal) locations. When the 64 locations are exceeded, the stack pointer wraps around and points to its upper limit ($00FF), thus, overwriting the previously stored information. A subroutine call occupies two RAM bytes on the stack, while an interrupt uses five RAM bytes.

Condition Code Register (CC)

The condition code register is a 5-bit register which indicates the results of the instruction just executed as well as the state of the processor. These bits can be individually tested by a program and specified action taken as a result of their state. Each bit is explained in the following paragraphs.

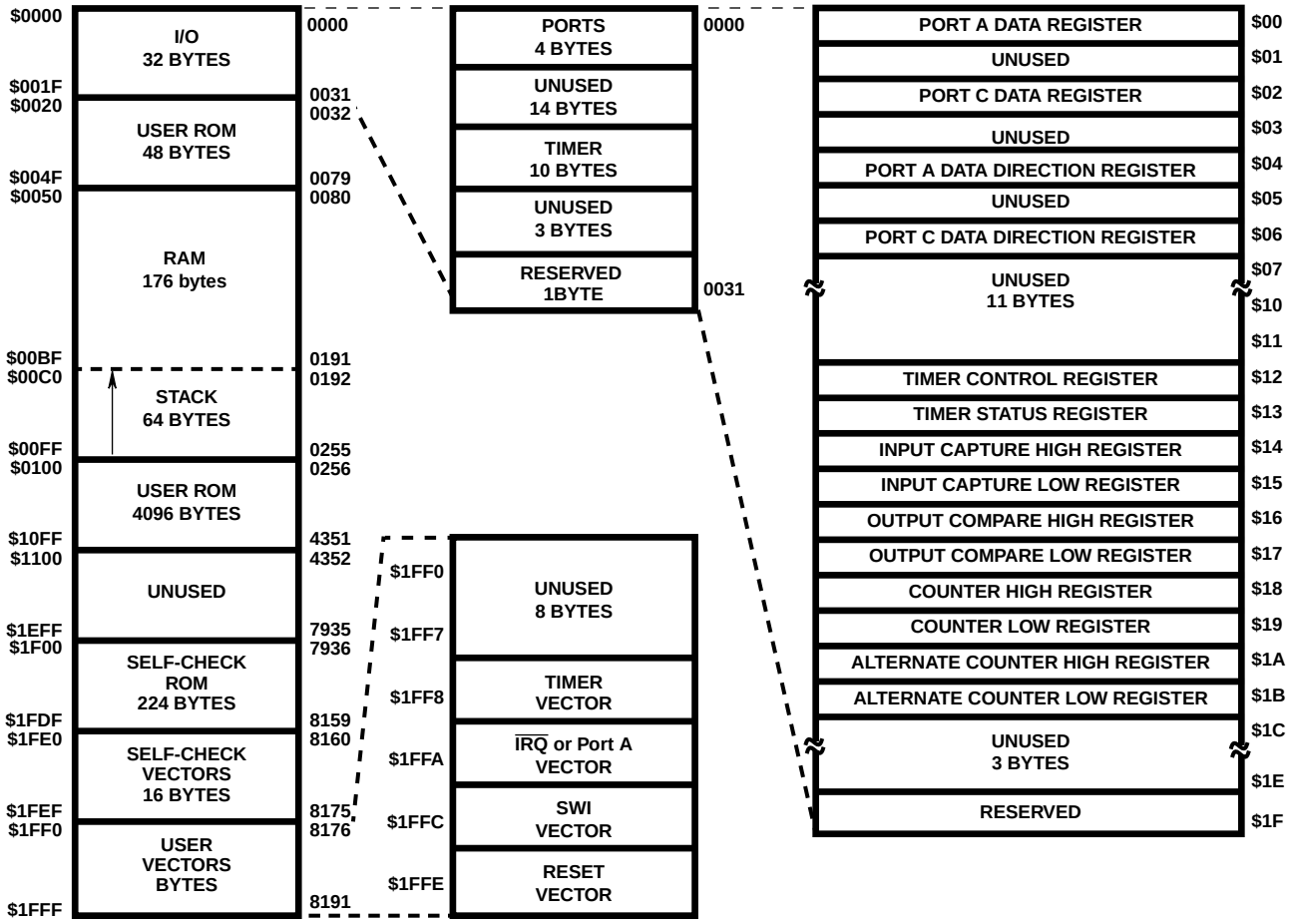


FIGURE 5. ADDRESS MAP

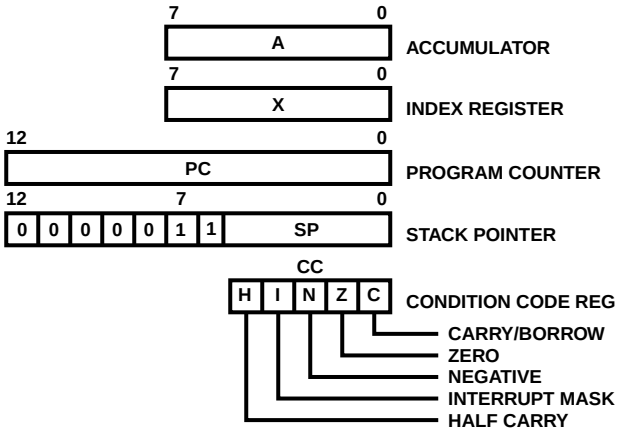


FIGURE 6. PROGRAMMING MODEL

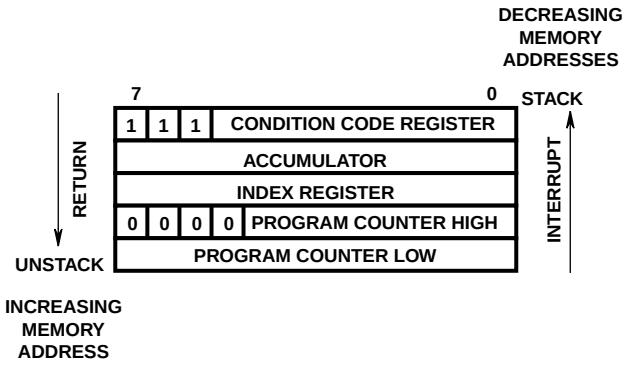


FIGURE 7. STACKING ORDER

Half Carry Bit (H)

The H-bit is set to a one when a carry occurs between bits 3 and 4 of the ALU during an ADD or ADC instruction. The H-bit is useful in binary coded decimal subroutines.

Interrupt Mask Bit (I)

When the I-bit is set, all interrupts are disabled. Clearing this bit enables the interrupts. If an external ($\overline{IRQ}$ or Port A) interrupt occurs while the I-bit is set, the interrupt is latched and processed after the I-bit is next cleared; therefore, no interrupts are lost because of the I-bit being set. An internal interrupt can be lost if it is cleared while the I-bit is set (refer to Programmable Timer Section for more information).

Negative (N)

When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation is negative (bit 7 in the result is a logic one).

Zero (Z)

When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation is zero.

Carry/Borrow (C)

Indicates that a carry or borrow out of the arithmetic logic unit (ALU) occurred during the last arithmetic operation. This bit is also affected during bit test and branch instructions, shifts, and rotates.

Resets, Interrupts, and Low Power Modes

RESETS

The MCU has two reset modes: an active low external reset pin ($\overline{\text{RESET}}$) and a power-on reset function; refer to Figure 8.

RESET Pin

The $\overline{\text{RESET}}$ input pin is used to reset the MCU to provide an orderly software start-up procedure. When using the external reset mode, the $\overline{\text{RESET}}$ pin must stay low for a minimum of one and one half t_{CYC}. The $\overline{\text{RESET}}$ pin contains an internal Schmitt Trigger as part of its input to improve noise immunity.

Power-On Reset

The power-on reset occurs when a positive transition is detected on V_{DD}. The power-on reset is used strictly for power turn-on conditions and should not be used to detect any drops in the power supply voltage. There is no provision for a power-down reset.

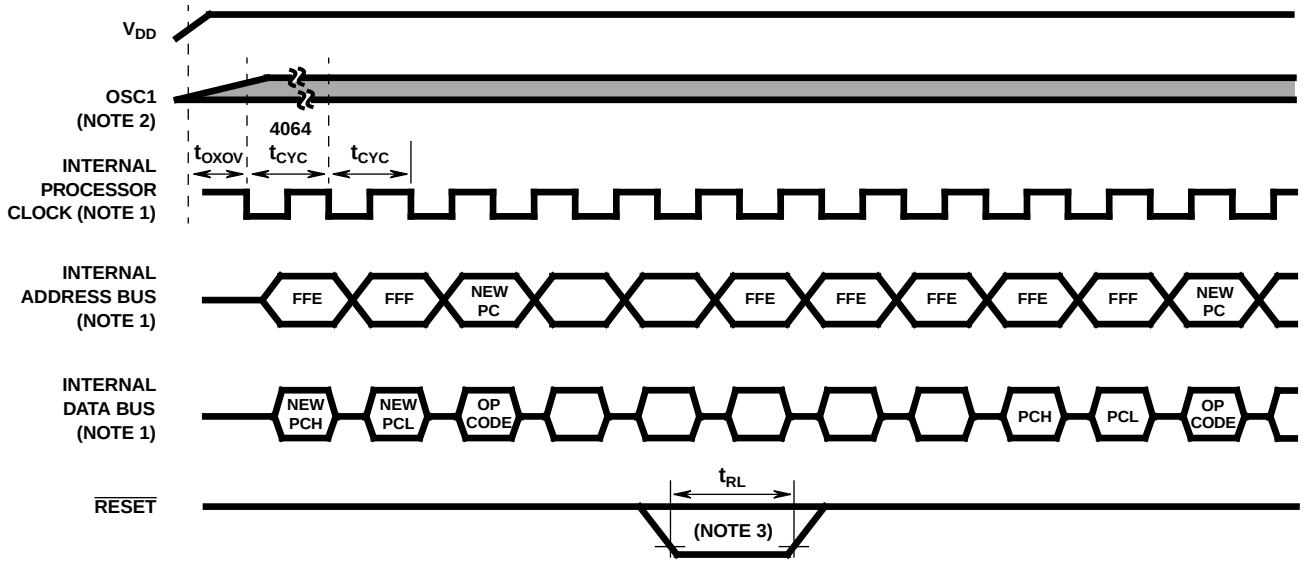
If the crystal oscillator option is chosen, the power-on circuitry provides for a 4064 t_{CYC} delay from the time that the oscillator becomes active. If the external $\overline{\text{RESET}}$ pin is low at the end of the 4064 t_{CYC} time out, the processor remains in the reset condition until $\overline{\text{RESET}}$ goes high.

If the RC oscillator option is chosen, the power-on circuitry provides a 2 t_{CYC} delay from the time that the oscillator becomes active. If the external $\overline{\text{RESET}}$ pin is low at the end of the 2 t_{CYC} time out, the processor remains in the reset condition until $\overline{\text{RESET}}$ goes high. Table 3 shows the actions of the two resets on internal circuits, but not necessarily in order of occurrence (X indicates that the condition occurs for the particular reset).

INTERRUPTS

Systems often require that normal processing be interrupted so that some external event may be serviced. The CDP68HC05J4 may be interrupted in one of two different methods: either via any of the maskable hardware interrupts ($\overline{\text{IRQ}}$/Port A or Timer) or via the non-maskable software interrupt (SWI). The Timer interrupt has several flag and status bits which control the interrupt.

Generally, interrupt flags are located in read-only status register, whereas their equivalent enable bits are located in associated control registers. The interrupt flags and enable bits are never contained in the same register. If the enable bit is a logic zero it blocks the interrupt from occurring but does not inhibit the flag from being set. Reset clears all enable bits to preclude interrupts during the reset procedure.



NOTES:

1. Internal timing signal and bus information is not available externally.
2. OSC1 line is not meant to represent frequency. It is only meant to represent time.
3. The next rising edge of the internal processor clock following the rising edge of $\overline{\text{RESET}}$ initiates the reset sequence.

FIGURE 8. POWER-ON RESET AND $\overline{\text{RESET}}$

TABLE 3. RESET ACTION ON INTERNAL CIRCUIT

CONDITION	$\overline{\text{RESET}}$ PIN	POWER-ON RESET
Oscillator Start-Up Delay Set to 4064 t_{CYC} (8128 Oscillator Cycles)	Note 1	X
Timer Prescaler Reset to Zero State	X	X
Timer Counter Configured to $FFFC	X	X
Timer Output Compare (TCMP) Bit Reset to Zero	X	X
All Timer Interrupt Enable Bits Cleared (ICIE, OCIE, and TOIE) to Disable Timer Interrupts	X	X
Timer OLVL Bit is Cleared to Zero	X	X
Both Port A and Port C DDR'S Cleared to Zero Configuring All Port Pins as Inputs	X	X
Configure Stack Pointer to $00FF	X	X
Force Internal Address to the RESET Vector ($1FFE)	X	X
Set Bit in Condition Code Register to a Logic One to Disable All Interrupts Except SWI	X	X
Clear External Interrupt Latch	X	X
Clear WAIT Latch	X	X
Clear Stop Latch	X (Note 2)	X

NOTES:

1. A delay of 2 t_{CYC} (4 oscillator cycles) is introduced when restarting with RESET, except from STOP mode.
2. 4064 t_{CYC} oscillator start-up time-out occurs.

The general sequence for clearing an interrupt is a software sequence of first accessing the status register while the interrupt flag is set, followed by a read or write of an associated register. When any of these interrupts occur, and if the enable bit is a logic 1, normal processing is suspended at the end of the current instruction execution. Interrupts cause the processor registers to be saved on the stack (see Figure 7) and the interrupt mask (I-bit) set to prevent additional interrupts. The appropriate interrupt vector then points to the starting address of the interrupt service routine (refer to Figure 5 for vector location). Upon completion of the interrupt service routine, the RTI instruction (which is normally a part of the service routine) causes the register contents to be recovered from the stack followed by a return to normal processing. The stack order is shown in Figure 7.

A discussion of interrupts, plus a table listing vector addresses for all interrupts, including RESET, of the MCU is provided in Table 4.

Hardware Controlled Interrupt Sequence

The following three functions (RESET, STOP, and WAIT) are not in the strictest sense an interrupt; however, they are acted upon in a similar manner. Flowcharts for hardware interrupts are shown in Figure 9, and for STOP and WAIT are provided in Figure 10. A discussion is provided below.

(a) RESET - A low input on the $\overline{\text{RESET}}$ input pin causes the program to vector to its starting address which is specified by the contents of memory locations $1FFE and $1FFF. The I-bit in the condition code register is also set. Much of the MCU is configured to a known state during this type of reset as previously described in RESETS paragraph.

(b) STOP - The STOP instruction causes the oscillator to be turned off and the processor to "sleep" until an external interrupt (IRQ or Port A interrupt) or a RESET.

(c) WAIT - The WAIT instruction causes all processor clocks to stop, but leaves the Timer running. This "rest" state of the processor can be cleared by RESET, an external interrupt ($\overline{\text{IRQ}}$ or Port A) or Timer interrupt.

TABLE 4. VECTOR ADDRESSES FOR INTERRUPTS AND RESET

REGISTER	FLAG NAME	INTER-RUPTS	CPU INTERRUPT	VECTOR ADDRESS
N/A	N/A	Reset	$\overline{\text{RESET}}$	$1FFE - $1FFF
N/A	N/A	Software	SWI	$1FFC - $1FFD
N/A	N/A	External Interrupt	$\overline{\text{IRQ}}$ or Port A	$1FFA - $1FFB
Timer Status (TCR)	ICF OCF TOF	Input Capture Output Compare Timer Overflow	TIMER	$1FF8 - $1FF9

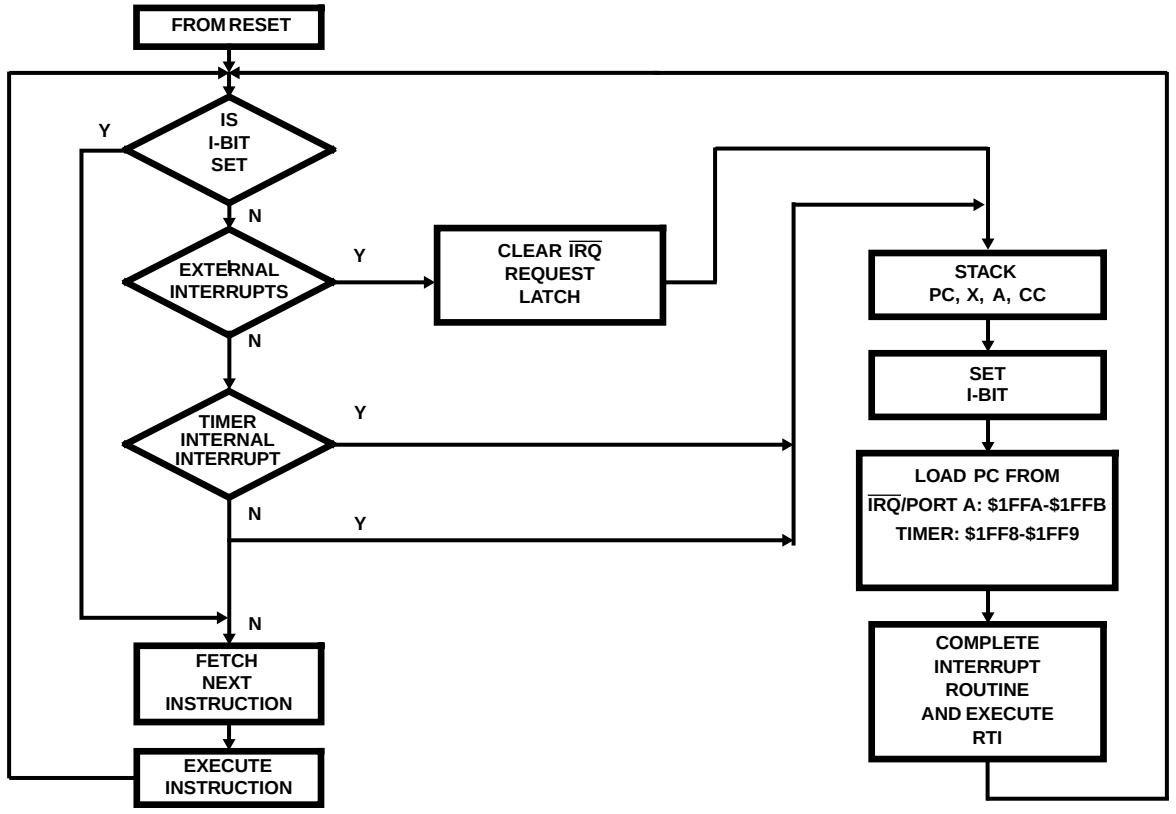


FIGURE 9. HARDWARE INTERRUPT FLOWCHART

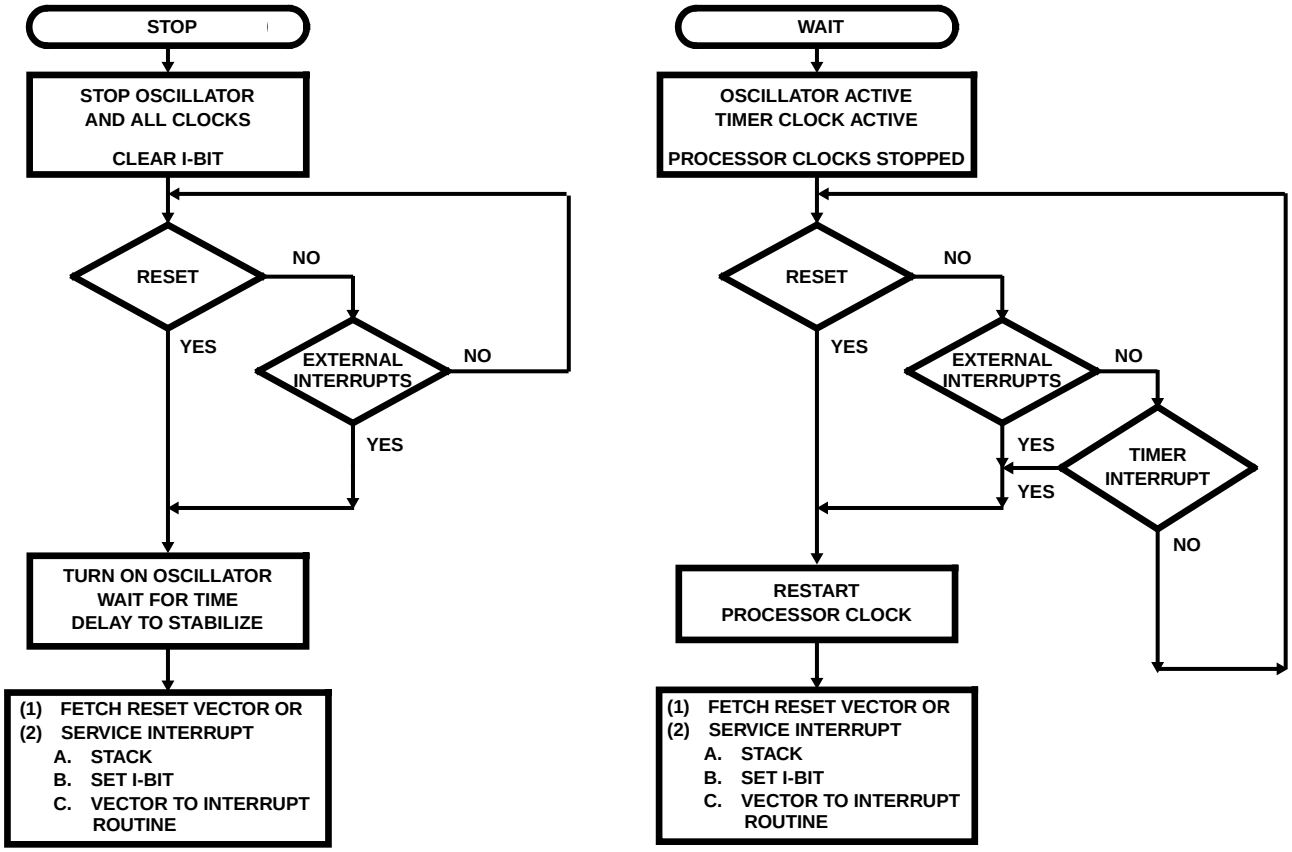


FIGURE 10. STOP/WAIT FLOWCHARTS

There are no special “WAIT” or “STOP” vectors for the interrupts. When the processor is released from the WAIT or STOP state, the same RESET and interrupt vectors are used as at all other times. The processor provides no indication that a WAIT or STOP state has been exited.

Software Interrupt (SWI)

The software interrupt is an executable instruction. The action of the SWI instruction is similar to the hardware interrupts. The SWI is executed regardless of the state of the interrupt mask (I-bit) in the condition code register. The interrupt service routine address is specified by the contents of memory location $1FFC and $1FFD.

External Interrupt

There are two sources of External Interrupts: the IRQ pin and the Port A pins. If the interrupt mask (I-bit) of the condition code register has been cleared and the external interrupt pin (lRQ) or a Port A pin (if mask programmed for interrupt and software programmed as input) has gone low, then the external interrupt is recognized. When the interrupt is recognized, the current state of the CPU is pushed onto the stack and the I-bit is set. This masks further interrupts until the present one is serviced. The interrupt service routine address is specified by the contents of memory location $1FFA and $1FFB. Either a level-sensitive and negative edge-sensitive trigger, or a negative edge sensitive only trigger are available as a mask option for all External Interrupts. Figure 11 shows both a functional and mode timing diagram for the interrupt line. The timing diagram shows two different treatments of the interrupt lines (lRQ/Port A) to the processor. The first method shows single pulses on the interrupt lines spaced far enough apart to be serviced. The minimum time between pulses is a function of the number of cycles required to execute the interrupt service routine plus 21 cycles. Once a pulse occurs, the next pulse should not occur until the MCU software has exited the routine (an RTI occurs). The second configuration shows several interrupt lines “wire-ORed” to form the interrupts at the processor. Thus, if after servicing one interrupt another interrupt line remains low, then the next interrupt is recognized.

NOTE: The internal interrupt latch is cleared in the first part of the service routine; therefore, one (and only one) external interrupt pulse could be latched during t_{ILIL} and serviced as soon as the I-bit is cleared.

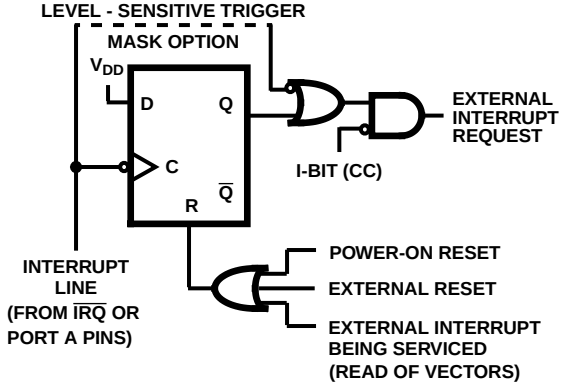
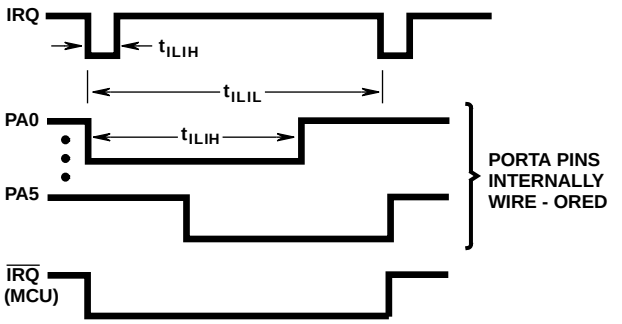


FIGURE 11A. EXTERNAL INTERRUPT FUNCTION DIAGRAM



NOTE:
Edge-Sensitive Trigger Condition - The minimum pulse width (t_{ILIH}) is either 125ns (V_{DD} = 5V) or 250ns (V_{DD} = 3V). The period t_{ILIL} should be less than the number of t_{CYC} cycles it takes to execute the interrupt service routine plus 21 t_{CYC} cycles.

Level-Sensitive Trigger Condition - If after servicing an interrupt the $\overline{IRQ}$ remains low, then the next interrupt is recognized.

FIGURE 11B. EXTERNAL INTERRUPT MODE DIAGRAM

Port A Interrupt Programming

The Port A interrupt mask option, allows the six Port A pins to be individually programmed to cause an external interrupt. For an interrupt to occur, the port pin must also be programmed as an input by setting the associated bit low in the DDRA. These six lines are internally ORed with the $\overline{IRQ}$ pin and behave in every way like the $\overline{IRQ}$ pin. The level-only/edge-and-level interrupt mask option affects all Port A and $\overline{IRQ}$ pins equally. Similarly, the BIH and BIL instructions are sensitive to the logical OR of all interrupt enabled Port A pins and the $\overline{IRQ}$ pin.

NOTE: BIH will cause a branch if and only if all interrupt enabled Port A pins and the $\overline{IRQ}$ pin are high. BIL will cause a branch if any of the interrupt enabled Port A pins or the $\overline{IRQ}$ pin is low.

Timer Interrupt

There are three different timer interrupt flags that will cause a timer interrupt whenever they are set and enabled. These three interrupt flags are found in the three most significant bits of the timer status register (TSR, location $13) and all three will vector to the same interrupt service routine ($1FF8 - $1FF9). All interrupt flags have corresponding enable bits (ICE, OCIE, and TOIE) in the timer control register (TCR, location $0012). Reset clears all enable bits, thus preventing an interrupt from occurring during the reset time period. The actual processor interrupt is generated only if the I-bit in the condition code register is also cleared. When the interrupt is recognized, the current machine state is pushed onto the stack and I-bit is set. This masks further interrupts until the present one is serviced.

The interrupt service routine address is specified by the contents of memory locations $1FF8 and $1FF9. The general sequence for clearing an interrupt is a software sequence of accessing the status register while the flag is set, followed by a read or write of an associated register. Refer to Programmable Timer for additional information about the timer circuitry.

LOW-POWER MODES

STOP Instruction

The STOP instruction places the MCU in its lowest power consumption mode. In the STOP mode the internal oscillator is turned off, causing all internal processing to be halted' refer to Figure 10. During the STOP mode, the I-bit in the condition code register is cleared to enable external interrupts. All other registers and memory remain unaltered and all input/output lines remain unchanged. This continues until an external interrupt (IRQ or Port A) or a RESET is sensed, at which time the internal oscillator is turned on. The external interrupt or RESET causes the program counter to load a vector from memory locations $1FFA-1FFB, or $1FFE-1FFF which contain the starting address of the interrupt or RESET service routine.

WAIT Instruction

The WAIT instruction places the MCU in a low power consumption mode, but the WAIT mode consumes somewhat more power than the STOP mode. In the WAIT mode, the internal clock remains active, and all CPU processing is stopped; however, the programmable timer system remains active. Refer to Figure 10. During the WAIT mode, the I-bit in the condition code register is cleared to enable all interrupts (Timer interrupts must be enabled by setting the appropriate bits in the TCR prior to entering WAIT). All other registers and memory remain unaltered and all parallel input/output lines remain unchanged. This continues until any interrupt or RESET is sensed. At this time the program counter loads a vector from the appropriate memory location which contains the starting address of the interrupt or RESET service routine.

Data Retention Mode

The contents of RAM and CPU registers are retained at supply voltages as low as 2VDC. This is referred to as the Data Retention mode, where the data is held, but the device is not guaranteed to operate.

Programmable Timer

Introduction

The programmable timer, which is preceded by a fixed divide-by-four prescaler, can be used for many purposes, including input waveform measurements while simultaneously generating an output waveform. Pulse widths can vary from several microseconds to many seconds. A block diagram of the timer is shown in Figure 12 and timing diagrams are shown in Figures 13 through 16.

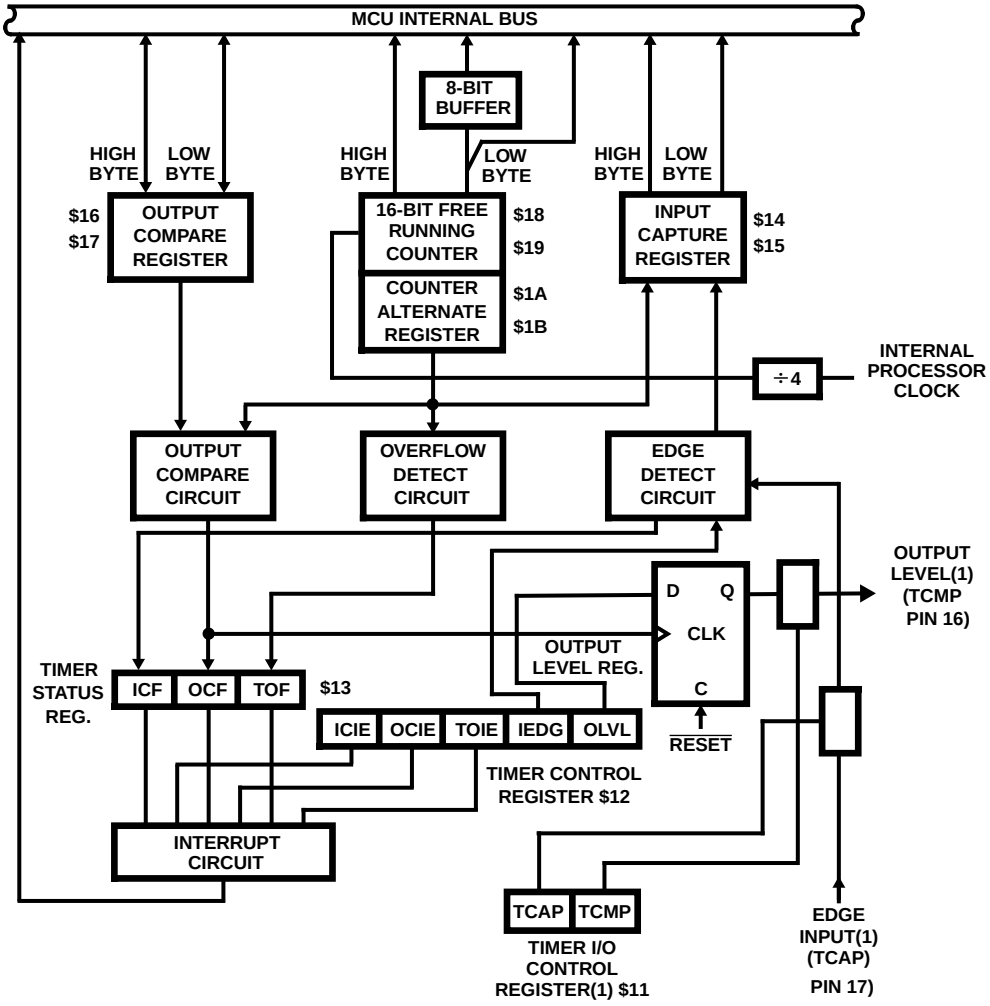
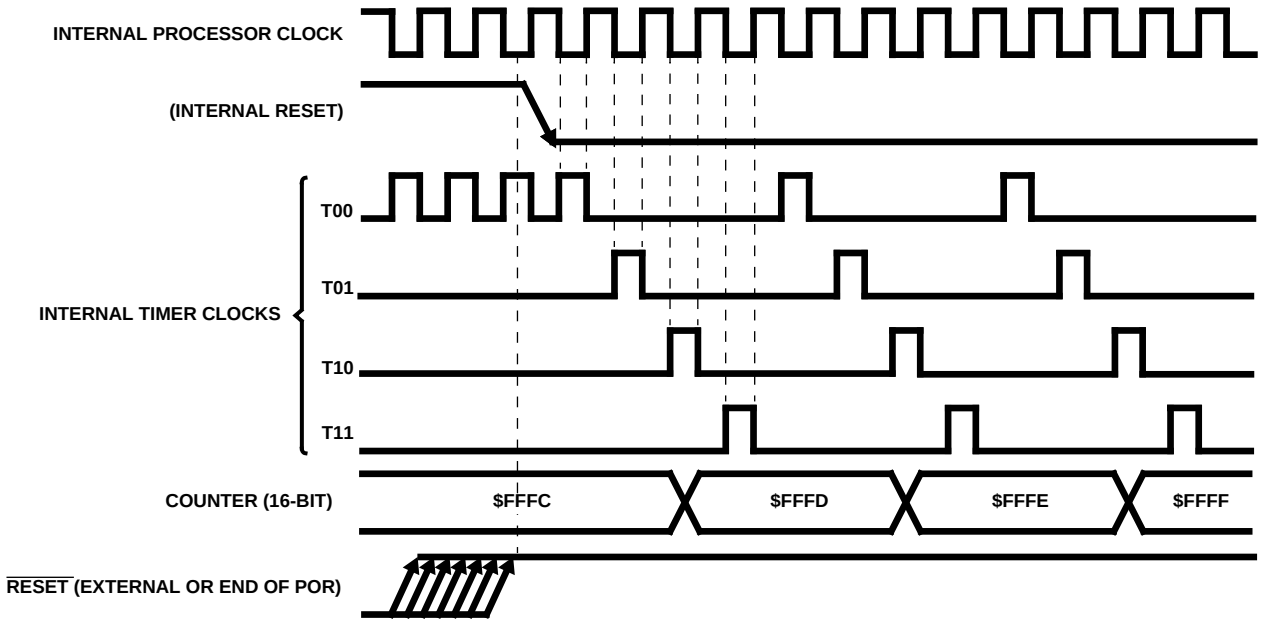


FIGURE 12. PROGRAMMABLE TIMER BLOCK DIAGRAM

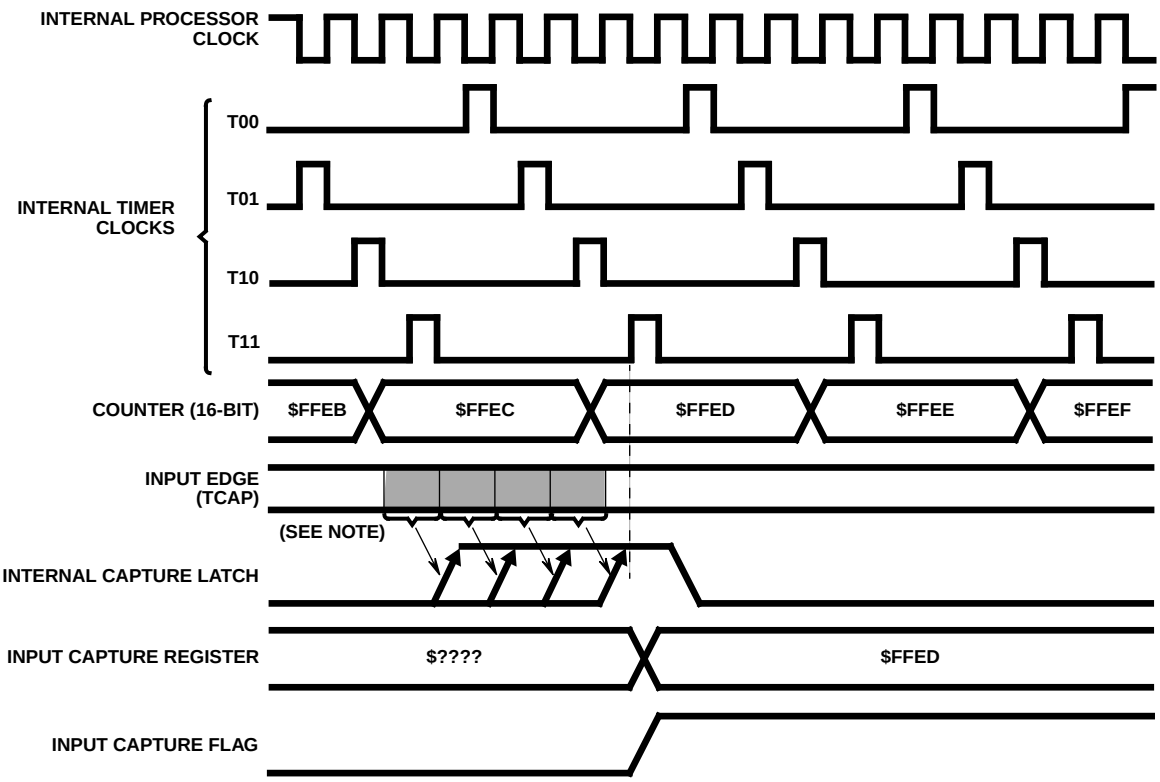
Timing Diagrams



NOTE:

1. The Counter Register and the Timer Control Register are the only ones affected by $\overline{\text{RESET}}$.

FIGURE 13. TIMER STATE DIAGRAM FOR RESET

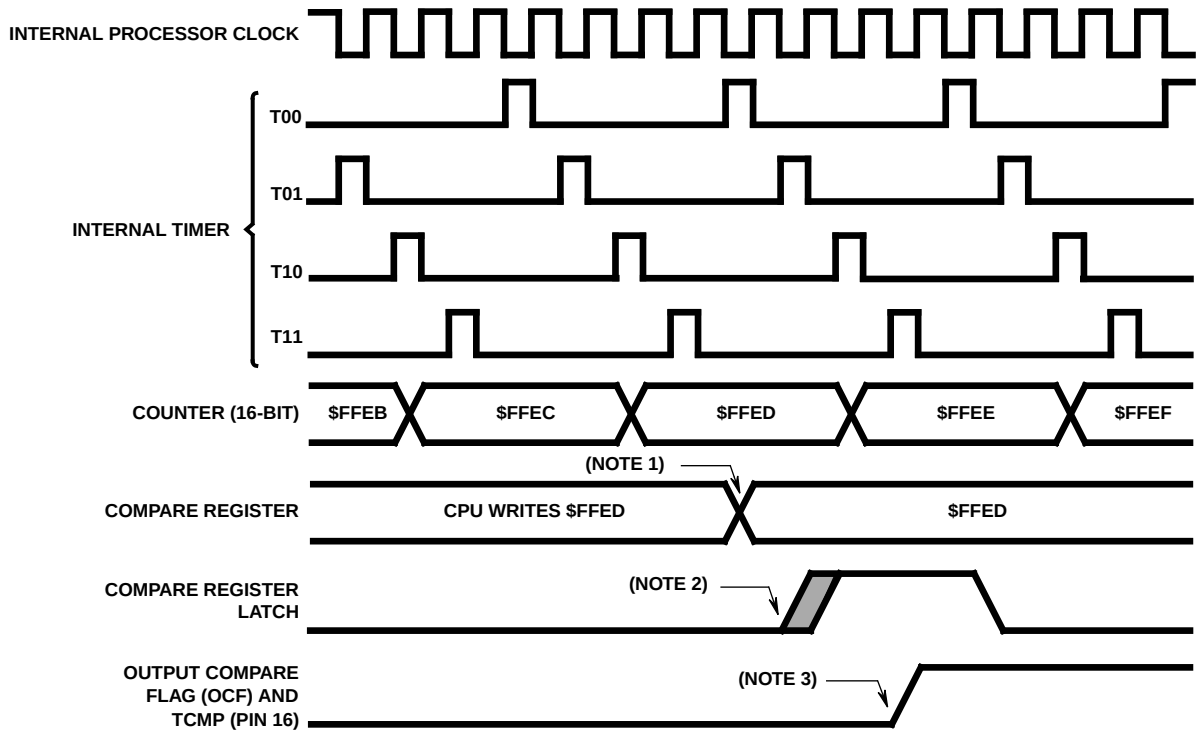


NOTE:

1. If the input edge occurs in the shaded area from one timer state T10 to the other timer state T10 the input capture flag is set during the next state T11.

FIGURE 14. TIMER STATE TIMING DIAGRAM FOR INPUT CAPTURE

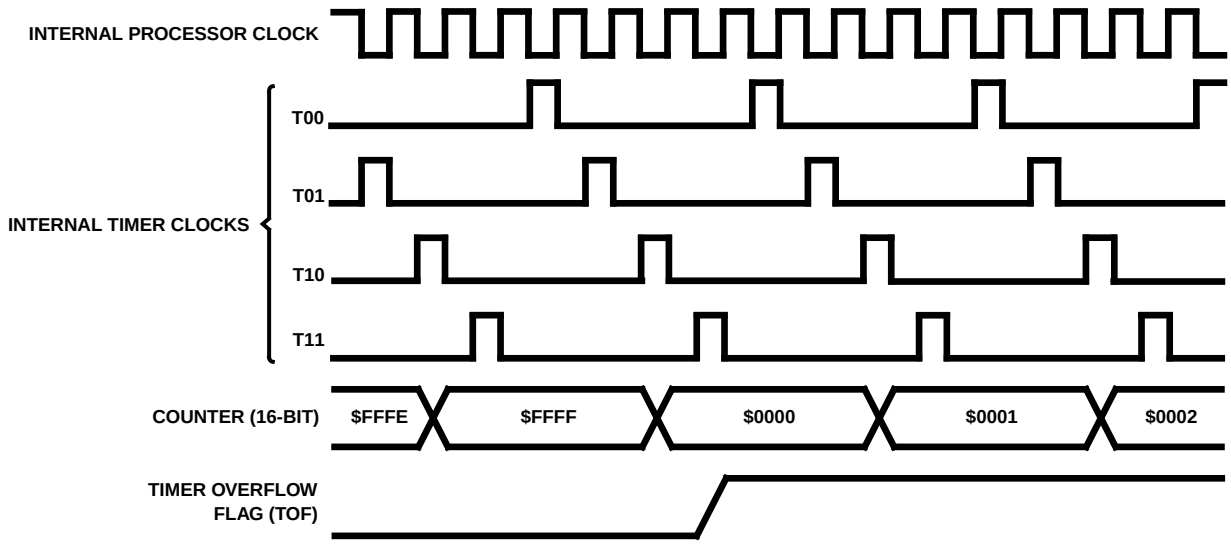
Timing Diagrams (Continued)



NOTE:

1. The CPU write to the Compare Register may take place at any time, but a compare only occurs at timer state T01. Thus a 4 cycle difference may exist between the write to the Compare Register and the actual compare.
2. Internal compare takes place during timer state T01.
3. OCF is set at the timer state T11 which follows the comparison match ($FFED in this example).

FIGURE 15. TIMER STATE TIMING DIAGRAM FOR OUTPUT COMPARE



NOTE:

1. The TOF bit is set at timer state T11 (transition of the counter from $FFFF to $0000). It is cleared by a read of the Timer Status Register during the internal processor clock high time followed by a read of the Counter Low Register.

FIGURE 16. TIMER STATE DIAGRAM FOR TIMER OVERFLOW

Because the timer has a 16-bit architecture, each specific functional segment (capability) is represented by two registers. These registers contain the high and low byte of that functional segment. Generally, accessing the low byte of a specific timer function allows full control of that function; however, an access of the high byte inhibits that specific timer function until the low byte is also accessed.

NOTE: The I-bit in the condition code register should be set while manipulating both the high and low byte register of a specific timer function to ensure that an interrupt does not occur. This prevents interrupts from occurring between the time that the high and low byte are accessed.

The programmable timer capabilities are provided by using the following ten addressable 8-bit registers (note the high and low represent the significance of the byte). A description of each register is provided below.

Timer Control Register (TCR) location $12,

Timer Status Register (TSR) location $13,

Input Capture High Register location $14,

Input Capture Low Register location $15,

Output Compare High Register location $16,

Output Compare Low Register location $17,

Counter High Register location $18,

Counter Low Register location $19,

Alternate Counter High Register location $1A, and

Alternate Counter Low Register location $1B.

Counter

The key element in the programmable timer is a 16-bit free running counter, or counter register, preceded by a prescaler which divides the internal processor clock by four. The prescaler gives the timer a resolution of 2.0µs if the internal processor clock is 2.0MHz. The counter is clocked to increasing values during the low portion of the internal processor clock. Software can read the counter at any time without affecting its value.

The double byte free running counter can be read from either of two locations $18 - $19 (called counter register at this location), or $1A - $1B (counter alternate register at this location). If a read sequence containing only a read of the least significant byte of the free running counter or counter alternate register first addresses the most significant byte ($18, $1A) it causes the least significant byte ($19, $1B) to be transferred to a buffer. This buffer value remains fixed after the first most significant byte “read” even if the user reads the most significant byte several times. This buffer is accessed when reading the free running counter or counter alternate register, if the most significant byte is read, the least significant byte must also be read in order to complete the sequence.

The free running counter is configured to $FFFC during reset and is always a read-only register. During a power-on-reset (POR), the counter is also configured to $FFFC and begins running after the oscillator start-up delay. Because the free running counter is 16 bits preceded by a fixed divide-by-four prescaler, the value in the free running counter repeats every 262,144 MPU internal processor clock cycles. When the counter rolls over from $FFFF to $0000, the timer overflow flag (TOF) bit is set. An interrupt can also be enabled when counter roll-over occurs by setting its interrupt enable bit (TOIE).

Output Compare Register

The output compare register is a 16-bit register, which is made up of two 8-bit registers at locations $16 (most significant byte) and $17 (least significant byte). The output compare register can be used for several purposes such as, controlling an output waveform or indicating when a period of time has elapsed. The output compare register is unique in that all bits are readable and writable and are not altered by the timer hardware. Reset does not affect the contents of this register and if the compare function is not utilized, the two bytes of the output compare register can be used as storage locations.

The contents of the output compare register are compared with the contents of the free running counter once during every four internal processor clocks. If a match is found, the corresponding output compare flag (OCF) bit is set and the corresponding output level (OLVL) bit is clocked (by the output compare circuit pulse) to an output level register. The values in the output compare register and the output level bit should be changed after each successful comparison in order to control an output waveform or establish a new elapsed time-out. An interrupt can also accompany a successful output compare provided the corresponding interrupt enable bit, OCIE, is set.

After a processor write cycle to the output compare register containing the most significant byte ($16), the output compare function is inhibited until the least significant byte ($17) is also written. The user must write both byte (locations) if the most significant byte is written first. A write made only to the least significant byte ($17) will not inhibit the compare function. The free running counter is updated every four internal processor clock cycles due to the internal prescaler. The minimum time required to update the output compare register is a function of the software program rather than the internal hardware. A processor write may be made to either byte of the output compare register without affecting the other byte. The output level (OLVL) bit is clocked to the output level register regardless of whether the output compare flag (OCF) is set or clear.

Because neither the output compare flag (OCF bit) nor the output compare register is affected by RESET, care must be exercised when initializing the output compare function with software. The following procedure is recommended:

1. Write the high byte of the output compare register to inhibit further compares until the low byte is written.
2. Read the timer status register to arm the OCF if it is already set.
3. Write the output compare register low byte to enable the output compare function with the flag clear.

The advantage of this procedure is that it prevents the OCF bit from being set between the time it is read and the write to the output compare register. A software example is shown below.

```
B716  STA  OCMPHI;   INHIBIT OUTPUT COMPARE
B613  LDA  TSTAT;    ARM OCF BIT IF SET
BF17  STX  OCMPLO;   READY FOR NEXT COMPARE
```

Input Capture Register

The two 8-bit registers which make up the 16-bit input capture register are read-only and are used to latch the value of the free running counter after a defined transition is sensed by the corresponding input capture edge detector. The level transition which triggers the counter transfer is defined by the corresponding input edge bit (IEDG). Reset does not affect the contents of the input capture register.

The result obtained by an input capture will be one more than the value of the free running counter on the rising edge of the internal processor clock preceding the external transition (refer to timing diagram shown in Figure 14). This delay is required for internal synchronization. Resolution is affected by the prescaler allowing the timer to only increment every four internal processor clock cycles.

After a read of the most significant byte of the input capture register ($14), counter transfer is inhibited until the least significant byte ($15) of the input capture register is also read. This characteristic forces the minimum pulse period attainable to be determined by the time used in the capture software routine and its interaction with the main program. The free running counter increments every four internal processor clock cycles due to the prescaler.

A read of the least significant byte ($15) of the input capture register does not inhibit the free running counter transfer. Again, minimum pulse periods are ones which allow software to read the least significant byte ($15) and perform needed operations. There is no conflict between the read of the input capture register and the free running counter transfer since they occur on opposite edges of the internal processor clock.

Timer Control Register (TCR)

The timer control register (TCR, location $12) is an 8-bit read/write register which contains five control bits. Three of these bits control interrupts associated with each of the three flag bits found in the timer status register (discussed below). The other two bits control: 1) which edge is significant to the capture edge detector (i.e., negative or positive), and 2) the next value to be clocked to the output level register in response to a successful output compare. The timer control register and the free running counter are the only sections of the timer affected by RESET. The TCMP pin is forced low during external reset and stays low until a valid compare changes it to a high. The timer control register is illustrated below followed by a definition of each bit.

B7, ICIE — If the input capture interrupt enable (ICIE) bit is set, a timer interrupt is enabled when the ICF status flag (in the timer status register) is set. If the ICIE bit is clear, the interrupt is inhibited. The ICIE bit is cleared by RESET.

B6, OCIE — If the output compare interrupt enable (OCIE) bit is set, a timer interrupt is enabled whenever the OCF status flag is set. If the OCIE bit is clear, the interrupt is inhibited. The OCIE bit is cleared by RESET.

B5, TOIE — If the timer overflow interrupt enable (TOIE) bit is set, a timer interrupt is enabled whenever the TOF status flag (in the timer status register) is set. If the TOIE bit is clear, the interrupt is inhibited. The TOIE bit is cleared by RESET.

B1, IEDG — The value of the input edge (IEDG) bit determines which level transition on pin 1 will trigger a free running counter transfer to the input capture register. Reset does not affect the IEDG bit.
0 = negative edge
1 = positive edge

B0, OLVL — The value of the output level (OLVL) bit is clocked into the output level register by the next successful output compare and will appear at pin 2. This bit and the output level register are cleared by RESET.
0 = low output
1 = high output

TCR (LOCATION $12)

7	6	5	4	3	2	1	0
ICIE	OCIE	TOIE	0	0	0	IEDG	OLVL

Timer Status Register (TSR)

The timer status register (TSR) is an 8-bit register of which the three most significant bits contain read-only status information. These three bits indicate the following:

1. A proper transition has taken place at the TCAP pin with an accompanying transfer of the free running counter contents to the input capture register,
2. A match has been found between the free running counter and the output compare register, and
3. A free running counter transition from $FFFF to $0000 has been sensed (timer overflow).

The timer status register is illustrated below followed by a definition of each bit. Refer to timing diagrams shown in Figures 14, 15, and 16 for timing relationship to the timer status register bits.

TSR (LOCATION $13)

7	6	5	4	3	2	1	0
ICF	OCF	TOF	0	0	0	0	0

B7, ICF — The input capture flag (ICF) is set when a proper edge has been sensed by the input capture edge detector. It is cleared by a processor access of the timer status register (with ICF set) followed by accessing the low byte ($15) of the input capture register. Reset does not affect the input compare flag.

B6, OCF — The output compare flag (OCF) is set when the output compare register contents match the contents of the free running counter. The OCF is cleared by accessing the timer status register (with OCF set) and then accessing the low byte ($17) of the output compare register. Reset does not affect the output compare flag.

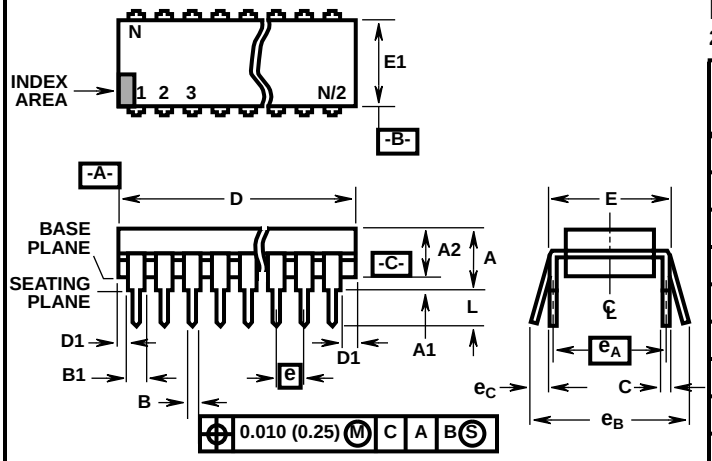
B5, TOF — The timer overflow flag (TOF) bit is set by a transition of the free running counter from $FFFF to $0000. It is cleared by accessing the timer status register (with TOF set) followed by an access of the free running counter least significant byte ($19). Reset does not affect the TOF bit.

Accessing the timer status register satisfies the first condition required to clear any status bits which happen to be set during the access. The only remaining step is to provide an access of the register which is associated with the status bit. Typically, this presents no problem for the input capture and output compare functions.

A problem can occur when using the timer overflow function and reading the free running counter at random times to measure an elapsed time. Without incorporating the proper precautions into software, the timer overflow flag could unintentionally be cleared if: 1) the timer status register is read or written when TOF is set, and 2) the least significant byte of the free running counter is read but not for the purpose of servicing the flag. The counter alternate register at address $1A and $1B contains the same value as the free running counter (at address $18 and $19); therefore, this alternate register can be read at any time without affecting the timer overflow flag in the timer status register.

During STOP and WAIT instructions, the programmable timer functions as follows: during the wait mode, the timer continues to operate normally and may generate an interrupt to trigger the CPU out of the wait state; during the stop mode, the timer holds at its current state, retaining all data, and resumes operation from this point when an external interrupt is received

Dual-In-Line Plastic Packages (PDIP)



NOTES:

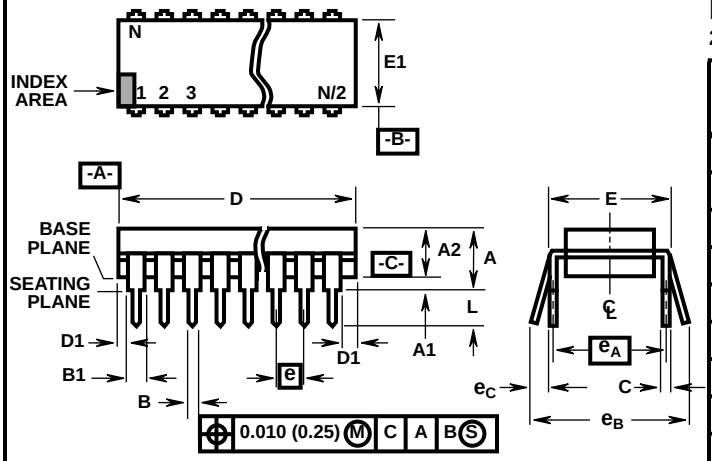
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E20.3 (JEDEC MS-001-AD ISSUE D)
20 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.55	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.980	1.060	24.89	26.9	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	20		20		9

Rev. 0 12/93

Dual-In-Line Plastic Packages (PDIP)



NOTES:

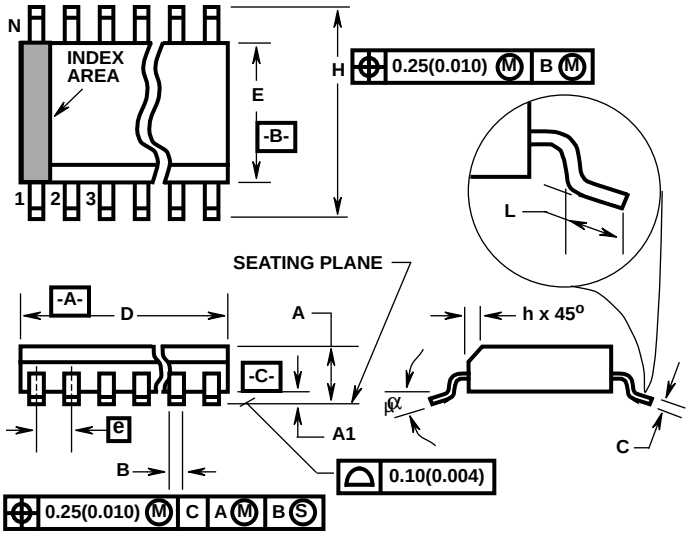
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E28.6 (JEDEC MS-011-AB ISSUE B)
28 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.380	1.565	35.1	39.7	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	28		28		9

Rev. 0 12/93

Small Outline Plastic Packages (SOIC)



M20.3 **(JEDEC MS-013-AC ISSUE C)**
20 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

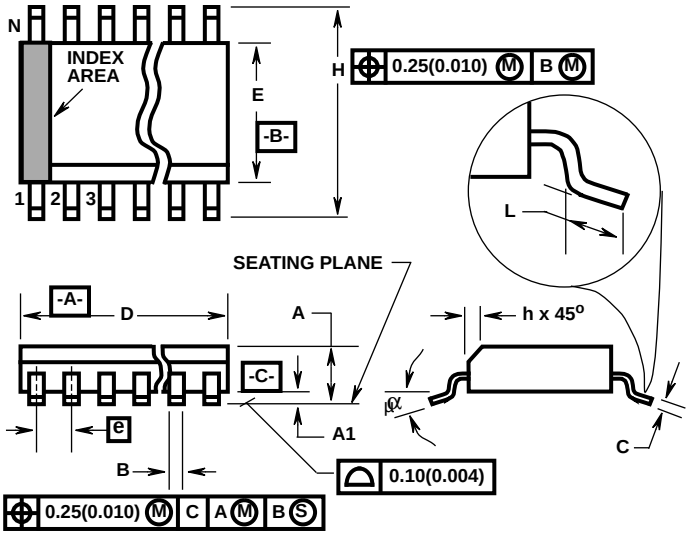
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4961	0.5118	12.60	13.00	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0^o	8^o	0^o	8^o	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC)



M28.3 (JEDEC MS-013-AE ISSUE C)
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0^o	8^o	0^o	8^o	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Notes

A. Package Type (select one):

20 Lead Packages

- ☐ Dual-In-Line Plastic (E20)
- ☐ Small Outline Plastic - SOIC (M20)

28 Lead Packages

- ☐ Dual-In-Line Plastic (E28)
- ☐ Small Outline Plastic - SOIC (M28)

B. Select the following microcomputer options. A manufacturing mask will be generated from this information. Refer to data sheet or data book instructions for submitting data for ROM patterns.

Internal Oscillator (select one)

- ☐ Crystal/Ceramic Resonator
- ☐ Resistor

Input Interrupt Trigger (select one)

- ☐ Edge Sensitive Only
- ☐ Level and Edge Sensitive

TCAP/PC0 (select one)

- ☐ TCAP
- ☐ PC0

TCMP/PC1 (select one)

- ☐ TCMP
- ☐ PC1

Port A Interrupt/Pullup Options (select all that apply - unselected indicates no interrupt and no pullup)

- ☐ PA5 Interrupt and Pullup
- ☐ PA4 Interrupt and Pullup
- ☐ PA3 Interrupt and Pullup
- ☐ PA2 Interrupt and Pullup
- ☐ PA1 Interrupt and Pullup
- ☐ PA0 Interrupt and Pullup

Operating Frequency (select one)

- ☐ Normal
- ☐ High (premium cost)

Operating Power (select one)

- ☐ Normal
- ☐ Low (premium cost)

C. Customer Company _____

Address _____

City _____

Phone (____) _____ Extension _____

Contact Person _____

Customer Part Number _____

D. Pattern Media (S-Record Formatted File Should Be Used - Unspecified locations are filled with 0's)

Floppy Disk: ☐ $3^1/_2$" ☐ $5^1/_4$" MODEM Upload: ☐ S-Record Filename _____

Medium if other than above † _____

Signature _____ Title _____

Date _____

† The J4 requires 8K of data

FOR HARRIS SEMICONDUCTOR USE ONLY

Custom Selection Number _____ Variant Code _____

RETURN THIS COMPLETED FORM TO YOUR HARRIS SEMICONDUCTOR SALES OFFICE OR REPRESENTATIVE

TABLE 5. I/O, CONTROL, STATUS, AND DATA REGISTER DEFINITIONS

	Bit 7	6	5	4	3	2	1	0	
$0000	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	PORT A
			3	4	5	6	7	8	Pin Numbers
	-	-	PA5	PA4	PA3	PA2	PA1	PA0	Pin Name
$0001	UNUSED								
$0002	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	PORT C
	9	8	12	13	14	15	16	17	Pin Numbers
	PC7	PC6	PC5	PC4	PC3	PC2	PC1/TCMP	PC0/TCAP	Pin Name
$0003	UNUSED								
$0004	0	0	I/O	I/O	I/O	I/O	I/O	I/O	DDRA
$0005	UNUSED								
$0006	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	DDRC
$0007	UNUSED								
$0008	UNUSED								
$0009	UNUSED								
$000A	UNUSED								
$000B	UNUSED								
$000C	UNUSED								
$000D	UNUSED								
$000E	UNUSED								
$000F	UNUSED								
$0010	UNUSED								
$0011	UNUSED								
$0012	ICIE	OCIE	TOIE	0	0	0	IEDG	OLVL	TCR
$0013	ICF	OCF	TOF	0	0	0	0	0	TSR
$0014	Bit 15							Bit 8	CAPHI
$0015	Bit 7							Bit 0	CAPLO
$0016	Bit 15							Bit 8	CMPHI
$0017	Bit 7							Bit 0	CMPLO
$0018	Bit 15							Bit 8	CNTHI
$0019	Bit 7							Bit 0	CNTLO
$001A	Bit 15							Bit 8	ALTHI
$001B	Bit 7							Bit 0	ALTLO
$001C	UNUSED								
$001D	UNUSED								
$001E	UNUSED								
$001F	RESERVED								RESERVED