CMOS 4-BIT MICROCONTROLLER

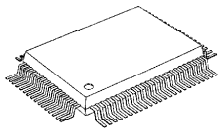
TMP47P1620VF

The 47P1620V is the system evaluation LSI of 47C1220 / 1620 with 128K bits one-time PROM. The 47P1620V programs / verifies using an adapter socket to connect with PROM programmer, as it is in TMM27128AD.
In addition, the 47P1620V and the 47C1220 / 1620 are pin compatible. The 47P1620V operates as the same as the 47C1220 / 1260 by programming to the internal PROM.

PART No.	EPROM	RAM	PACKAGE	ADAPTER SOCKET
TMP47P1620VF	OTP 16384 × 8-bit	768 × 4-bit	QFP80-P-1420-0.80B	BM1162

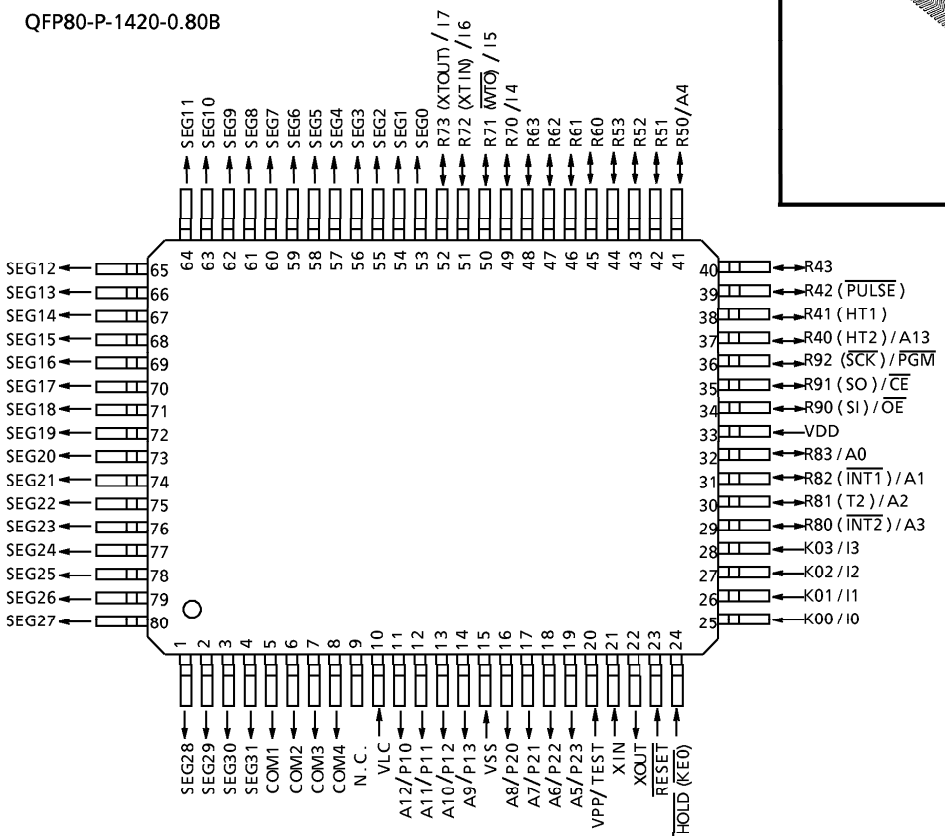
PIN ASSIGNMENT (TOP VIEW)

QFP80-P-1420-0.80B



TMP47P1620VF

QFP80-P-1420-0.80B



PIN FUNCTION

The 47P1620V has MCU mode and PROM mode.

(1) MCU mode

The 47C1220/1620 and the 47P1620V are pin compatible (TEST pin for out-going test. Be fixed to low level).

(2) PROM mode

PIN NAME	INPUT / OUTPUT	FUNCTIONS	PIN NAME(MCU mode)
A13	INPUT	Address inputs	R40
A12 - A9			P10 - P13
A8 - A5			P20 - P23
A4			R50
A3 - A0			R80 - R83
I7 - I4	I/O	Data outputs (Inputs)	R73 - R70
I3 - I0			K03 - K00
$\overline{PGM}$	Input	Program control input	R92
$\overline{CE}$		Chip Enable input	R91
$\overline{OE}$		Output Enable input	R90
VPP	Power supply	+ 12.5V / 5V (Program supply voltage)	TEST
VCC		+ 5V	VDD
VSS		0V	VSS
SEG31 - SEG0	output	Open	
COM4 - COM1			
VLC	Power supply		
N.C.			
R53 - R51	I/O	Be fixed to low level	
R63 - R60			
R43 - R41			
$\overline{RESET}$	Input	PROM mode setting pins. Be fixed to low level.	
$\overline{HOLD}$	Input		
XIN	Input	Resonator connecting pins	
XOUT	output		

OPERATIONAL DESCRIPTION

The following is an explanation of hardware configuration and operation in relation to the 47P1620V. The 47P1620V is the same as the 47C1220/1620 except that an OTP is used instead of a built-in mask ROM.

1. OPERATION mode

The 47P1620V has an MCU mode and a PROM mode.

1.1 MCU mode

The MCU mode is set by fixing the TEST/VPP pin at the "L" level. Operation in the MCU mode is the same as for the 47C1220/1620, except that the TEST/VPP pin does not have built in pull-down resistor and cannot be used open.

1.1.1 Program Memory

The program storage area is the same as for the 47C1620. Data conversion tables must be set in two locations when using the 47P1620V to check 47C1220 operation.

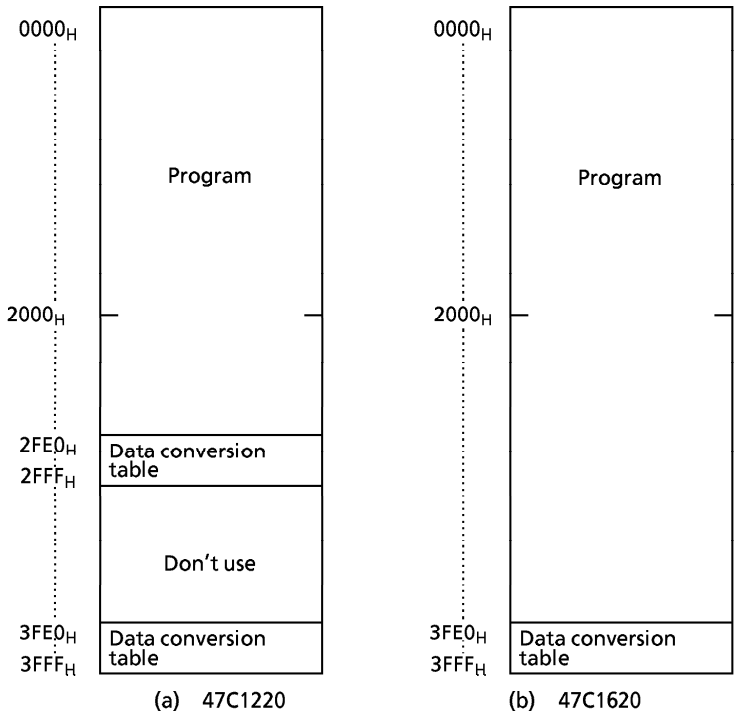


Figure 1-1. Program area

1.1.2 Data Memory

The 47P1620V has 768 × 4-bit of data memory (RAM), 256 × 4-bit (addresses 00_H through FF_H) on each of banks (bank 0, bank 1 and bank 2).

1.1.3 Input/Output Circuitry

(1) Control pins
This is the same as for the 47C1220/1620 except that there is no built-in pull-down resistance for the TEST pin.

(2) I/O Ports
The input/output circuit of the 47P1620V is the same as I/O code GA of the 47C1220/1620.
External resistance, for example, is required when using as evaluator of other I/O codes (GB to GF), (Refer to Figure 1-2)

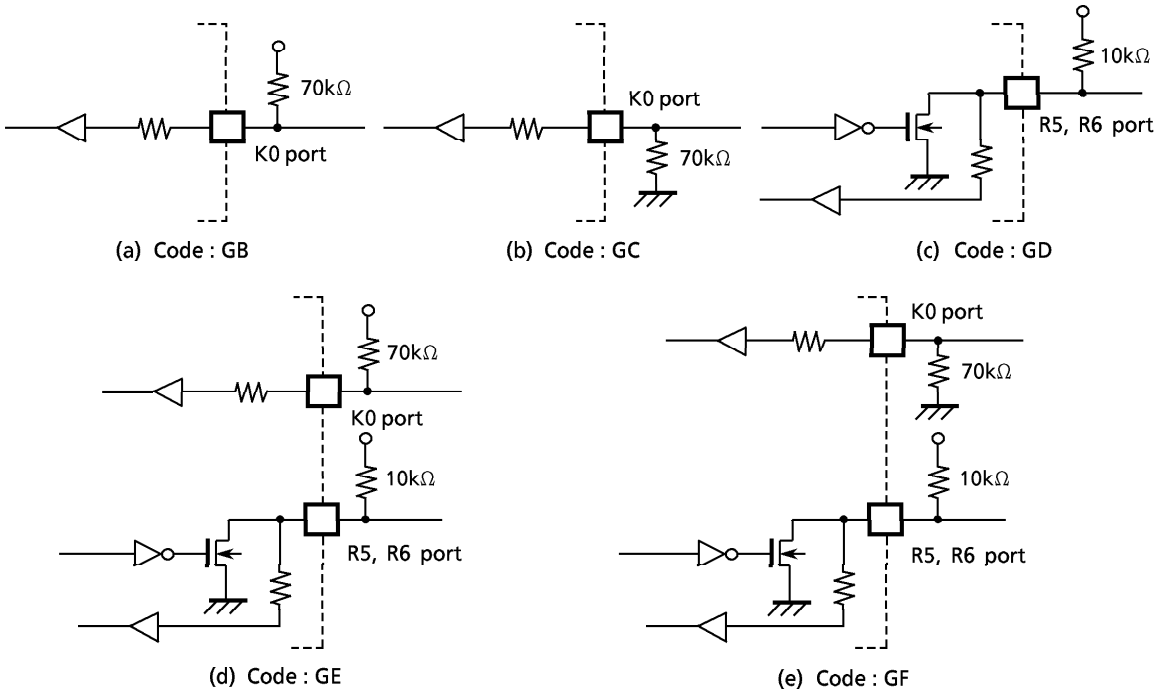


Figure 1-2. I/O code and external circuitry

1.2 PROM mode

The PROM mode is set by setting the $\overline{RESET}$, $\overline{HOLD}$ pins to the "L" level. The PROM mode can be used as a general-purpose PROM writer for program writing and verification (A high-speed program mode is used set the ROM type the same as for the TMM 27128AD.)

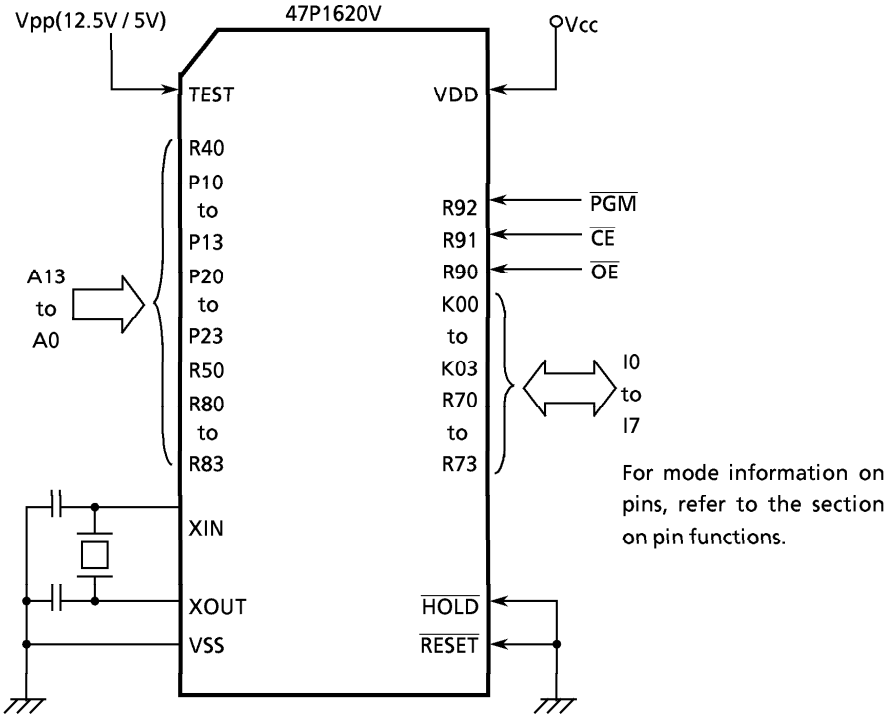


Figure 1-3. Setting for PROM mode

1.2.1 High Speed Programming Mode

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+ 12.5V) is applied to the V_{PP} terminal with V_{CC} = 6V and $\overline{PGM}$ = V_{IH}.

The programming is achieved by applying a single low level 1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, one additional program pulse with pulse width 3 times that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with V_{CC} = V_{PP} = 5V.

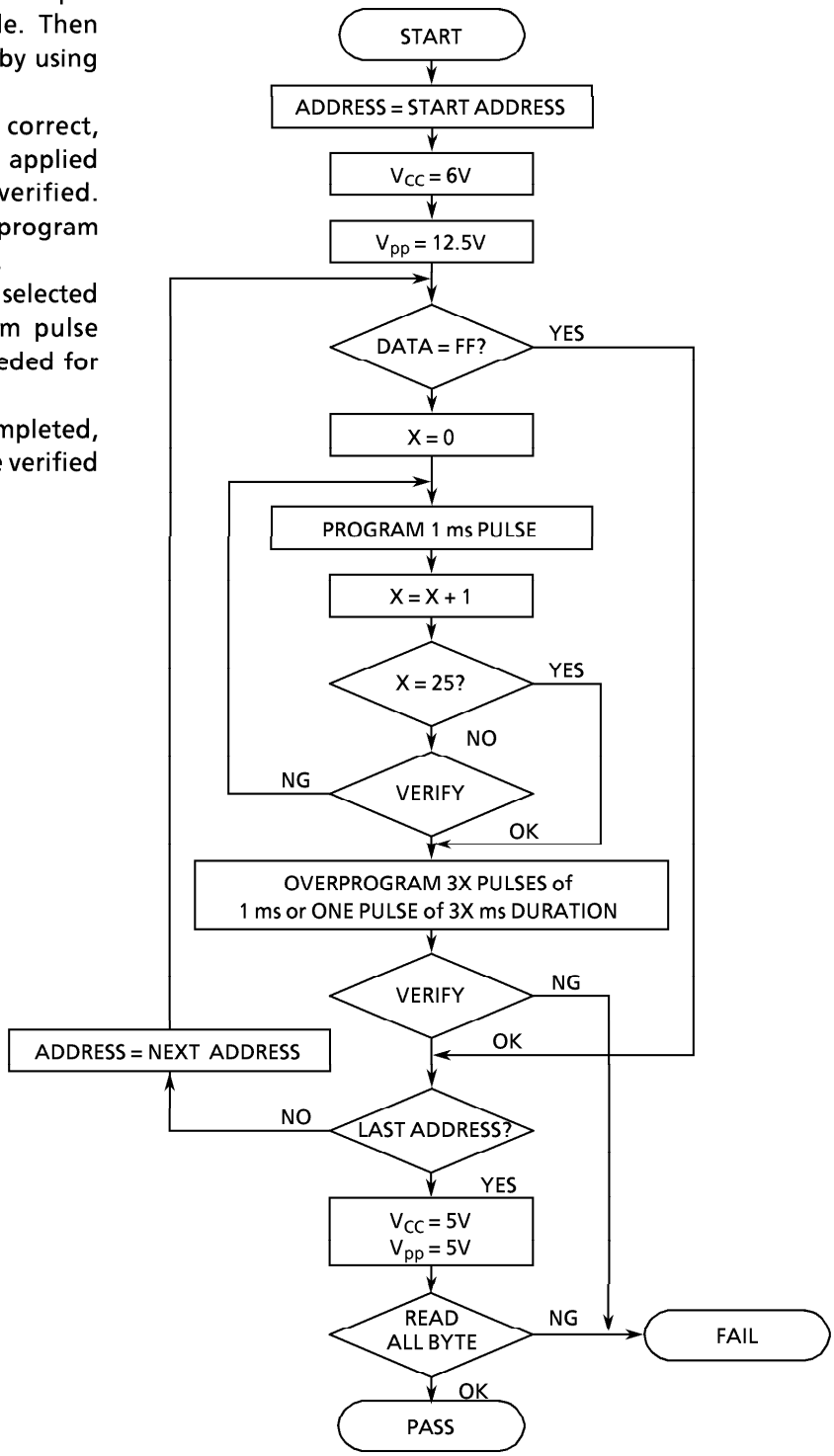


Figure 1-4. Flow Chart

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATINGS	UNIT
Supply Voltage	V_{DD}		– 0.3 to 7	V
Program Voltage	V_{PP}		– 0.3 to 13.0	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	Except sink open drain pin	– 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	Sink open drain pin	– 0.3 to 10	
Output Current (Per 1 pin)	I_{OUT1}	Ports R4 to R9	3.2	mA
	I_{OUT2}	Ports P1, P2	15	
Output Current (Total)	ΣI_{OUT1}	Ports P1, P2	60	mA
Power Dissipation [T_{opr} = 70°C]	PD		600	mW
Soldering Temperature (time)	T_{sld}		260 (10 s)	°C
Storage Temperature	T_{stg}		– 55 to 125	°C
Operating Temperature	T_{opr}		– 40 to 70	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_{opr} = – 40 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		In the Normal mode fc = 4.2MHz	2.7	6.0	V
			In the Normal mode fc = 6MHz	4.5		
			In the SLOW mode	2.7		
			In the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5V$	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5V$		$V_{DD} \times 0.1$	
Clock Frequency	fc	XIN, XOUT	V_{DD} = 2.7V	0.4	4.2	MHz
			V_{DD} = 4.5V		6.0	
	fs	XTIN, XTOUT		30.0	34.0	kHz

Note. Input Voltage V_{IH3}, V_{IL3} ; in the SLOW and HOLD mode.
fc ; High-frequency clock [Hz]
fs ; Low-frequency clock [Hz]

D.C. CHARACTERISTICS (V_{SS} = 0V, T_{opr} = – 40 to 70°C)

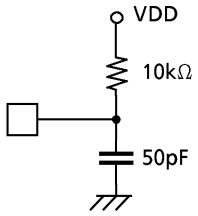
PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		—	0.7	—	V
Input Current	I_{IN1}	Port K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5V, V_{IN} = 5.5V / 0V	—	—	± 2	μA
	I_{IN2}	Open drain R port					
Low Level Input Current	I_{IL}	Push Pull R port	V_{DD} = 5.5V, V_{IN} = 0.4V	—	—	– 2	mA
Input Registance	R_{IN}	$\overline{RESET}$		100	220	450	kΩ
Output Leakage Current	I_{LO}	Open drain ports P, R	V_{DD} = 5.5V, V_{OUT} = 5.5V	—	—	2	μA
High Level Output Voltage	V_{OH}	Push Pull R port	V_{DD} = 4.5V, I_{OH} = – 200μA	2.4	—	—	V
Output Low Voltage	V_{OL2}	Except XOUT XTOUT and ports P1, P2	V_{DD} = 4.5V, I_{OL} = 1.6mA	—	—	0.4	V
Output Low Current	I_{OL1}	Ports P1, P2	V_{DD} = 4.5V, V_{OL} = 1.0V	—	10	—	mA
Segment Output Low Registance	R_{OS1}	SEG pin	V_{DD} = 5V, V_{DD} – V_{LC} = 3V	—	20	—	kΩ
Common Output Low Registance	R_{OC1}	COM pin					
Segment Output High Registance	R_{OS2}	SEG pin		—	200	—	
Common Output High Registance	R_{OC2}	COM pin					
Segment/Common Output Registance	$V_{O2/3}$	SEG / COM pin		3.8	4.0	4.2	V
	$V_{O1/2}$			3.3	3.5	3.7	
	$V_{O1/3}$			2.8	3.0	3.2	
Supply Current (in the Normal mode)	I_{DD}		V_{DD} = 5.5V, V_{LC} = V_{SS}, fc = 4MHz	—	3	6	mA
	I_{DDS}		V_{DD} = 3.0V, V_{LC} = V_{SS}, fc = 4MHz	—	1.5	—	
Supply Current (in the SLOW mode)	I_{DDH}		V_{DD} = 3.0V, V_{LC} = V_{SS}, fs = 32.768kHz	—	30	60	μA
Supply Current (in the HOLD mode)			V_{DD} = 5.5V	—	0.5	10	μA

Note 1. Typ. values show those at T_{opr} = 25°C, V_{DD} = 5V.
Note 2. Input Current I_{IN1} ; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.
Note 3. Output Resistance R_{os}, R_{oc} ; Shows on-resistance at the level switching.
Note 4. $V_{O2/3}$; Shows 2/3 level output voltage, when the 1/4 or 1/3 duty LCD is used.
Note 5. $V_{O1/2}$; Shows 1/2 level output voltage, when the 1/2 duty or static LCD is used.
Note 6. $V_{O1/3}$; Shows 1/3 level output voltage, when the 1/4 or 1/3 duty LCD is used.
Note 7. Supply Current I_{DD} ; V_{IN} = 5.3V/0.2V
The K0 port is open when the input resistor is contained.
The voltage applied to the R port is within the valid range.
Note 8. Supply Current I_{DDS} ; V_{IN} = 2.8V/0.2V. Only low frequency clock is only osillated (connecting XTIN, XTOUT).
Note 9. When using LCD, it is necessary to consider values of $R_{OS1/2}$ and $R_{OC1/2}$.
Note 10. Times for SEG / COM output switching on ;R_{OS1}, R_{OC1} : 2/fs (s)
R_{OS2}, R_{OC2} : 1/(n · f_F) (1/n : duty, f_F : frame frequency)

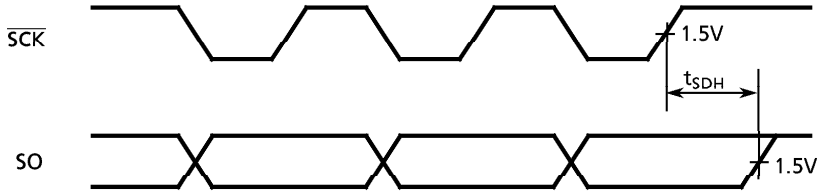
A.C. CHARACTERISTICS (V_{SS} = 0V, V_{DD} = 2.7 to 6.0V, T_{opr} = – 40 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Instruction Cycle Time	t_{cy}	in the Normal mode V_{DD} = 2.7V fc = 4.2MHz	1.9	—	20	μs
		in the Normal mode V_{DD} = 4.5V fc = 6.0MHz	1.3			
		in the SLOW mode	235	—	267	μs
High Level Clock Pulse Width	t_{WCH}	For external clock operation	80	—		ns
Low Level Clock Pulse Width	t_{WCL}					
Shift data Hold Time	t_{SDH}		$0.5t_{cy}$ – 300	—	—	ns
High Speed Timer/Counter input frequency	f_{HT}		—	—	fc	MHz

Note. Shift data Hold time :
External circuit for $\overline{SCK}$ pin and SO pin



Serial port (completion of transmission)



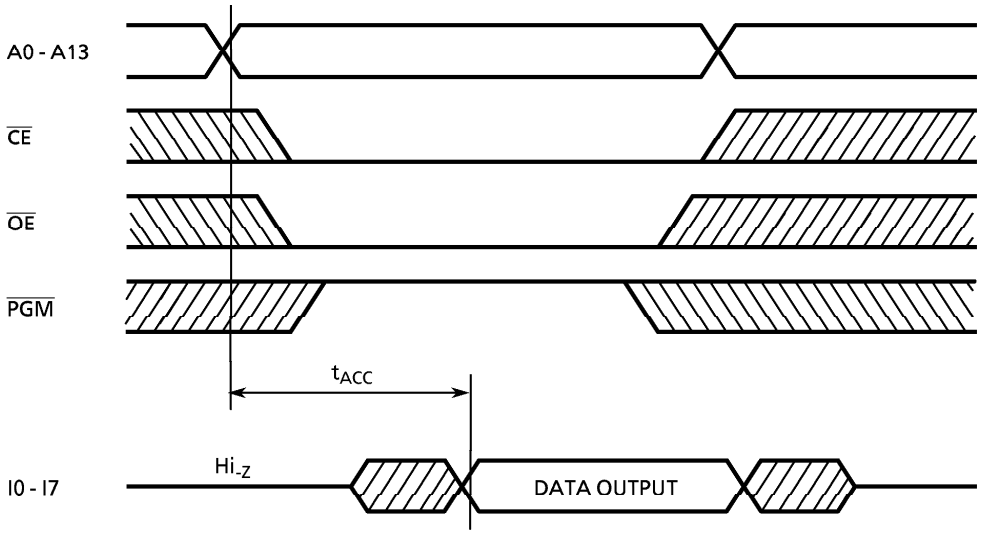
RECOMMENDED OSCILLATING CONDITIONS (V_{SS} = 0V, V_{DD} = 2.7 to 6.0V, T_{opr} = – 40 to 70°C)

Recommended oscillating conditions of the 47P1620 are equal to the 47C1620's.

D.C./A.C. CHARACTERISTICS (V_{SS} = 0V)

(1) Read Operation

PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Output Level High Voltage	V_{IH4}		V_{CC} × 0.7	–	V_{CC}	V
Output Level Low Voltage	V_{IL4}		0	–	V_{CC} × 0.1	V
Supply Voltage	V_{CC}		4.75	–	6.0	V
Programming Voltage	V_{PP}					
Address Access Time	t_{ACC}	V_{CC} = 5.0 ± 0.25V	–	–	350	ns



(2) High Speed Programming Operation

PARAMETER	SYBOL	CONDITION	Min.	Typ.	Max.	UNIT
Input High Voltage	V_{IH4}		$V_{CC} \times 0.7$	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.1$	V
Supply Voltage	V_{CC}		4.75	–	6.0	V
V_{PP} Power Supply Voltage	V_{PP}		12.0	12.5	13.0	V
Programming Pulse Width	t_{PW}	$V_{CC} = 6.0 \pm 0.25V$	0.95	1.0	1.05	ms