CMOS 4-BIT MICROCONTROLLER

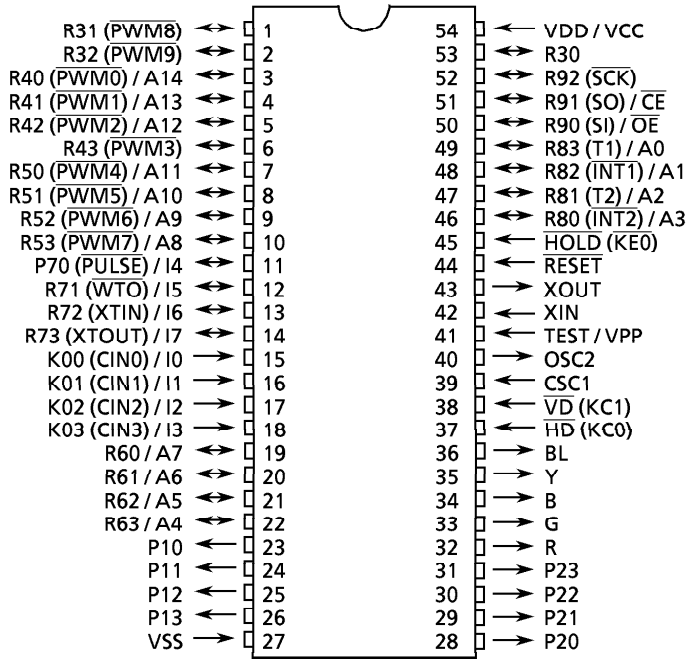
TMP47P1638VN

The 47P1638V is the OTP microcontroller with 128kbits PROM. For program operation, the programming is achieved by using with EPROM programmer (TMM27256AD type) and adaptor socket.
The function of this device is exactly same as the 47C1238A/1638A.

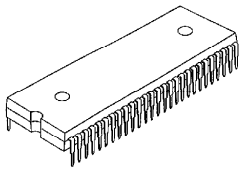
PART No.	ROM	RAM	PACKAGE	ADAPTOR SOCKET
TMP47P1638VN	OTP 16384 × 8-bit	512 × 4-bit	SDIP54-P-600-1.78	BM1169

PIN ASSIGNMENT (TOP VIEW)

SDIP54-P-600-1.78



SDIP54-P-600-1.78



TMP47P1638VN

PIN FUNCTION

The 47P1638V has MCU mode and PROM mode.

(1) MCU mode

The 47C1238A and the 47C1638A are pin compatible (TEST pin for out-going test. Be fixed to low level).

(2) PROM mode

PIN NAME	Input / Output	FUNCTIONS	PIN NAME (MCU mode)
A14 to A12	Input	Address inputs	R40 to R42
A11 to A8			R50 to R53
A7 to A4			R60 to R63
A3 to A0			R80 to R83
I7 to I4	I/O	Data Inputs / outputs	R73 to R70
I3 to I0			K03 to K00
$\overline{CE}$	Input	Chip Enable input	R91
$\overline{OE}$		Output Enable input	R90
VPP	Power supply	+ 12.5 V / 5 V (Program supply voltage)	TEST
VCC		+ 5 V	VDD
VSS		0 V	VSS
$\overline{HD}$, $\overline{VD}$	Input	Be fixed to low level	
R32 to R30	I/O	Open	
R43			
R92			
P13 to P10	Output		
P23 to P20			
BL, Y, R, G, B			
$\overline{RESET}$	Input	PROM mode setting pin. Be fixed to low level.	
$\overline{HOLD}$	Input		
XIN	Input	Resonator connecting pins	
XOUT	Output		
OSC 1	Input	Open	
OSC 2	Output		

OPERATIONAL DESCRIPTION

The following is an explanation of hardware configuration and operation in relation to the 47P1638V. The 47P1638V is the same as the 47C1238A/1638A except that an OTP is used instead of a built-in mask ROM.

1. OPERATION mode

The 47P1638V has an MCU mode and a PROM mode.

1.1 MCU mode

The MCU mode is set by fixing the TEST/VPP pin at the "L" level. Operation in the MCU mode is the same as the 47C1238A/1638A, except that the TEST/VPP pin does not have a built in pull-down resistor and cannot be used open.

1.1.1 Program Memory

The program storage area is the same as the 47C1638A.
When using the 47P1638V check 47C1238A operation, place data conversion tables at two locations.

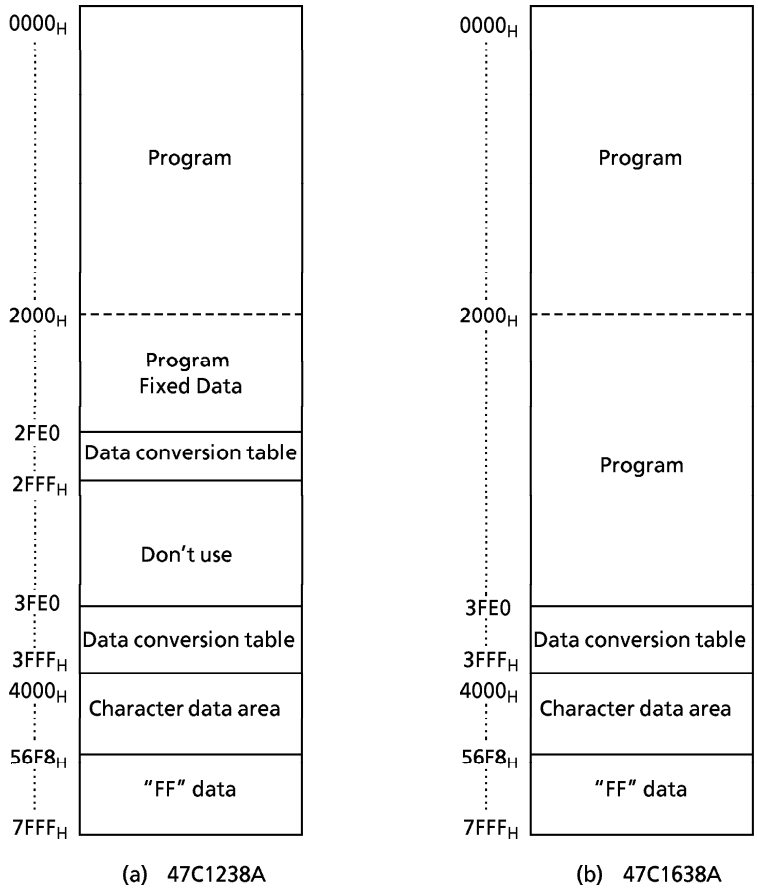


Figure 1-1. Program area

*Note. "FF" data have to be written in address "***9$_H$" to "***F$_H$" of character data area.*
And "1" data heve to be written in bit "7" of character data area.

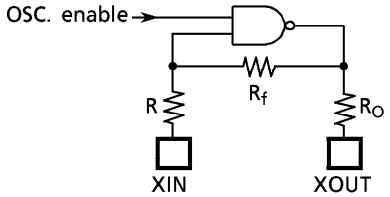
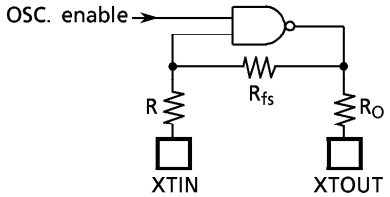
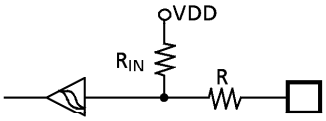
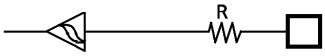
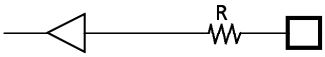
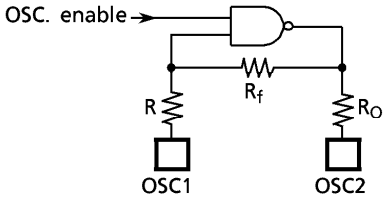
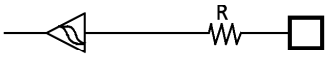
1.1.2 Data Memory

The 47P1638V has two built-in 256 × 4-bit data memory banks (DMB0, DMB1).

1.1.3 Input/Output Circuitry

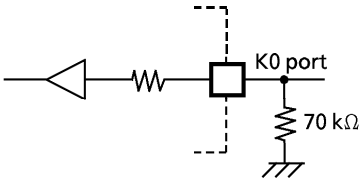
(1) Control pins

This is the same as for the 47C1238A/1638A except that there is no built in pull-down resistor for the TEST pin. Input/output circuitry of the 47P1638V control pins is shown below.

CONTROL PIN	I/O	CIRCUITRY	REMARKS
XIN XOUT	Input Output		Resonator connecting pins R = 1 kΩ (typ.) R_f = 1.5 MΩ (typ.) R_O = 2 kΩ (typ.)
XTIN XTOUT	Input Output		Resonator connecting pins (R = 1 kΩ typ.) (R_{fs} = 6 MΩ typ.) (R_O = 220 kΩ typ.)
$\overline{\text{RESET}}$	Input		Hysteresis input Contained pull-up resistor R_{IN} = 220 kΩ (typ.) R = 1 kΩ (typ.)
$\overline{\text{HOLD}}$ ($\overline{\text{KE0}}$)	Input (Input)		Hysteresis input (Sence input) R = 1 kΩ (typ.)
TEST	Input		Not contained pull-down resistor R = 1 kΩ (typ.)
OSC1 OSC2	Input Output		Oscillation terminals for OSD R = 1 kΩ (typ.) R_f = 1.5 MΩ (typ.) R_O = 2 kΩ (typ.)
$\overline{\text{HD}}$ $\overline{\text{VD}}$	Input		Synchronous signal input Hysteresis input R = 1 kΩ (typ.)

(2) I/O port

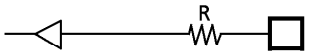
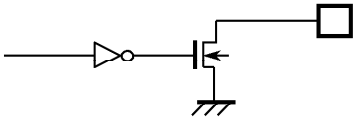
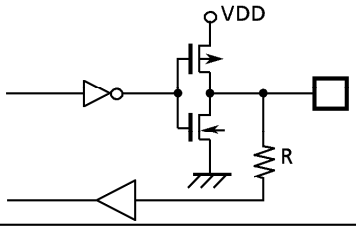
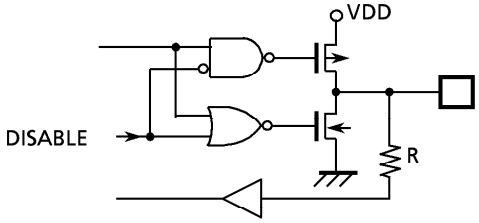
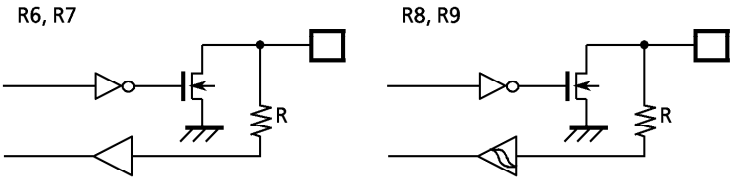
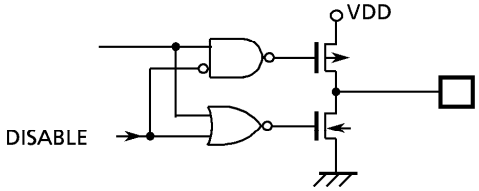
The input/output circuit of the 47P1638V is the same as I/O code PA of the 47C1238A/1638A. When this chip is used as evaluator with the I/O code, it is necessary to provide such as external resisters.



Pull-down resistor for code PC

Figure 1-2. Example of External Circuitry

The input / output circuitries of the 47P1638V I/O ports it as follows.

PORT	I/O	INPUT/OUTPUT CIRCUITRY (code : PA)	REMARKS
K0	Input		Not contained Pull-up or Pull-down resistor R = 1 kΩ (typ.)
P1 P2	Output		Sink open drain Initial "Hi-Z" High drive current I_{OL} = 20 mA (typ.)
R3	I/O		Push-pull output Initial "High" R = 1 kΩ (typ.)
R4 R5	I/O		Tri-state I/O Initial "Hi-Z" R = 1 kΩ (typ.)
R6 R7 R8 R9	I/O		Sink open drain Initial "Hi-Z" Hysteresis input (R8, R9) R = 1 kΩ (typ.)
R G B Y BL	Output		Tri-state output Initial "Hi-z"

1.2 PROM mode

The PROM mode is set by setting the $\overline{RESET}$, $\overline{HOLD}$, pins to the "L" level. The PROM mode can be used as a general-purpose PROM writer for program writing and verification. (A high-speed program mode is used set the ROM type the same as for the TMM 27256AD)

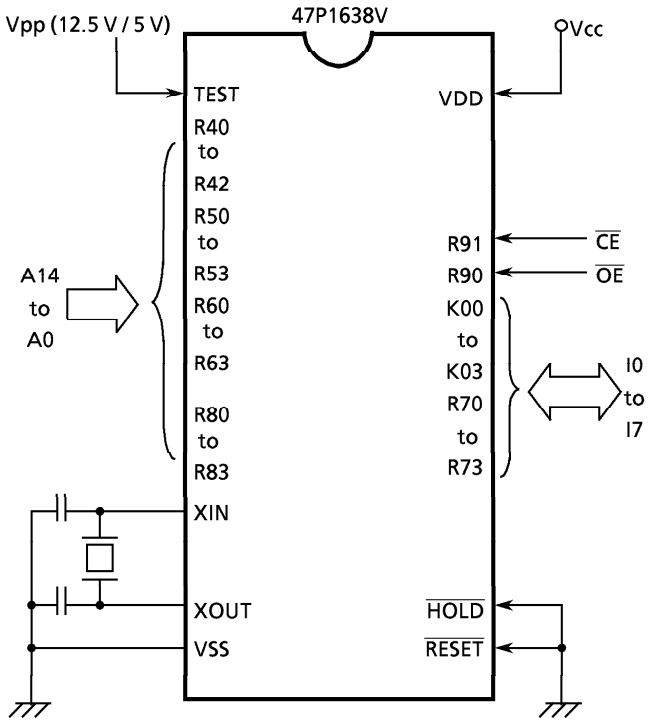


Figure 1-3. Setting for PROM mode

1.2.1 Programming flow chart (High-speed programming mode)

The high-speed programming mode is activated by applying the programming voltage of Vpp (12.5 V) under Vcc = 6 V. After addresses and input data are stable, the programming is performed by supplying 1ms of program pulse (single) to $\overline{CE}$ input. The data is verified by using Program Verify mode. If the program data is not correct, additional 1ms of program pulse is supplied until the programming operates correctly (max. 25 times). Further, program pulse with a pulse width 3 times that of required for programming (number of programming X 1 ms) is resupplied. This completes programming of one address.

Subsequently, repeat the same procedures by changing addresses and input data. When all programming has been ended, the data in all address should be verified under Vcc = Vpp = 5 V.

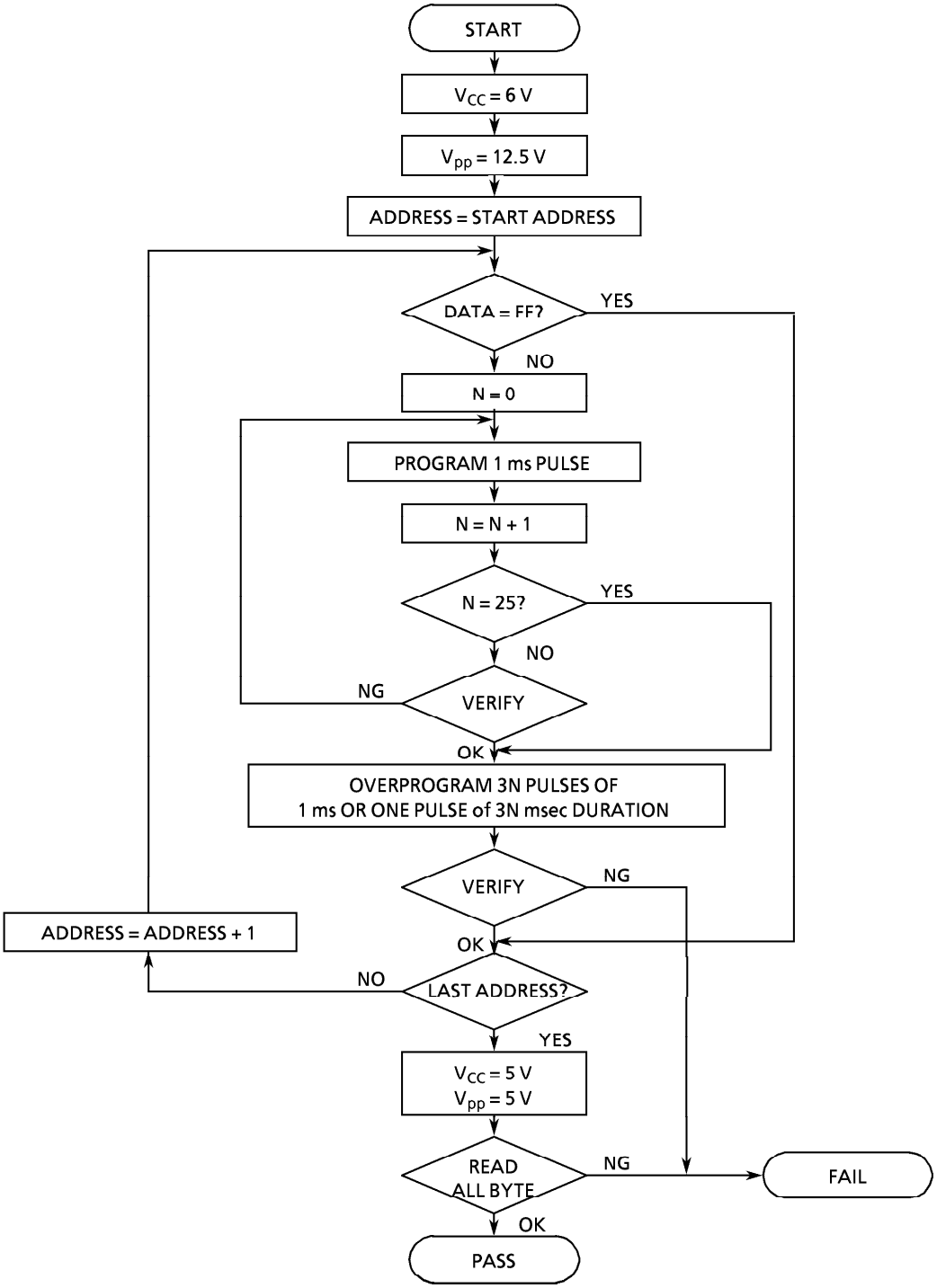


Figure1-4. FLOW CHART

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0 V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V_{DD}		– 0.3 to 7	V
Program Voltage	V_{pp}	TEST / VPP pin	– 0.3 to 14.0	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	Except sink open drain pin, R7 port	– 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	Sink open drain pin except R7 port	– 0.3 to 10	
Output Current (Per 1 pin)	I_{OUT1}	P1, P2 port	30	mA
	I_{OUT2}	R3, R6, R7, R8, R9 port	3.2	
Output Current (Total)	ΣI_{OUT1}	P1, P2 port	60	mA
Power Dissipation	PD		600	mW
Soldering Temperature (time)	T_{sld}		260 (10 s)	℃
Storage Temperature	T_{stg}		– 55 to 125	℃
Operating Temperature	T_{opr}		– 30 to 70	℃

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0 V, T_{opr} = – 30 to 70 °C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		in the Normal mode	4.5	6.0	V
			in the SLOW mode	2.7		
			in the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geqq 4.5$ V	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geqq 4.5$ V	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.1$	
Clock Frequency	fc	XIN, XOUT		0.4	6.0	MHz
	fs	XTIN, XTOUT		30.0	34.0	kHz
	f_{OSD}	OSC1, OSC2		–	8.0	MHz

Note. Input Voltage V_{IH3}, V_{IL3} : in the SLOW or HOLD mode

D.C. CHARACTERISTICS (VSS = 0 V, T_{opr} = − 30 to 70 °C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		—	0.7	—	V
Input Current	I_{IN1}	K0 port, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5 V, V_{IN} = 5.5 V / 0 V	—	—	± 2	μA
	I_{IN2}	R port (open drain)					
Input Low Current	I_{IL}	R port (push-pull)	V_{DD} = 5.5 V, V_{IN} = 0.4 V	—	—	− 2	mA
Input Resistance	R_{IN2}	$\overline{RESET}$		100	220	450	kΩ
Output Leakage Current	I_{LO}	Tri-state R3, R6, R8, R9 port (open drain)	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	—	—	± 2	μA
Output High Voltage	V_{OH1}	R port (push-pull)	V_{DD} = 4.5 V, I_{OH} = − 200 μA	2.4	—	—	V
	V_{OH2}	R port (tri-state), OSD output	V_{DD} = 4.5 V, I_{OH} = − 0.7 mA	4.1	—	—	
Output Low Voltage	V_{OL1}	R3, R6~R9 port	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	—	—	0.4	V
	V_{OL2}	R port (tri-state), OSD output	V_{DD} = 4.5 V, I_{OL} = 0.7 mA				
Output Low Current	I_{OL}	Ports P1, P2	V_{DD} = 4.5 V, V_{OL} = 1.0 V	—	20	—	mA
Supply Current (in the Nomal mode)	I_{DD}		V_{DD} = 5.5 V fc = 4 MHz	—	3	6	mA
Supply Current (in the SLOW mode)	I_{DDS}		V_{DD} = 3.0 V	—	30	60	μA
Supply Current (in the HOLD mode)	I_{DDH}		V_{DD} = 5.5 V	—	0.5	10	μA

Note 1. Typ. values show those at T_{opr} = 25 °C, VDD = 5 V.
Note 2. Input Current I_{IN1} : The current through resistor is not included, when the pull-up/pull-down resistor is contained.
Note 3. Supply Current
I_{DD}, I_{DDH} : V_{IN} = 5.3 V / 0.2 V
The K0 port is open when the pull-up / pull-down resistor is contained.
The voltage applied to the R port is within the valid range V_{IL} or V_{IH}.
I_{DDS} : V_{IN} = 2.8V / 0.2V
Low frequency clock is only oscillated (connecting XTIN, XTOUT) comparator function is disabled.

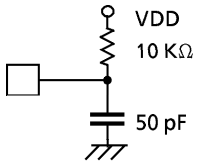
A / D CONVERSION CHARACTERRISTICS

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Analog Input Voltage	V_{AIN}	CIN3 to CIN0		V_{SS}	—	V_{DD}	V
A/D Conversion Error	–			—	—	$\pm\frac{1}{2}$	LSB

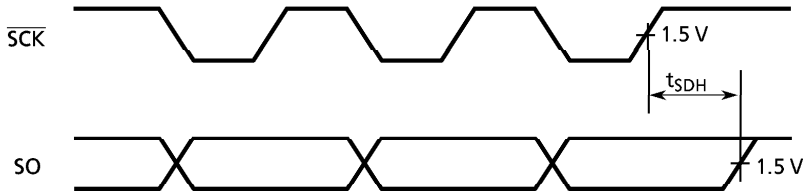
A.C. CHARACTERISTICS (V_{SS} = 0 V, V_{DD} = 4.5 to 6.0 V, T_{opr} = – 30 to 70 °C)

PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}	in the NORMAL mode	1.3	–	20	μs
		in the SLOW mode	235		267	
High level Clock Pulse Width	t_{WCH}	For external clock operation	80	–	–	ns
Low level Clock Pulse Width	t_{WCL}					
Shift Data Hold Time	t_{SDH}		0.5 t_{cy} – 300	–	–	ns

Note. Shift data Hold Time
External circuit for $\overline{SCK}$ pin and SO pin



Serial port (completion of transmission)



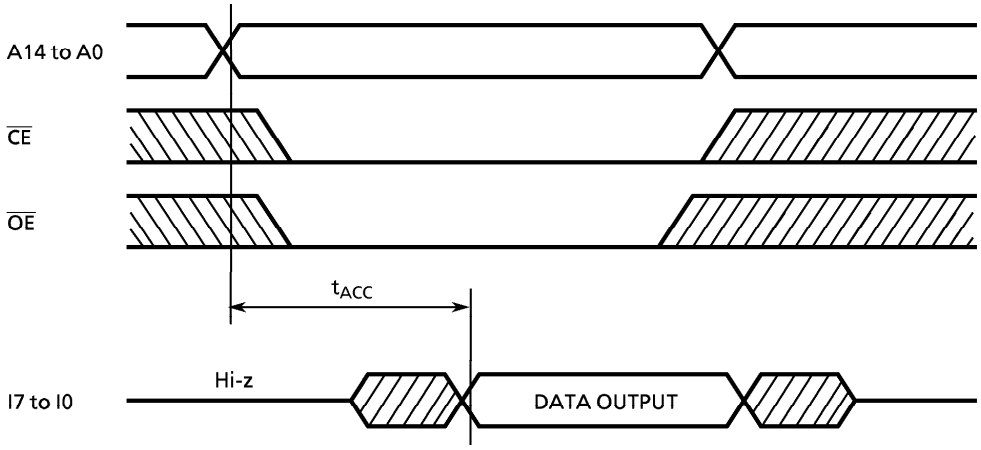
RECOMMENDED OSCILLATING CONDITIONS (V_{SS} = 0 V, V_{DD} = 4.5 to 6.0 V, T_{opr} = – 30 to 70 °C)

Recommended oscillating conditions of the 47P1638V are equal to those of the 47C1238A/1638A.

DC/AC CHARACTERISTICS (V_{SS} = 0 V)

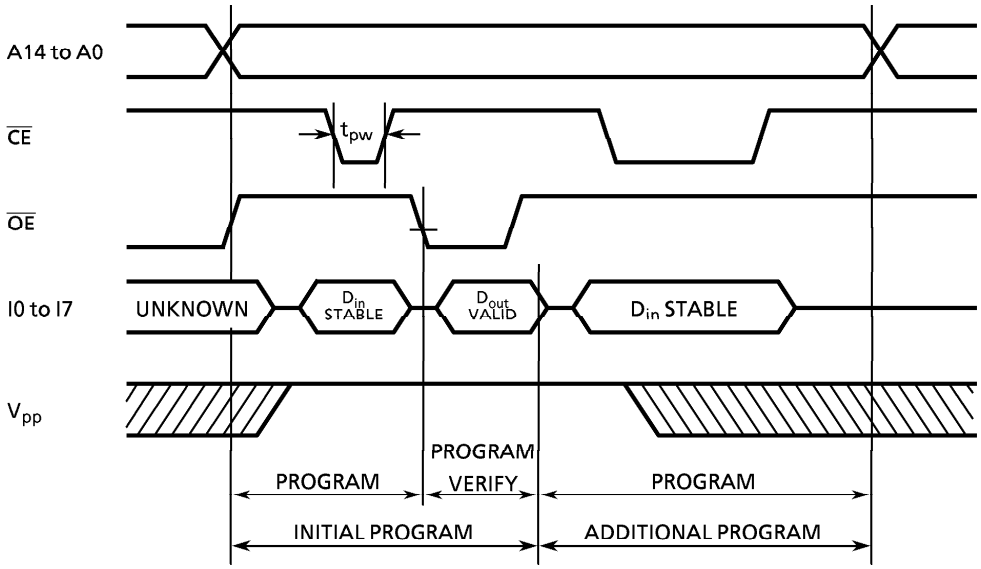
(1) Read Operation

PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Output Level High Voltage	V_{IH4}		V_{CC} × 0.7	–	V_{CC}	V
Output Level Low Voltage	V_{IL4}		0	–	V_{CC} × 0.3	V
Supply Voltage	V_{CC}		4.75	–	6.0	V
Programming Voltage	V_{PP}					
Address Access Time	t_{ACC}	V_{CC} = 5.0 ± 0.25 V	0	–	350	ns



(2) High Speed Programming Operation

PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Input High Voltage	V_{IH4}		$V_{CC} \times 0.7$	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.3$	V
Supply Voltage	V_{CC}		5.75	–	6.25	V
V_{PP} Power Supply Voltage	V_{PP}		12.25	12.5	12.75	V
Programming Pulse Width	t_{PW}	$V_{CC} = 6.0 \pm 0.25$ V	0.95	1.0	1.05	ms



Note : An electrical shield by metal shield plate on the surface of the IC package should be recommendable in order to prevent the device from the high electric fieldstress applied from CRT (Cathode Ray Tube) for continuous reliable operation.