CMOS 4-BIT MICROCONTROLLER

TMP47P1670VN

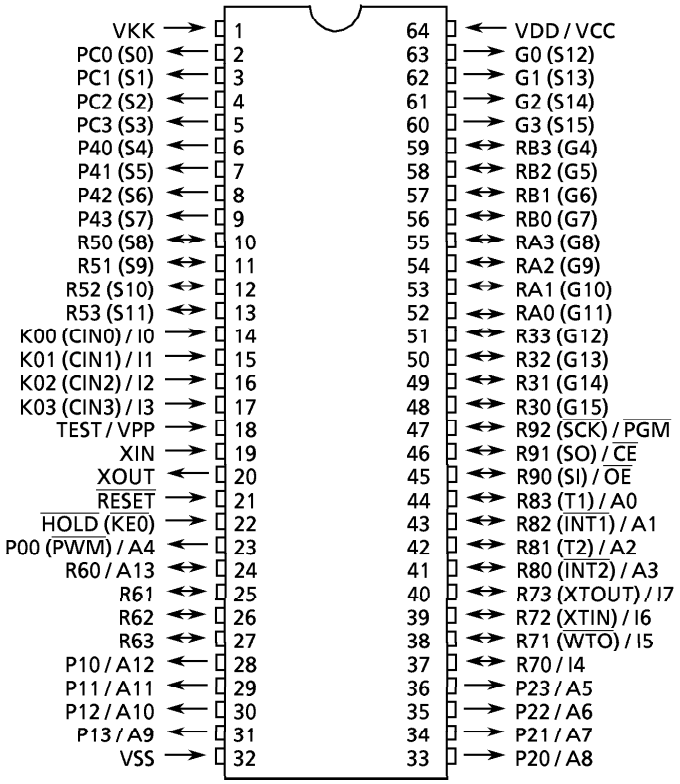
The 47P1670V is the system evaluation LSI of 47C1270 / 1670A with 128K bits one-time PROM. The 47P1670V programs / verifies using an adaptersocket to connect with PROM programmer, as it is in TMM27128AD.
In addition, the 47P1670V and the 47C1270 / 1670A are pin compatible. The 47P1670V operates as the same as the 47C1270 / 1670A by programming to the internal PROM.

.

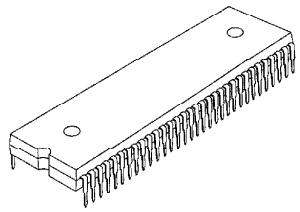
PART No.	ROM	RAM	PACKAGE	ADAPTER SOCKET
TMP47P1670VN	OTP 16384 × 8-bit	768 × 4-bit	SDIP64-P-750-1.78	BM1133

PIN ASSIGNMENT (TOP VIEW)

SDIP64-P-750-1.78



SDIP64-P-750-1.78



TMP47P1670VN

PIN FUNCTION

The 47P1670V has MCU mode and PROM mode.

(1) MCU mode
The 47C1270/1670 and the 47P1670V are pin compatible (TEST pin for out-going test. Be fixed to low level.).

(2) PROM mode

PIN NAME	INPUT/OUTPUT	FUNCTIONS	PIN NAME (MCU MODE)
A13	Input	Address inputs	R60
A12 - A9			P10 - P13
A8 - A5			P20 - P23
A4			P00
A3 - A0			R80 - R83
I7 - I4	I/O	Data outputs/inputs	R73 - R70
I3 - I0			K03 - K00
$\overline{PGM}$	Input	Program control input	R92
$\overline{CE}$		Chip Enable input	R91
$\overline{OE}$		Output Enable input	R90
VPP	Power supply	+ 12.5V / 5V (Program supply voltage)	TEST
VCC		+ 5V	VDD
VSS		0V (GND)	VSS
P43 - P40	Output	Open	
PC3 - PC0			
G3 - G0			
R33 - R30	I/O		
R53 - R50			
RA3 - RA0			
RB3 - RB0			
R63 - R61		Be fixed to low level.	
$\overline{RESET}$	Input	PROM mode setting pins. Be fixed to low level.	
$\overline{HOLD}$	Input		
XIN	Input	Resonator connecting pins	
XOUT	Output		
VKK	Power supply	Be fixed to low level.	

OPERATIONAL DESCRIPTION

The following is an explanation of hardware configuration and operation in relation to the 47P1670V.
The 47P1670V is the same as the 47C1270/1670 except that an OTP is used instead of a Mask ROM.

1. OPERATION MODE

The 47P1670V has an MCU mode and a PROM mode.

1.1 MCU mode

The MCU mode is set by fixing the TEST/VPP pin at the "L" level. Operation in the MCU mode is the same as for the 47C1270/1670, except that the TEST/VPP pin does not have pull-down resistor and cannot be used open.

1.1.1 Program Memory

The program storage area is the same as for the 47C1670. Data conversion tables must be set in two locations when using the 47P1670V to check 47C1270 operation.

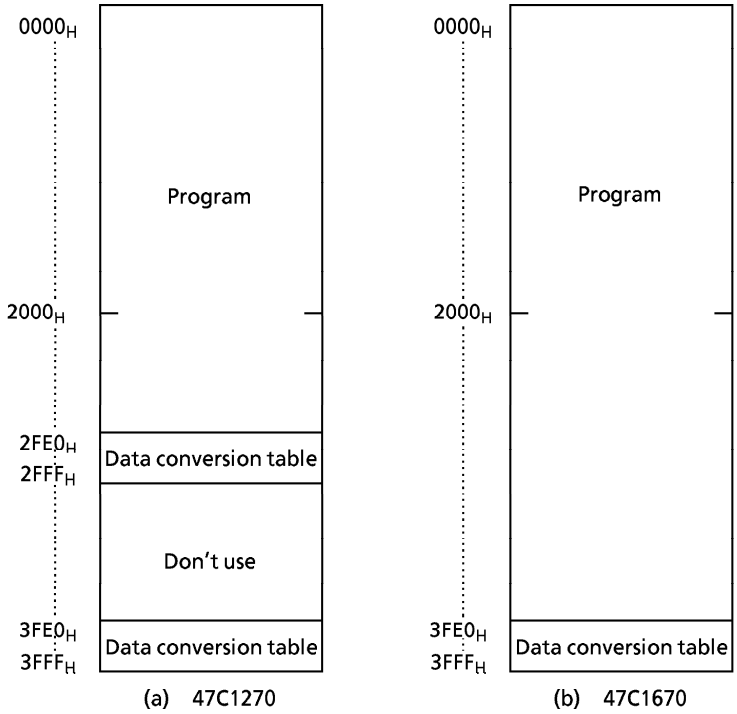


Figure 1-1. Program Area

1.1.2 Data Memory

The 47P1670V has 768 × 4 bits of data memory (RAM), 256 × 4 bits (addresses 00_H through FF_H) on each of banks (bank0, bank1 and bank2).

1.1.3 Input/Output Circuitry

(1) Control pins
This is the same as for the 47C1270/1670 except that there is no built in pull-down resistor for the TEST pin.

(2) I/O port
The input/output circuit of the 47P1670V is the same as I/O code MA of the 47C1270/1670.
External resistor, for example, is required when using as evaluator of other codes (MB, MC), (Refer to Figure1-2).

(a) Equivalent to I/O code MB (b) Equivalent to I/O code MC

Figure 1-2. I/O Code and External Circuitry

1.2 PROM mode

The PROM mode is set by setting the $\overline{RESET}$, $\overline{HOLD}$ pins to the "L" level. The PROM mode can be used as a general-purpose PROM writer for program writing and verification (A high-speed program mode is used set the ROM type the same as for the TMM27128AD).

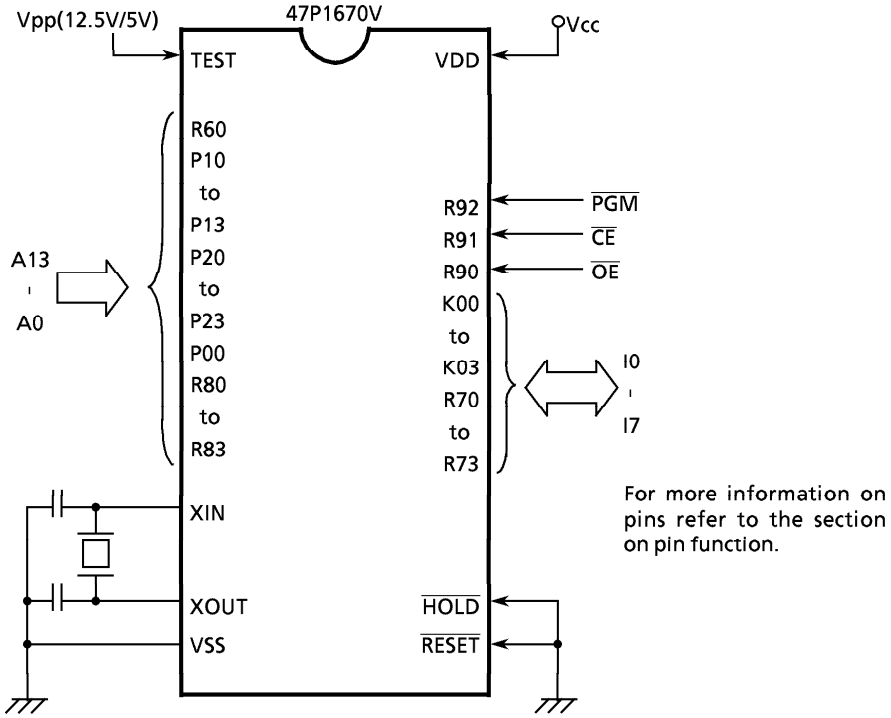


Figure 1-3. Setting for PROM Mode

An adapter socket is available for connecting a PROM writer.

- BM1133 : TMP47P1670VN

1.2.1 High Speed Programming Mode

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+ 12.5V) is applied to the V_{PP} terminal with V_{CC} = 6V and $\overline{PGM}$ = V_{IH}.

The programming is achieved by applying a single low level 1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, one additional program pulse with pulse width 3 times that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with V_{CC} = V_{PP} = 5V.

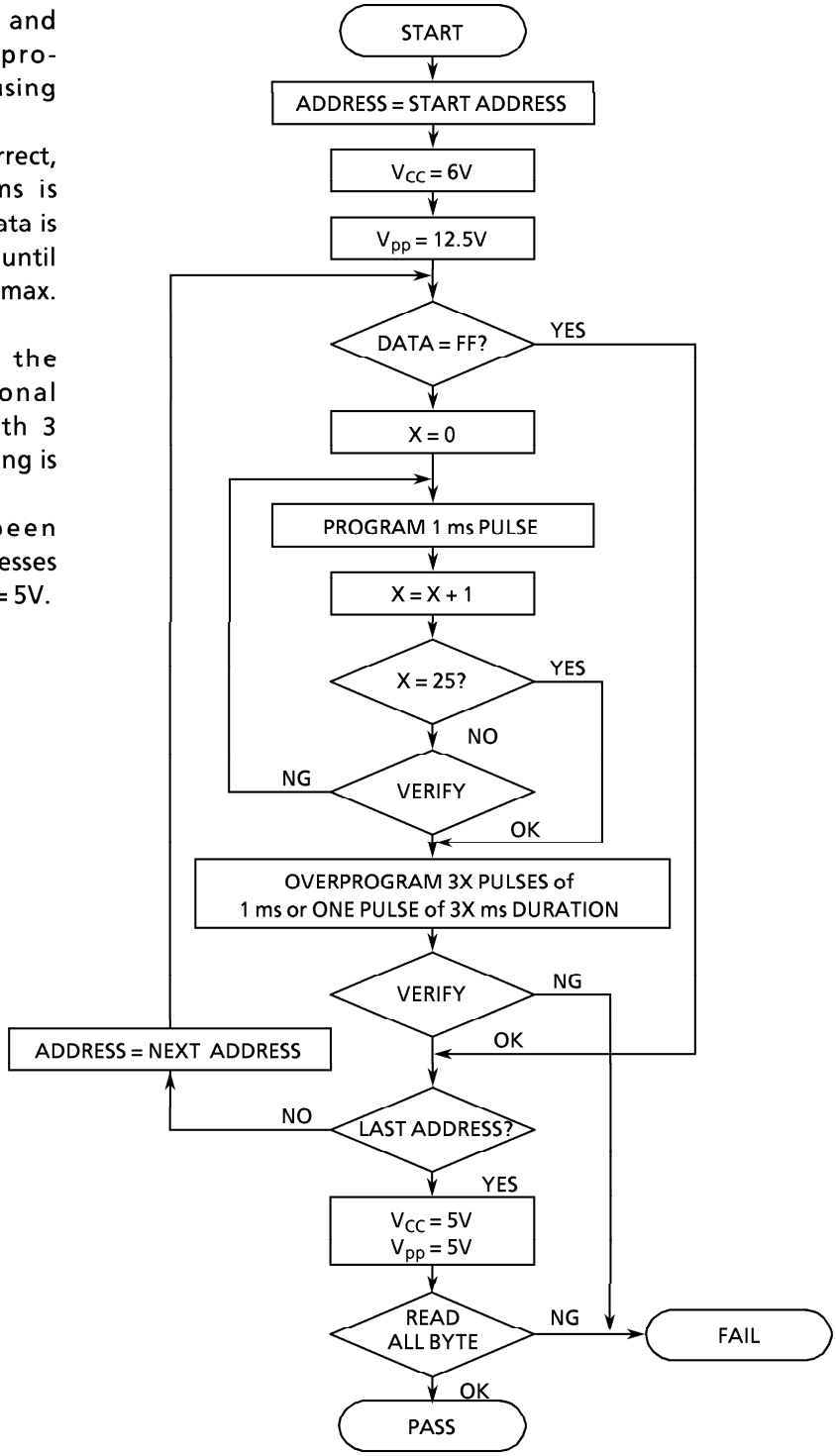


Figure 1-4. Flow Chart

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V_{DD}		– 0.3 to 7	V
Program Voltage	V_{PP}	TEST / VPP pin	– 0.3 to 14.0	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	R7, XOUT	– 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	Ports P0-P2, R6, R8, R9	– 0.3 to 10	
	V_{OUT3}	Source open drain ports	– 35 to V_{DD} + 0.3	
Output Current (per 1 pin)	I_{OUT1}	Ports P1, P2	30	mA
	I_{OUT2}	Ports P0, R6-R9	3.2	
	I_{OUT3}	Ports P4, R5, PC	– 12	
	I_{OUT4}	Ports R3, RA, RB, G / S	– 25	
Output Current (total)	ΣI_{OUT1}	Ports P1, P2	120	mA
	ΣI_{OUT3}	Ports P4, R5, PC	– 80	
	ΣI_{OUT4}	Ports R3, RA, RB, G / S	– 100	
Power Dissipation [T_{opr} = 70℃]	PD		600	mW
Soldering Temperature (time)	T_{sld}		260 (10 s)	℃
Storage Temperature	T_{stg}		– 55 to 125	℃
Operating Temperature	T_{opr}		– 40 to 70	℃

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, Topr = – 40 to 70℃)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		In the Normal mode	4.5	6.0	V
			In the SLOW mode	2.7		
			In the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5V$	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5V$		$V_{DD} \times 0.1$	
Clock Frequency	fc	XIN, XOUT	High-freq.clock	0.4	6.0	MHz
	fs	XTIN, XTOUT	Low-freq.clock	30.0	34.0	kHz

Note. Input Voltage V_{IH3}, V_{IL3} : in the SLOW operation or HOLD operation

D.C. CHARACTERISTICS (V_{SS} = 0V, T_{opr} = – 40 to 70℃)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis input		—	0.7	—	V
Input Current	I_{IN1}	Port K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5V V_{IN} = 5.5V / 0V	—	—	± 2	μA
	I_{IN2}	Ports R (open drain)					
Input Resistance	R_{IN2}	$\overline{RESET}$		100	220	450	kΩ
Pull-down Resistance	R_K	Source open drain	V_{DD} = 5.5V, V_{KK} = – 30V	—	80	—	kΩ
Output Leakage Current	I_{LO1}	Sink open drain ports	V_{DD} = 5.5V, V_{IN} = 5.5V	—	—	2	μA
	I_{LO2}	Source open drain ports	V_{DD} = 5.5V, V_{OUT} = – 32V	—	—	– 2	μA
Output Level High Voltage	V_{OH}	Ports P4, R5, PC	V_{DD} = 4.5V, I_{OH} = – 5mA	2.4	—	—	V
Output Level Low Voltage	V_{OL}	Ports P0, R6 - R9	V_{DD} = 4.5V, I_{OL} = 1.6mA	—	—	0.4	
High Level Output Current	I_{OH}	Ports R3, RA, RB, G / S	V_{DD} = 4.5V, V_{OL} = 2.4V	—	– 15	—	mA
Low Level Output Current	I_{OL}	Ports P1, P2	V_{DD} = 4.5V, V_{OL} = 1.0V	—	20	—	
Supply Current (in the Normal mode)	I_{DD}		V_{DD} = 5.5V fc = 4MHz	—	3	6	mA
Supply Current (in the SLOW mode)	I_{DDS}		V_{DD} = 3.0V fs = 32.768kHz	—	30	—	μA
Supply Current (in the HOLD mode)	I_{DDH}		V_{DD} = 5.5V	—	0.5	10	μA

Note 1. Typ. values show those at T_{opr} = 25℃, V_{DD} = 5V.

Note 2. Input Current I_{IN1} ; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

Note 3. I_{DD}, I_{DDH}; V_{IN} = 5.3V / 0.2V
The voltage applied to the R port is within the valid range.
I_{DDS}; V_{IN} = 2.8V / 0.2V, low frequency clock is only oscillated (connecting XTIN, XTOUT).
The comparator input is disable. The current through pull-down resistor of source open drain port is not included.

A / D CONVERSION CHARACTERISTICS (V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = – 40 to 70℃)

PARAMETER	SYMBOL	TERMINALS	Min.	Typ.	Max.	UNIT
Analog Input Voltage Range	V_{AIN}	CIN3 - CIN0	V_{SS}	—	V_{DD}	V
Error			—	—	$\pm\frac{1}{2}$	LSB

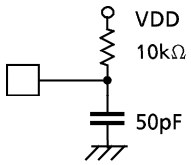
A.C. CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = – 40 to 70℃)

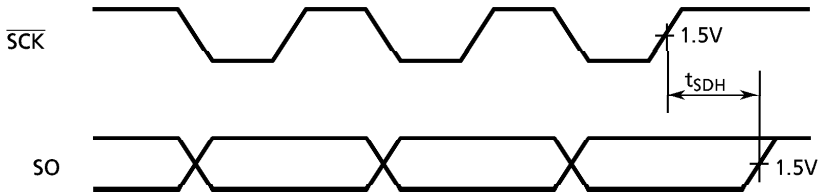
PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}	In the Normal mode	1.33	–	20	μs
		In the SLOW mode	235	–	267	
High Level Clock Pulse Width	t_{WCH}	For external clock operation	80	–	–	ns
Low Level Clock Pulse Width	t_{WCL}					
Shift Data Hold Time	t_{SDH}		$0.5t_{cy}$ – 300	–	–	ns

Note. Shift Data Hold Time:

External circuit $\overline{SCK}$ pin and SO pin



Serial port (completion of transmission)



RECOMMENDED OSCILLATING CONDITIONS

(V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = – 40 to 70℃)

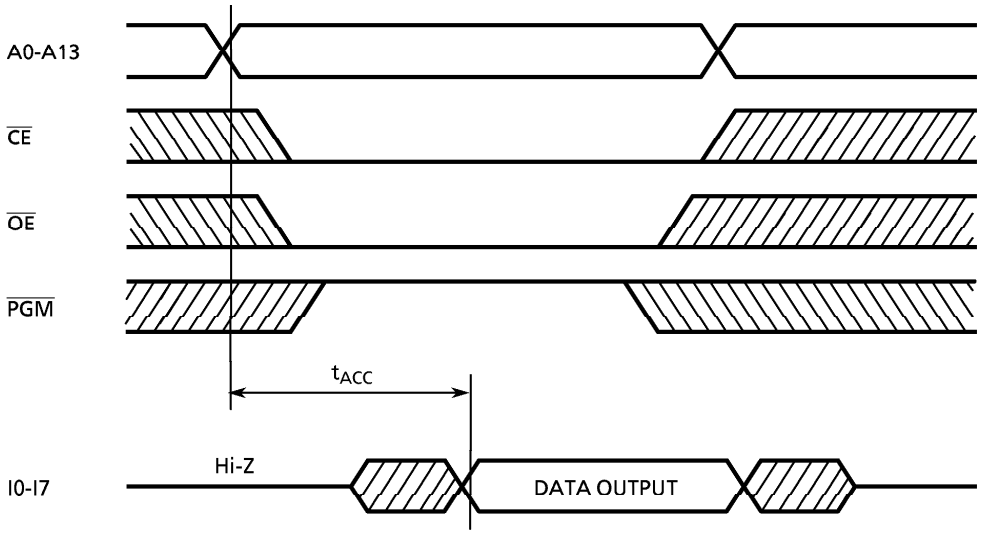
Recommended oscillating conditions of the 47P1670V are equal to the 47C1670's.

D.C./A.C. CHARACTERISTICS

(V_{SS} = 0V)

(1) Read Operation

PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Input High Voltage	V_{IH4}		V_{CC} × 0.7	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	V_{CC} × 0.3	V
Supply Voltage	V_{CC}		4.75	–	6.0	V
Programming Voltage	V_{PP}					
Address Access Time	t_{ACC}	V_{CC} = 5.0 ± 0.25V	0	–	350	ns



(2) High Speed Programming Operation

PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Input High Voltage	V_{IH4}		$V_{CC} \times 0.7$	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.3$	V
Supply Voltage	V_{CC}		4.75	–	6.0	V
Programming Voltage	V_{PP}		12.25	12.50	12.75	V
Initial Programming Pulse Width	t_{PW}	$V_{CC} = 6.0 \pm 0.25V$	0.95	1.0	1.05	ms