QUALITY SEMICONDUCTOR, INC.

Guaranteed Low Skew 3.3V CMOS Clock Driver/Buffer

QS53807
QS532807

FEATURES/BENEFITS

- JEDEC compatible LVTTL level
- 10 low skew clock outputs
- Clock input is 5V tolerant
- Pinout and function compatible with QS5807
- QS532807 has 25Ω on-chip resistors for low noise
- Input hysteresis for better noise margin
- Guaranteed low skew
  – 0.35ns same transition
  – 0.6ns opposite transition
  – 0.75ns different devices
- Industrial temperature range
- Available in QSOP (Q) and SOIC (SO)

DESCRIPTION

The QS53807 and QS532807 clock driver/buffer circuits can be used for clock buffering schemes where low skew is a key parameter. The QS53806 offers ten non-inverting outputs. Designed in QSI's proprietary QCMOS process, these devices provide low propagation delay buffering with on-chip skew of 0.35ns for same-transition, same-bank signals. The QS532807 has on-chip series termination resistors for lower noise clock signals. The series resistor versions are recommended for driving unterminated lines with capacitive loading and other noise sensitive clock distribution circuits. These clock buffer products are designed for use in high-performance workstations, embedded and personal computing systems. Several devices can be used in parallel or scattered throughout a system for guaranteed low skew, system-wide clock distribution networks. See Application Note AN-21 for more information on low-skew clock buffers.

Figure 1. Functional Block Diagram

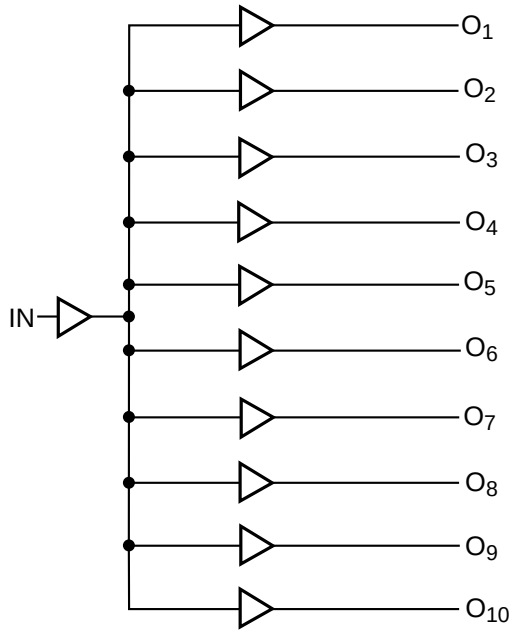


Figure 2. Pin Configurations (All Pins Top View)

QSOP, SOIC

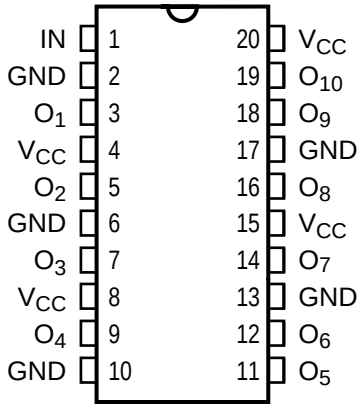


Table 1. Pin Description

Name	I/O	Description
IN	I	Clock Input
Ox	O	Clock Outputs

Table 2. Absolute Maximum Ratings

Supply Voltage to Ground ..... –0.5V to 4.6V
DC Output Voltage V_{OUT} ..... –0.5V to V_{CC} + 0.5V
DC Input Voltage V_{IN} ..... –0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20ns) ..... –3.0V
DC Input Diode Current with V_{IN} < 0 ..... –20mA
DC Output Current Max. Sink Current/Pin 120mA
Maximum Power Dissipation At T_A=85°C, QSOP ..... 0.82 watts
SOIC ..... 0.75 watts
T_{STG} Storage Temperature ..... –65° to 150°C

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to QSI devices that result in functional or reliability type failures.

Table 3. Capacitance

T_A = 25°C, f = 1MHz, V_{IN} = 0V

Pins	QSOP		SOIC		Unit
	Typ	Max	Typ	Max	
C_{IN}	3	6	5	7	pF

Note: Capacitance is characterized but not tested.

Table 4. DC Electrical Characteristics Over Operating Range

Industrial: T_A = –40°C to 85°C, V_{CC} = 3.3 ± 0.3V

Symbol	Parameter	Test Conditions	Min	Typ[1]	Max	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Inputs	2.0	1.7	5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Inputs	–0.5	—	0.8	
V_{IC}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA[3]	—	–0.7	–1.2	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –100µA	V_{CC}-0.2	—	—	
		V_{CC} = Min., I_{OH} = –8mA	2.4	—	—	
V_{OL}	Output LOW Voltage QS53807	V_{CC} = Min., I_{OL} = 100µA	—	—	0.2	
		V_{CC} = Min., I_{OL} = 16mA	—	—	0.4	
		V_{CC} = Min., I_{OL} = 24mA	—	—	0.5	
V_{OL}	Output LOW Voltage QS532807	V_{CC} = Min., I_{OL} = 100µA	—	—	0.2	
		V_{CC} = Min., I_{OL} = 6mA	—	—	0.4	
		V_{CC} = Min., I_{OL} = 8mA	—	—	0.5	
$\lvert I_{IN} \rvert$	Input Leakage Current	$0 \le V_{IN} \le 5.5V$	—	—	1	µA
I_{OS}	Short Circuit Current[2,3]	V_{CC} = Max., V_{OUT} = GND	–60	–195	—	mA
$\lvert I_{ODH} \rvert$	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V	–50	–80	–200	mA
$\lvert I_{ODL} \rvert$	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V	50	112	200	mA
ΔV_T	Input Hysteresis	V_{TLH} - V_{THL} for All Inputs	—	0.2	—	V
R_{OUT}	Output Resistance[4] QS532807	V_{CC} = Min.	—	28	—	Ω

Notes:
1. Typical values indicate V_{CC} = 3.3V and T_A = 25°C.
2. Not more than one output should be used to test this high power condition, and the duration is ≤ 1 second.
3. Guaranteed by design but not production tested.
4. Output resistance represents the total output impedence of the logic device and includes added series termination resistance.

Table 5. Power Supply Characteristics

Symbol	Parameter	Test Conditions[1]		Typ[3]	Max	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.,V_{IN} = GND or V_{CC}		0.01	100	uA
ΔI_{CC}	Supply Current per Input HIGH	V_{CC} = Max., V_{IN} = 3.0V Input toggling @ 50% duty cycle		0.1	30	uA
I_{CCD}	Dynamic Power Supply Current Per Output[2]	V_{CC} = Max., outputs enabled		60	90	uA/ MHz
I_C	Total Power Supply[2,4] Current	V_{CC} = Max., Input @ 50% duty cycle, f_I = 10MHz	V_{IN} = V_{CC} or V_{IN} = GND	6.0	10	mA
		V_{CC} = Max., Input @ 50% duty cycle, f_I = 2.5MHz	V_{IN} = V_{CC} or V_{IN} = GND	1.5	3.0	

Notes:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Guaranteed but not production tested. C_L=0pF.
3. Typical values are for reference only. Conditions are V_{CC} = 3.3V and T_A = 25°C.
4. $I_C = I_{CC} + (\Delta I_{CC})(D_H)(N_T) + I_{CCD}(f_O)(N_O)$
   where:
   D_H = Input duty cycle
   N_T = Number of TTL HIGH inputs at D_H (one)
   f_O = Output Frequency
   N_O = Number of outputs at f_O (ten)

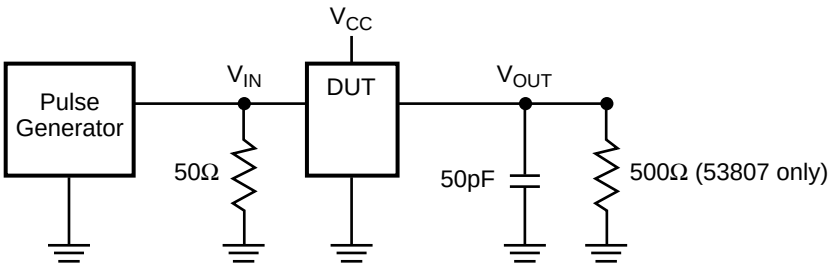
Table 6. Switching Characteristics Over Operating Range

Industrial: T_A = –40°C to 85°C, V_{CC} = 3.3 ± 0.3V
For QS53807, C_{LOAD} = 50pF, R_{LOAD} = 500Ω.
For QS532807, C_{LOAD} = 50pF (no resistor)

Symbol	Description[1]		— Min	— Max	A Min	A Max	Unit
$t_{SK(01)}$	Skew between outputs – same transition		—	0.5	—	0.35	ns
$t_{SK(p)}$	Pulse Skew: Skew between opposite transitions of the same output (t_{PHL}-t_{PLH})		—	0.5	—	0.35	
$t_{SK(t)}$	Part-to-part skew[2]		—	1.0	—	0.75	
t_{PLH} t_{PHL}	Propagation Delay[3] IN to Ox	QS53807	1.5	4.8	1.5	4.3	
		QS532807	1.5	5.2	1.5	4.8	
t_R	Output Rise Time, 0.8V to 2.0V	QS53807	—	1.5	—	1.5	
		QS532807	—	2.0	—	2.0	
t_F	Output Fall Time, 2.0V to 0.8V	QS53807	—	1.5	—	1.5	
		QS532807	—	2.0	—	2.0	

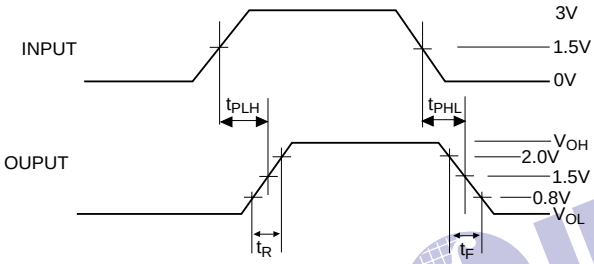
Notes:
1. Skew parameters are guaranteed but not production tested. See Test Circuit and Waveforms. Minimums guaranteed but not tested.
2. $t_{SK(t)}$ only applies to devices of the same transition, part type, temperature, power supply voltage, loading, package and speed grade.
3. The propagation delay range indicated by Min. and Max. specifications results from process and environmental variables. These propagation delay limits do not imply skew.

Figure 3. Test Circuits and Waveforms

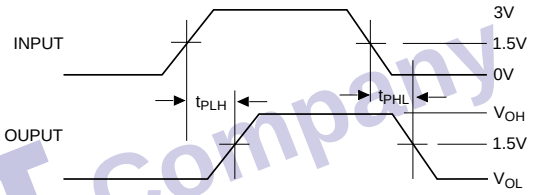


Pulse generator for all pulses: $f \leq 1.0MHz$; $t_F \leq 2.5ns$; $t_R \leq 2.5ns$

Test Circuit

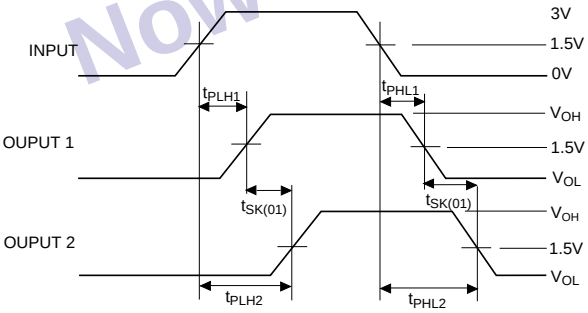


Propagation Delay



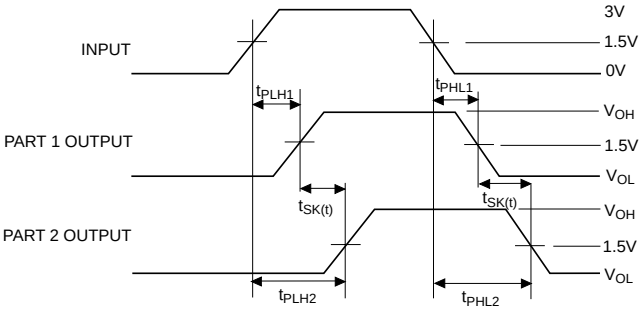
$t_{SK(p)} = |t_{PHL} - t_{PLH}|$

Pulse Skew - $t_{SK(p)}$



$t_{SK(O1)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

Output Skew - $t_{SK(01)}$



$t_{SK(t)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

Part-to-Part Skew - $t_{SK(t)}$

Figure 3. Ordering Information
Example: