QUALITY SEMICONDUCTOR, INC.

Guaranteed Low Skew PECL-TTL Clock Driver/Buffer

QS5P807T
QS5P2807T

FEATURES/BENEFITS

- PECL clock input
- 10 TTL clock output,
- 25Ω on-chip resistors available for low noise
- Guaranteed low skew
  – 0.5ns same bank
  – 0.7ns opposite transition
  – 0.75ns different devices
- Industrial temperature range
- Available in QSOP (Q) and SOIC (SO)

DESCRIPTION

The QS5P807T clock driver/buffer circuits can be used for clock buffering schemes where low skew is a key parameter. The QS5P807T generates ten TTL outputs from a pair of differential PECL (pseudo emitter couple logic) inputs. Designed in QSI's proprietary QCMOS process, these devices provide low propagation delay buffering with on-chip skew of 0.5ns for same-transition, same-bank signals. The QS5P2807T has on-chip series termination resistors for lower noise clock signals. The series resistor versions are recommended for driving unterminated lines with capacitive loading and other noise sensitive clock distribution circuits. These clock buffer products are designed for use in high-performance workstations, embedded and personal computing systems. Several devices can be used in parallel or scattered throughout a system for guaranteed low skew, system-wide clock distribution networks. See Application Note AN-21 for more information on low-skew clock buffers.

Figure 1. Functional Block Diagram

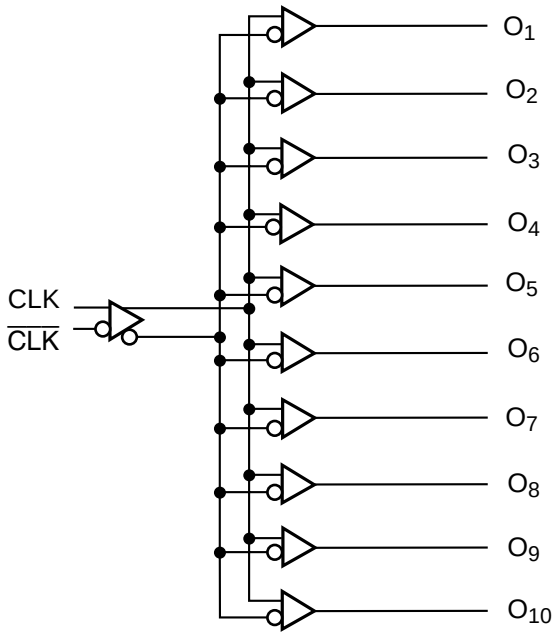


Figure 2. Pin Configurations (All Pins Top View)

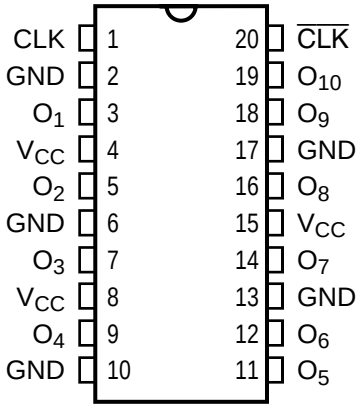


Table 1. Pin Description

Name	I/O	Description
CLK	I	Clock Input (True PECL reference clock input)
$\overline{CLK}$	I	Clock Input (Compliment PECL reference clock input)
Ox	O	Clock Outputs

Table 2. Absolute Maximum Ratings

Supply Voltage to Ground ..... –0.5V to 7.0V
DC Output Voltage V_{OUT} ..... –0.5V to 7.0V
DC Input Voltage V_{IN} ..... –0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20ns) ..... –3.0V
DC Input Diode Current with $V_{IN} < 0$ ..... –20mA
DC Output Current Max. Sink Current/Pin 120mA
Maximum Power Dissipation At T_A=85°C, QSOP ..... 0.82 watts
SOIC ..... 0.75 watts
T_{STG} Storage Temperature ..... –65° to 150°C

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to QSI devices that result in functional or reliability type failures.

Table 3. Capacitance

T_A = 25°C, f = 1MHz, V_{IN} = 0V

Pins	QSOP		SOIC		Unit
	Typ	Max	Typ	Max	
C_{IN}	4	6	5	7	pF

Note: Capacitance is characterized but not tested.

Table 4. DC Electrical Characteristics Over Operating Range

Industrial: T_A = –40°C to 85°C, V_{CC} = 5.0V ±10%

Symbol	Parameter	Test Conditions		Min	Typ(1)	Max	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for PECL Inputs		V_{CC} –1.165	—	V_{CC} –0.87	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for PECL Inputs		V_{CC} –1.83	—	V_{CC} –1.475	V
V_{DIFF}	Input Voltage Differential	Required for Full Output Swing(3)		200	—	—	mV
V_{CM}	Common Mode Voltage	High Level(3)		V_{CC} –2.0	—	V_{CC} –0.6	V
$\lvert I_{IH} \rvert$	Input HIGH Current	$V_{IN} = V_{IH}$ (Max.)		—	—	5	µA
$\lvert I_{IL} \rvert$	Input LOW Current	$V_{IN} = V_{IL}$ (Min.)		—	—	5	µA
$\lvert I_{IN} \rvert$	Input Leakage Current	V_{IN} = 0V		—	—	5	µA
V_{OH}	Output HIGH Voltage QS5P807T	V_{CC} = Min.,V_{IN}=V_{IH} or V_{IL},	I_{OH} = –15mA	2.4	3.3	—	V
			I_{OH} = –32mA	2.0	3.0	—	
V_{OH}	Output HIGH Voltage QS5P2807T	V_{CC} = Min.,V_{IN}=V_{IH} or V_{IL}, I_{OH} = –8mA		2.4	3.3	—	V
V_{OL}	Output LOW Voltage QS5P807T	V_{CC} = Min.,V_{IN}=V_{IH} or V_{IL}, I_{OL} = 48mA		—	0.2	0.5	V
V_{OL}	Output LOW Voltage QS5P2807T	V_{CC} = Min.,V_{IN}=V_{IH} or V_{IL}, I_{OL} = 8mA		—	—	0.5	V
I_{OS}	Short Circuit Current(2,3)	V_{CC} = Max., V_{OUT} = GND		–60	—	–250	mA
R_{OUT}	Output Resistance(4) QS5P2807T	V_{CC} = Min., I_{OL} = 12mA		—	28	—	Ω

Notes:
1. Typical values indicate V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be used to test this high power condition and the duration is ≤1 second.
3. Guaranteed by design but not tested.
4. Output resistance represents the total output impedence of the logic device and includes added series termination resistance.

Table 5. Power Supply Characteristics

Industrial: T_A = –40°C to 85°C, V_{CC} = 5.0V ±10%

Symbol	Parameter	Test Conditions		Typ(1)	Max	Unit
I_{CC}	Quiescent Power Supply Current(2)	V_{CC} = Max., V_{DIFF} = 200mV, V_{CM} = V_{CC}-1.3V		15	30	mA
I_{CCD}	Dynamic Power Supply(2) Current Per Output	V_{CC} = Max. Outputs enabled		0.35	0.50	mA/ MHz
I_C	Total Power Supply(2,3) Current Examples	V_{CC} = Max.,	f_I = 10MHz	40	80	mA
			f_I = 2.5MHz	20	43	

Notes:

1. Typical values are for reference only. Conditions are V_{CC} = 5.0V and T_A = 25°C.
2. Guaranteed but not tested. C_L = 0pF, R_L = ∞.
3. $I_C = I_{CC} + I_{CCD} (f_O)(N_O)$
   f_O = Output frequency
   N_O = Number of outputs at f_O (ten)

Table 6. Skew Characteristics Over Operating Range

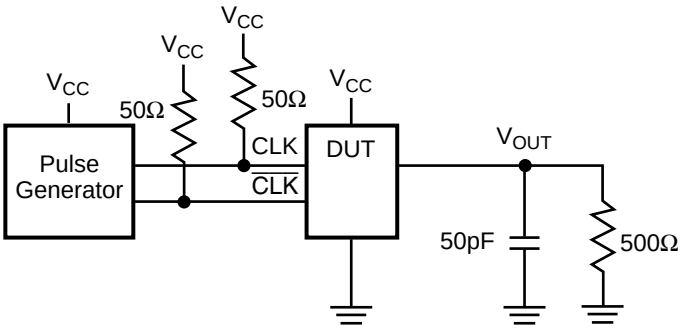
Industrial: T_A = –40°C to 85°C, V_{CC} = 5.0V ±10%
For QS5P807T, C_{LOAD} = 50pF, R_L = 500Ω
For QS5P2807T, C_{LOAD} = 50pF, (no resistor)

Symbol	Description(1,2)		—		A		B		C		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{SK(O1)}$	Skew between outputs of same transition		—	0.6	—	0.55	—	0.5	—	0.5	ns
$t_{SK(p)}$	Pulse Skew: Skew between opposite transitions of the same output (t_{PHL}-t_{PLH})	5P807T	—	0.6	—	0.55	—	0.5	—	0.5	ns
		5P2807T	—	0.8	—	0.8	—	0.75	—	0.7	
$t_{SK(t)}$	Part to part skew(3)		—	1.0	—	1.0	—	0.75	—	0.75	ns
t_{PLH} t_{PHL}	Propagation Delay(4) CLK to Ox	5P807T	1.5	6.5	1.5	6.0	1.5	5.5	1.5	5.0	ns
		5P2807T	1.5	7.0	1.5	6.5	1.5	6.0	1.5	5.5	
t_R, t_F	Output Rise and Fall Time		—	1.5	—	1.5	—	1.5	—	1.5	ns

Notes:

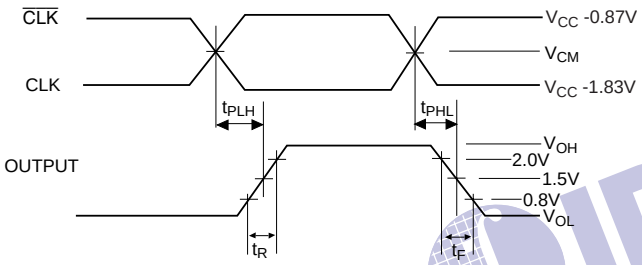
1. Skew parameters are guaranteed by characterization, but not production tested. Skew parameters apply to propagation delays only.
2. See Test Circuit and Waveforms.
3. $t_{SK(t)}$ only applies to devices of the same transition, same part type, same temperature, power supply voltage, loading, package and speed grade.
4. The propagation delay range indicated by Min. and Max. specifications results from process and environmental variables. These propagation delay limits do not imply skew.

Figure 3. Test Circuits and Waveforms

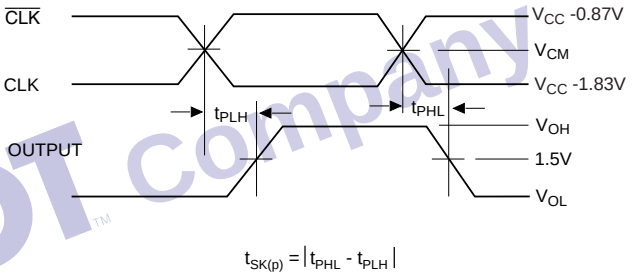


Pulse generator for all pulses: f ≤ 1.0MHz

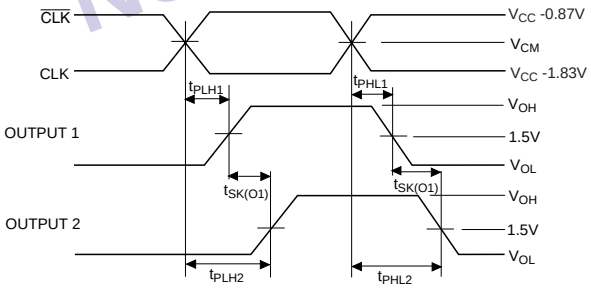
Test Circuit



Propagation Delay

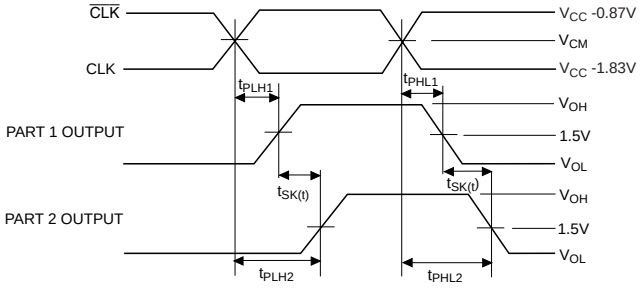


Pulse Skew - $t_{SK(p)}$



$t_{SK(O1)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

Output Skew - $t_{SK(O1)}$



$t_{SK(t)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

Part-to-Part Skew - $t_{SK(t)}$

ORDERING INFORMATION

Example: