ICS300-11
QTClock™ 125 MHz Clock Synthesizer

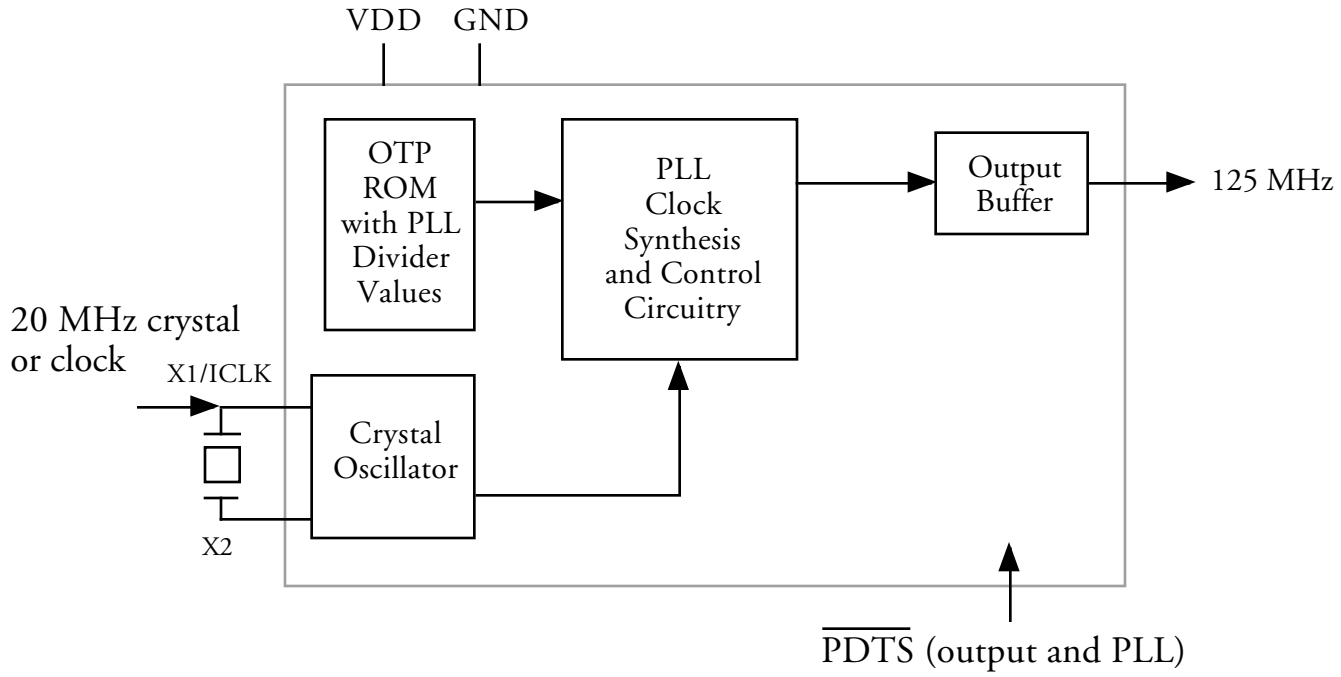
Description

The ICS300-11 QTClock™ generates a high quality, 125 MHz clock output from a 20 MHz crystal or clock input. It is designed to replace crystal oscillators in most electronic systems. The ICS300 contains a One Time Programmable (OTP) ROM which, in the -11 version, is factory programmed with the PLL divider values to output 125 MHz. Using Phase-Locked-Loop (PLL) techniques, the device runs from a standard fundamental mode, inexpensive crystal or clock. It is smaller and less expensive than a single 125 MHz oscillator.

Features

- Packaged in 8 pin SOIC
- Output clock frequency of 125 MHz at 3.3V
- Input crystal or clock frequency of 20 MHz
- Internal multiplier of 6.25
- Quick turn frequency programming allows production in two to four weeks
- Low jitter - 20 ps one sigma typical
- Duty cycle of 45/55
- Full CMOS level outputs with 25 mA drive capability at TTL levels
- Tri-state output + PLL power down pin
- Advanced, low power CMOS process

Block Diagram



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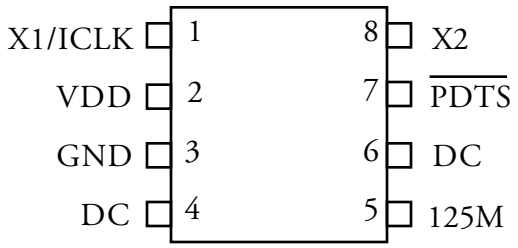
Pin Assignment



Pin Descriptions

Number	Name	Type	Description
1	X1/ICLK	I	Crystal connection. Connect to 20 MHz crystal or clock.
2	VDD	P	Connect to +3.3V or +5V.
3	GND	P	Connect to ground.
4	DC	-	Don't Connect anything to this pin.
5	125M	O	125 MHz clock output whose amplitude matches VDD.
6	DC	-	Don't Connect anything to this pin.
7	$\overline{\text{PDTS}}$	I	Powers down PLL, and puts output into high impedance state, when low.
8	X2	O	Crystal connection to 20 MHz crystal. Leave unconnected for clock input.

Key: I = Input, O = output, P = power supply connection

Device Configuration

The ICS300 QTClock has many programming options, so the two character alphanumeric programming code (in this case, the -11) must be specified when ordering parts.

External Components / Crystal Selection

The ICS300 requires a 0.01µF decoupling capacitor to be connected between VDD and GND. It must be connected close to the ICS300 to minimize lead inductance. No external power supply filtering is required for this device. A 33Ω terminating resistor can be used next to the CLK pin. The total on-chip capacitance is approximately 16 pF, so a parallel resonant, fundamental mode crystal should be used. For crystals with a specified load capacitance greater than 16 pF, crystal capacitors can be connected from each of the pins X1 and X2 to Ground. The value (in pF) of these crystal caps should be = $(C_L\text{-}16)*2$, where C_L is the crystal load capacitance in pF. These external capacitors are only required for applications where the exact frequency is critical. For a clock input, connect to X1 and leave X2 unconnected (no capacitors on either).

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Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
ABSOLUTE MAXIMUM RATINGS (stresses beyond these can permanently damage the device)					
Supply Voltage, VDD	Referenced to GND			7	V
Inputs	Referenced to GND	-0.5		VDD+0.5	V
Clock Output	Referenced to GND	-0.5		VDD+0.5	V
Ambient Operating Temperature		0		70	C
Soldering Temperature	Max of 10 seconds			260	C
Storage temperature		-65		150	C
DC CHARACTERISTICS (VDD = 3.3V, 25C unless otherwise noted)					
Operating Voltage, VDD		3.13		5.5	V
Input High Voltage, VIH, ICLK only	ICLK (Pin 1)	(VDD/2)+1	VDD/2		V
Input Low Voltage, VIL, ICLK only	ICLK (Pin 1)		VDD/2	(VDD/2)-1	V
Input High Voltage, VIH	$\overline{\text{PDTS}}$	2			V
Input Low Voltage, VIL	$\overline{\text{PDTS}}$			0.8	V
Output High Voltage, VOH	IOH=-4mA	VDD-0.4			V
Output High Voltage, VOH	IOH=-25mA	2.4			V
Output Low Voltage, VOL	IOL=25mA			0.4	V
IDD Operating Supply Current, 20 MHz crystal	No Load, 125MHz		18		mA
Short Circuit Current	CLK output		±70		mA
On-Chip Pull-up Resistor, $\overline{\text{PDTS}}$	Pin 7		270		kΩ
Input Capacitance, $\overline{\text{PDTS}}$	Pin 7		4		pF
AC CHARACTERISTICS (VDD = 3.3V, 25C unless otherwise noted)					
Input Frequency, crystal input			20	21.6	MHz
Output Frequency	VDD = 3.13 to 5.5V		125	135	MHz
Output Clock Rise Time, 0.8 to 2.0V	20pF load		0.7	1.2	ns
Output Clock Fall Time, 2.0 to 0.8V	20pF load		0.6	1.2	ns
Output Clock Duty Cycle	at VDD/2	45	49 to 51	55	%
Absolute Clock Period Jitter	Deviation from mean		±65	±130	ps
One Sigma Clock Period Jitter			20	40	ps
Power-up time, $\overline{\text{PDTS}}$ goes high until CLK out			8	20	ms

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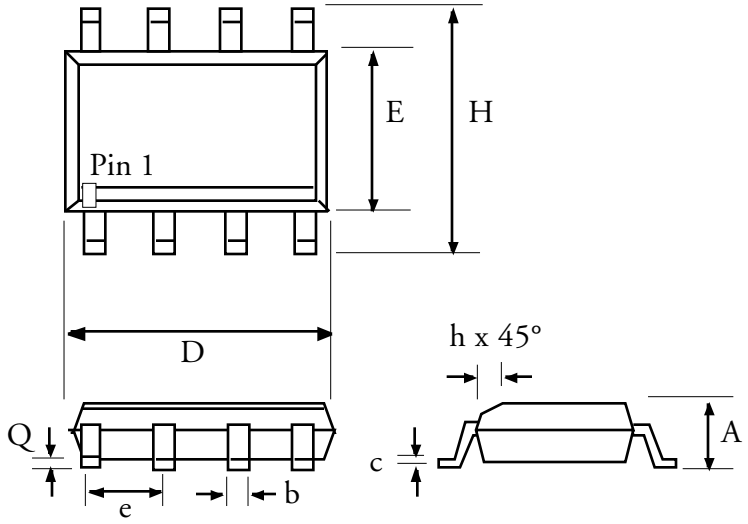
Package Outline and Package Dimensions



8 pin SOIC

	Inches		Millimeters	
Symbol	Min	Max	Min	Max
A	0.055	0.068	1.397	1.7272
b	0.013	0.019	0.330	0.483
D	0.185	0.200	4.699	5.080
E	0.150	0.160	3.810	4.064
H	0.225	0.245	5.715	6.223
e	.050 BSC		1.27 BSC	
h		0.015		0.381
Q	0.004	0.01	0.102	0.254

Ordering Information

Part/Order Number	Marking	Package	Temperature
ICS300M-11	ICS300M (top line)	8 pin SOIC	0 to 70 C
	YYWW -11 (2nd line)		
ICS300M-11T	ICS300M (top line)	8 pin SOIC on tape and reel	0 to 70 C
	YYWW -11 (2nd line)		

YYWW represents a 4 digit date code. The -11 is assigned by the factory, and indicates the output frequencies on CLK and REF, and other programming options.

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