High-Speed CMOS 3.3V 16-Bit Buffers/Line Drivers with Bus Hold

QS74LVCH16244A

ADVANCE INFORMATION

FEATURES/BENEFITS

- 5V tolerant inputs and outputs
- Bus Hold feature holds last active state during 3-state operation
- 10µA I_{CCQ} quiescent power supply current
- Hot insertable
- 2.0V–3.6V V_{CC} supply operation
- ±24mA balanced output drive
- Power down high impedance inputs and outputs
- t_{PD} = 4.1ns max.
- Input hysteresis for noise immunity
- Meets or exceeds JEDEC Standard 36 specifications
- Multiple power and ground pins for low noise
- Operating temperature range:
    –40°C to 85°C
- Latch-up performance exceeds 500mA
- ESD performance:
    Human body model > 2000V
    Machine model > 200V
- Packages available:
    48-pin TSSOP
    48-pin SSOP

DESCRIPTION

The QS74LVCH16244A is a 16-bit bus interface buffer with three-state output that is ideal for driving address, clocks, and data buses. Output enables are used to enable or disable Y ports by placing them in a high impedance condition. The QS74LVCH16244A provides Bus Hold circuitry on the data inputs to retain the last active state during 3-state operation, eliminating the need for external pull-up resistors. The 3.3V LVC family features low power, low switching noise, and fast switching speeds for low power portable applications as well as high-end, advanced workstation applications. 5V tolerant inputs and outputs allow these LVC products to be used in mixed 5V and 3.3V applications. Easy board layout is facilitated by the use of flow-through pinouts and byte enable controls provide architectural flexibility for systems designers. To accommodate hot-plug or live insertion applications, this product is designed not to load an active bus when V_{CC} is removed. However, during power up or power down sequence, $\overline{OE}$ should be tied to V_{CC} to ensure high-impedance state on the outputs.
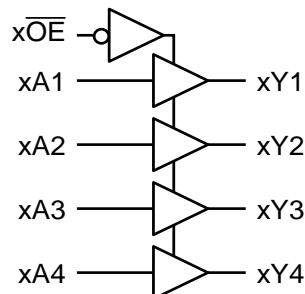
Figure 1. Functional Block Diagram
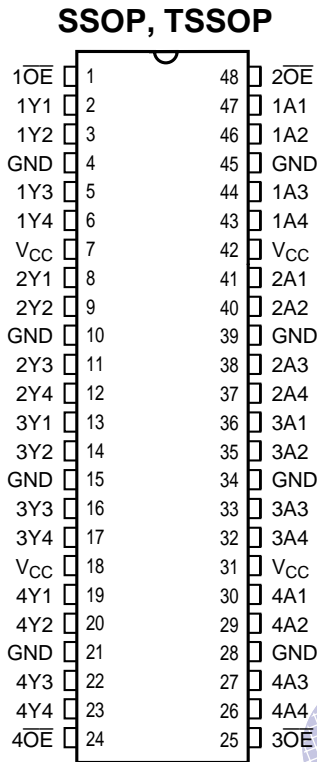
Figure 2. Pin Configuration
(All Pins Top View)

SSOP, TSSOP

1$\overline{\text{OE}}$	1	48	2$\overline{\text{OE}}$
1Y1	2	47	1A1
1Y2	3	46	1A2
GND	4	45	GND
1Y3	5	44	1A3
1Y4	6	43	1A4
V_{CC}	7	42	V_{CC}
2Y1	8	41	2A1
2Y2	9	40	2A2
GND	10	39	GND
2Y3	11	38	2A3
2Y4	12	37	2A4
3Y1	13	36	3A1
3Y2	14	35	3A2
GND	15	34	GND
3Y3	16	33	3A3
3Y4	17	32	3A4
V_{CC}	18	31	V_{CC}
4Y1	19	30	4A1
4Y2	20	29	4A2
GND	21	28	GND
4Y3	22	27	4A3
4Y4	23	26	4A4
4$\overline{\text{OE}}$	24	25	3$\overline{\text{OE}}$

Table 1. Pin Description

Name	Description
x$\overline{\text{OE}}$	Three-State Output Enable Inputs
xAx	Data Inputs (Bus Hold)
xYx	Three-State Outputs

Table 2. Function Table

Inputs		Outputs
x$\overline{\text{OE}}$	xAx	xYx
L	L	L
L	H	H
H	X	Hi-Z

Table 3. Absolute Maximum Ratings

Supply Voltage to Ground .... –0.5V to 7.0V
DC Output Voltage V_{OUT}
 Outputs HIGH-Z .... –0.5V to 7.0V
 Outputs Active .... –0.5V to V_{CC} + 0.5V
DC Input Voltage V_{IN} .... –0.5V to 7.0V
DC Input Diode Current with V_{IN} < 0 .... –50mA
DC Output Diode Current
 V_O < 0 .... –50mA
 V_O > V_{CC} 50mA
DC Output Source/Sink Current (I_{OH}/I_{OL}) .... ±50mA
DC Supply Current per Supply Pin .... ±100mA
DC Ground Current per Ground Pin .... ±100mA
T_{STG} Storage Temperature .... –65°C to 150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

Table 4. Recommended Operating Conditions

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage, Operating		2.0	3.6	V
	Supply Voltage, Data Retention Only		1.5	3.6	
V_{IH}	Input HIGH Voltage	V_{OL} = 2.7 to 3.6V	2.0	—	V
V_{IL}	Input LOW Voltage	V_{CC} = 2.7 to 3.6V	—	0.8	V
V_{IN}	Input Voltage		0	5.5	V
V_{OUT}	Output Voltage in Active State		0	V_{CC}	V
	Output Voltage in "OFF" State		0	5.5	
I_{OH}	Output Current HIGH	V_{CC} = 3.0–3.6V	—	−24	mA
		V_{CC} = 2.7V		−12	
I_{OL}	Output Current LOW	V_{CC} = 3.0–3.6V	—	24	mA
		V_{CC} = 2.7V	—	12	
$\Delta t/\Delta v$	Input Transition Slew Rate		—	10	ns/V
T_A	Operating Free Air Temperature		−40	85	°C

Table 5. DC Electrical Characteristics Over Operating Range

Industrial Temperature Range, T_A = –40°C to 85°C

Symbol	Parameter	Test Conditions		Min	Typ[1]	Max	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 2.7V, I_{OH} = –100µA		V_{CC} –0.2	—	—	V
		V_{CC} = 2.7V, I_{OH} = –12mA		2.2	—	—	
		V_{CC} = 3.0V, I_{OH} = –12mA		2.4	—	—	
		V_{CC} = 3.0V, I_{OH} = –24mA		2.2	—	—	
V_{OL}	Output LOW Voltage	V_{CC} = 2.7V, I_{OL} = 100µA		—	—	0.2	V
		V_{CC} = 2.7V, I_{OL} =12mA		—	—	0.4	
		V_{CC} = 3.0V, I_{OL} = 24mA		—	—	0.55	
V_{IK}	Input Clamp Voltage	V_{CC} = 2.7V, I_{IN} = –18mA		—	–0.7	–1.2	V
I_I	Input Leakage Current	V_I = 0V, V_I = 5.5V, V_{CC} = 3.6V		—	—	±1.0	µA
$|I_{BH}|$	Bus Hold Inputs Overdrive Current[2,3]	V_{CC} = 3.6V, V_{IN} =0V or V_{IN} = V_{CC}		—	—	50	µA
		V_{CC} = 3.6V, 0.8V < V_{IN} < 2.0V		—	—	500[4]	
I_{BHH}	Bus Hold Input Sustaining Current	V_{CC} = 3V	V_{IN} = 2.0V	–75	—	—	µA
I_{BHL}			V_{IN} = 0.8V	75	—	—	
I_{OZ}	High-Z I/O Leakage	V_O = 0V, V_O = 5.5V, V_I = V_{IH} or $V_{IL,}$ V_{CC} = 3.6V		—	—	±1.0	µA
I_{OFF}	Power Off Leakage	V_{CC} = 0V, V_I or V_O = 5.5V		—	—	10	µA
I_{CC}	Quiescent Power Supply Current	V_{CC} = 3.6V, V_{IN} = V_{CC} or GND		—	0.1	10	µA
ΔI_{CC}	Quiescent Power Supply Current per Control Inputs at TTL HIGH	V_{CC} = 3.6V, V_{IN} = V_{CC} – 0.6V[5]		—	2.0	3.0	µA
	Quiescent Power Supply Current per Bus Hold Inputs at TTL HIGH	V_{CC} = 3.6V, V_{IN} = V_{CC} – 0.6V[5]		—	75	500	µA

Notes:
1. Typical values are at V_{CC} = 3.3V and T_A = 25°C.
2. These parameters are guaranteed by characterization, but not production tested.
3. Pins with Bus Hold are identified in the pin description.
4. An external driver must provide at least $|I_{BH}|$ during transition to guarantee that the Bus Hold input will change state.
5. Per TTL driven input. All other inputs at V_{CC} or GND.

Table 6. Dynamic Switching Characteristics

Symbol	Parameter	Test Conditions		Typ[1]	Unit
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50pF$, $V_{CC} = 3.3V$	$V_{IH} = 3.3V$, $V_{IL} = 0V$	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50pF$, $V_{CC} = 3.3V$	$V_{IH} = 3.3V$, $V_{IL} = 0V$	0.8	V
C_{PD}	Power Dissipation	$C_L = 50pF$, $f = 10MHz$, $V_{CC} = 3.3 \pm 0.3V$	Output Enable	20	pF
			Output Disable	4	

Note:

1. Typical values are at $V_{CC} = 3.3V$, 25°C ambient.

Table 7. Capacitance[1]

Symbol	Pins	Conditions	Typ	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$, $V_{OUT} = 0V$, $f = 1MHz$	7.0	pF
$C_{I/O}$	I/O Capacitance	$V_{IN} = 0V$, $V_{OUT} = 0V$, $f = 1MHz$	8.0	pF

Note:

1. Capacitance is characterized but not production tested.

Table 8. Switching Characteristics Over Operating Range

Industrial Temperature Range, $T_A = -40°C$ to 85°C.

$C_{LOAD} = 50pF$, $R_{LOAD} = 500\Omega$ unless otherwise noted.

Symbol	Description[1]	$V_{CC} = 3.3 \pm 0.3V$		$V_{CC} = 2.7V$[2]		Unit
		Min	Max	Min	Max	
t_{PD}	Propagation Delay xAx to xYx	1.5	4.1	1.5	4.7	ns
t_{EN}	Output Enable Time x$\overline{OE}$ to xYx	1.5	4.6	1.5	5.8	ns
t_{DIS}	Output Disable Time[2] x$\overline{OE}$ to xYx	1.5	5.8	1.5	6.2	ns
$t_{SK(O)}$	Output Skew[3]	—	0.5	—	—	ns

Notes:

1. Minimums guaranteed but not tested. See Test Circuit and Waveforms.
2. Guaranteed by characterization.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by characterization but not production tested.

TEST CIRCUIT AND WAVEFORMS
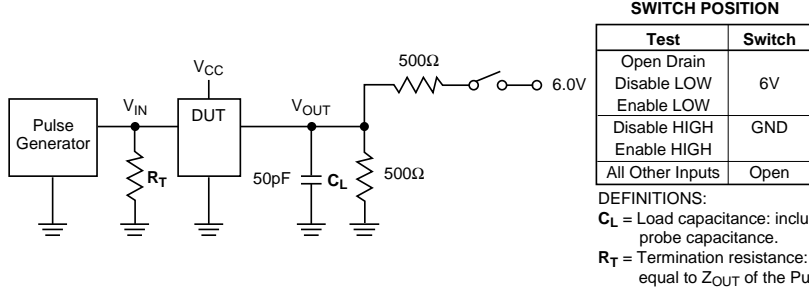
Figure 3. Test Circuit

SWITCH POSITION	
Test	**Switch**
Open Drain Disable LOW Enable LOW	6V
Disable HIGH Enable HIGH	GND
All Other Inputs	Open

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

Figure 4. Setup, Hold, and Release Timing
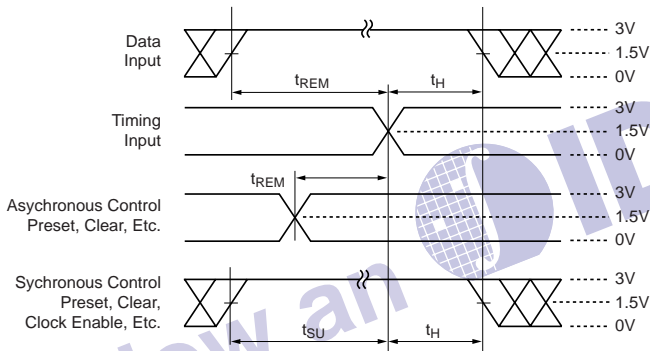
Figure 6. Pulse Width
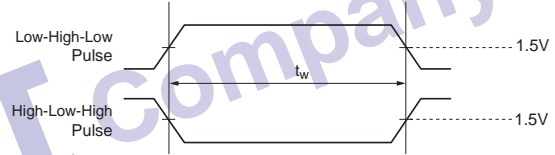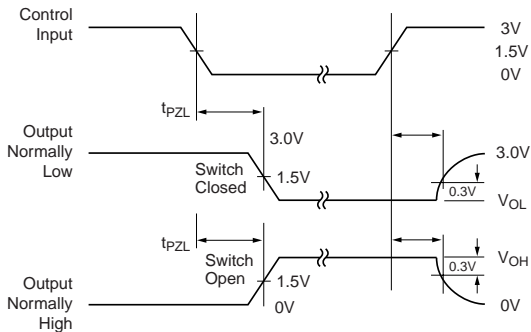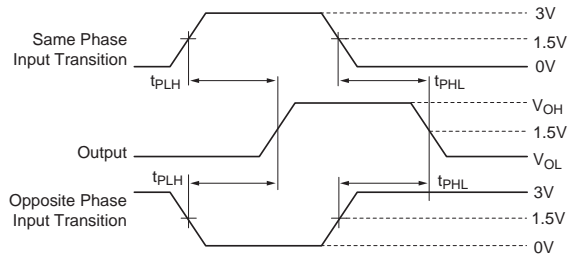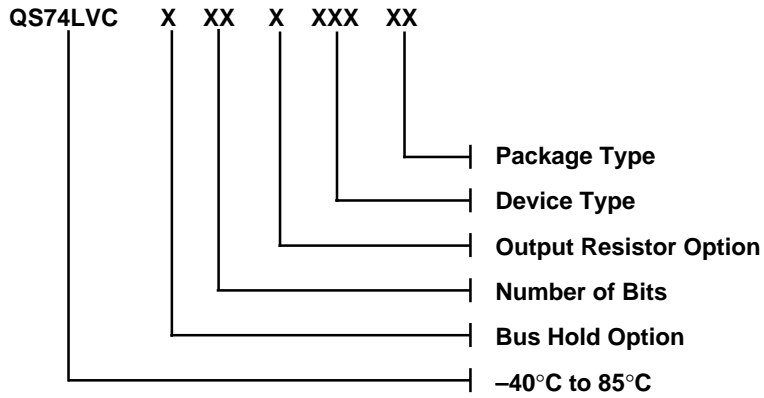

Figure 5. Enable and Disable Timing

Figure 7. Propagation Delay

Notes:

1. Input Control Enable = LOW and Input Control Disable = HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_{OUT} \le 50\Omega$; t_F, $t_R \le 2.5$ns.

QUALITY SEMICONDUCTOR, INC.

ORDERING INFORMATION

QS74LVC   X XX X XXX XX

                     Package Type

                     Device Type

                     Output Resistor Option

                     Number of Bits

                     Bus Hold Option

                     −40°C to 85°C

Bus Hold Option:
H – with Bus Hold

Number of Bits:
16 – 16-Bit

Output Resistor Option:
Blank – No Output Resistor

Device Type:
244

Package Type:
PV – SSOP, 300 mil
PA – TSSOP, 240 mil