

March 1997

CMOS Dual Counter-Timer

Features

- Compatible with General Purpose and CDP1800 Series Microprocessor Systems
- Two 16-Bit Down Counters and Two 8-Bit Control Registers
- 5 Modes Including a Versatile Variable-Duty Cycle Mode
- Programmable Gate-Level Select
- Two-Complemented Output Pins for Each Counter-Timer
- Software-Controlled Interrupt Output
- Addressable in Memory Space or CDP1800-Series I/O Space

Description

The CDP1878C is a dual counter-timer consisting of two 16-bit programmable down counters that are independently controlled by separate control registers. The value in the registers determine the mode of operation and control functions. Counters and registers are directly addressable in memory space by any general industry type microprocessors, in addition to input/output mapping with the CDP1800 series microprocessors.

Each counter-timer can be configured in five modes with the additional flexibility of gate-level control. The control registers in addition to mode formatting, allow software start and stop, interrupt enable, and an optional read control that allows a stable readout from the counters. Each counter-timer has software control of a common interrupt output with an interrupt status register indicating which counter-timer has timed out.

In addition to the interrupt output, true and complemented outputs are provided for each counter-timer for control of peripheral devices.

This type is supplied in 28-lead dual-in-line ceramic packages (D suffix), and 28-lead dual-in-line plastic packages (E suffix).

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE	PKG. NO.
CDP1878CE	-40°C to +85°C	PDIP	E28.6
CDP1878CD	-40°C to +85°C	SBDIP	N28.6

Pinout

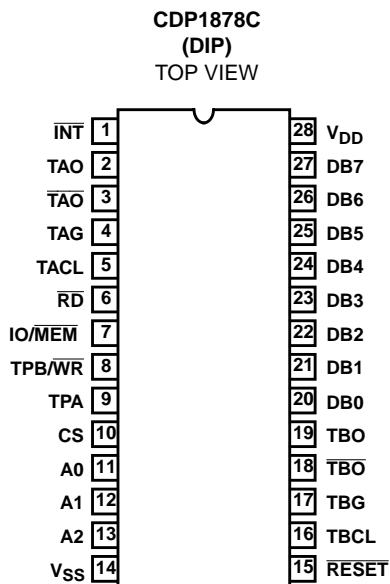


TABLE 1. MODE DESCRIPTION

MODE	FUNCTION	APPLICATION
1 Timeout	Outputs change when clock decrements counter to "0"	Event counter
2 Timeout Strobe	One clockwise output pulse when clock decrements counter to "0"	Trigger pulse
3 Gate-Controlled One Shot	Outputs change when clock decrements counter to "0". Retriggerable	Time-delay generation
4 Rate Generator	Repetitive clockwise output pulse	Time-base generator
5 Variable-Duty Cycle	Repetitive output with programmed duty cycle	Motor control

CDP1878C

Absolute Maximum Ratings

DC Supply-Voltage Range, (V_{DD})
(All Voltages Referenced to V_{SS} Terminal)
CDP1878C -0.5V to +7V
Input Voltage Range, All Inputs -0.5V to $V_{DD} + 0.5V$
DC Input Current, Any One Input. $\pm 10mA$

Thermal Information

Thermal Resistance (Typical) θ_{JA} ($^{\circ}C/W$) θ_{JC} ($^{\circ}C/W$)
PDIP Package 55 N/A
SBDIP Package 50 12
Device Dissipation Per Output Transistor
 T_A = Full Package Temperature Range
(All Package Types) 100mW
Operating Temperature Range (T_A)
Package Type D $-55^{\circ}C$ to $+125^{\circ}C$
Package Type E $-40^{\circ}C$ to $+85^{\circ}C$
Storage Temperature Range (T_{STG}) $-65^{\circ}C$ to $+150^{\circ}C$
Lead Temperature (During Soldering)
At distance $1/16 \pm 1/32$ In. ($1.59 \pm 0.79mm$)
from case for 10s max. $+265^{\circ}C$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions At T_A = Full Package Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

PARAMETER	SYMBOL	MIN	MAX	UNITS
DC Operating Voltage Range		4	6.5	V
Input Voltage Range		V_{SS}	V_{DD}	V
Maximum Clock Input Rise or Fall Time	t_R, t_F	-	5	μs
Minimum Clock Pulse Width	t_{WL}, t_{WH}	200	-	ns
Maximum Clock Input Frequency	f_{CL}	DC	1	MHz

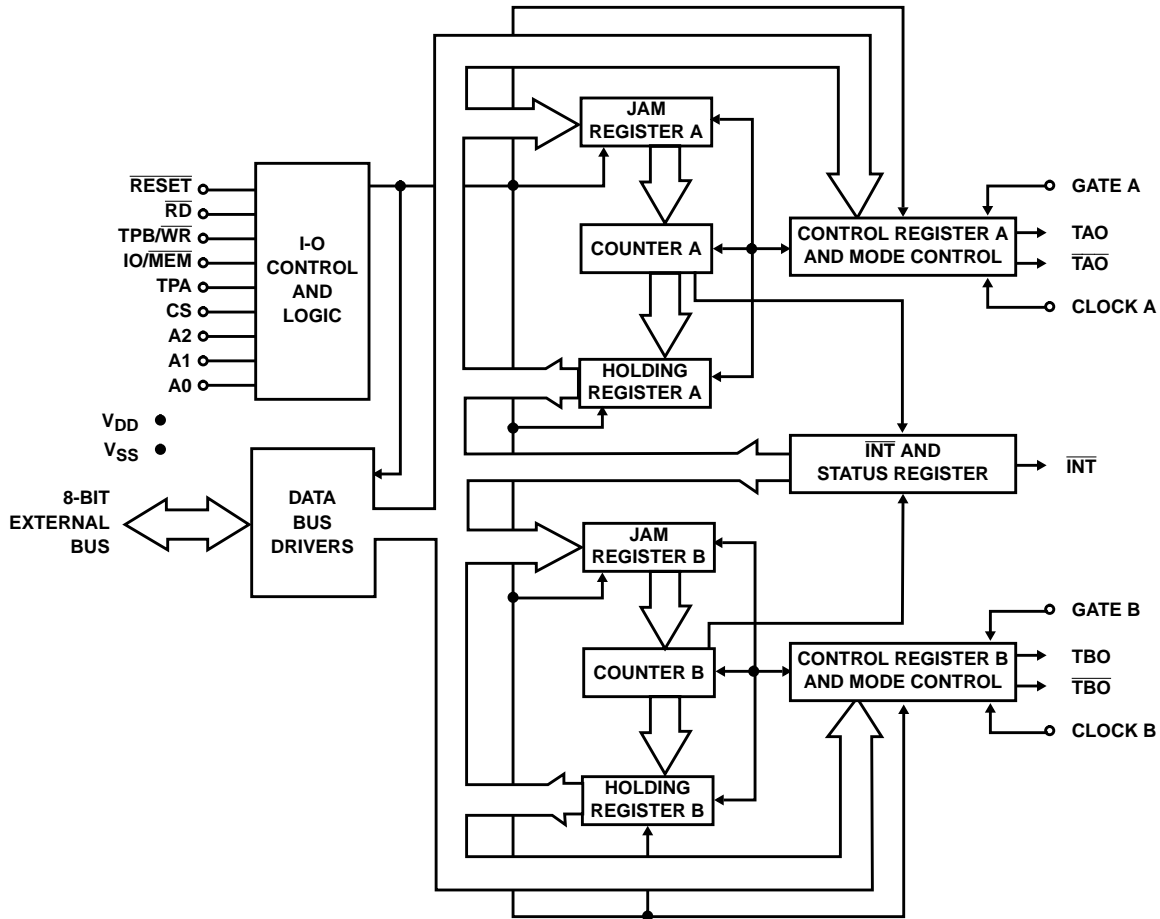
Static Electrical Specifications At T_A = $-40^{\circ}C$ to $+85^{\circ}C$, $V_{DD} \pm 5\%$ Except as noted:

PARAMETER	SYMBOL	CONDITIONS			LIMITS			UNITS
		V_O (V)	V_{IN} (V)	V_{DD} (V)	MIN	(NOTE 1) TYP	MAX	
Quiescent Device Current	I_{DD}	-	0, 5	5	-	0.02	200	μA
Output Low Drive (Sink) Current	I_{OL}	0.4	0, 5	5	1.6	3.2	-	mA
Output High Drive (Source) Current	I_{OH}	4.6	0, 5	5	-1.15	-2.3	-	mA
Output Voltage Low-Level (Note 2)	V_{OL}	-	0, 5	5	-	0	0.1	V
Output Voltage High-Level (Note 2)	V_{OH}	-	0, 5	5	4.9	5	-	V
Input Low Voltage	V_{IL}	0.5, 4.5	-	5	-	-	1.5	V
Input High Voltage	V_{IH}	0.5, 9.5	-	5	3.5	-	-	V
Input Leakage Current	I_{IN}	Any Input	0, 5	5	-	-	± 1	μA
Operating Current (Note 3)	I_{DD1}	-	0, 5	5	-	1.5	3	mA
Input Capacitance	C_{IN}	-	-	-	-	5	7.5	pF
Output Capacitance	C_{OUT}	-	-	-	-	10	15	pF

NOTES:

- Typical values are for $T_A = +25^{\circ}C$ and nominal V_{DD} .
- $I_{OL} = I_{OH} = 1\mu A$
- Operating current measured at 200kHz for $V_{DD} = 5V$, with open outputs (worst-case frequencies for CDP1802A system operating at maximum speed of 3.2MHz).

Functional Diagram



FUNCTIONAL DEFINITIONS FOR CDP1878C TERMINALS

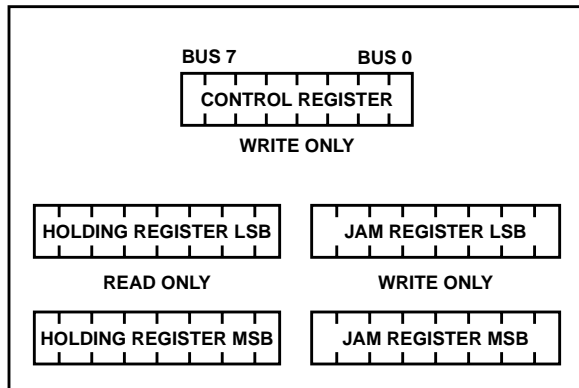
TERMINAL	USAGE
V _{DD} - V _{SS}	Power
DB0-DB7	Data to and from device
TPB/WR, RD	Directional Control Signals
A0, A1, A2	Addresses that select counters or registers
TACL, TBCL	Clocks used to decrement counters
TAG, TBG	Gate inputs that control counters

TERMINAL	USAGE
TAO, TAŌ	Complemented outputs of Timer A
TBO, TBŌ	Complemented outputs of Timer B
TPA	Used with CDP1800-series processors, tied high otherwise
CS	Active high input that enables device
INT̄	Low when counter is "0"
RESET	When active, TAO, TBO are low, TAŌ, TBŌ are high. Interrupt status register is cleared.
IO/MEM̄	Tied high in CDP1800 input/output mode, otherwise tied low

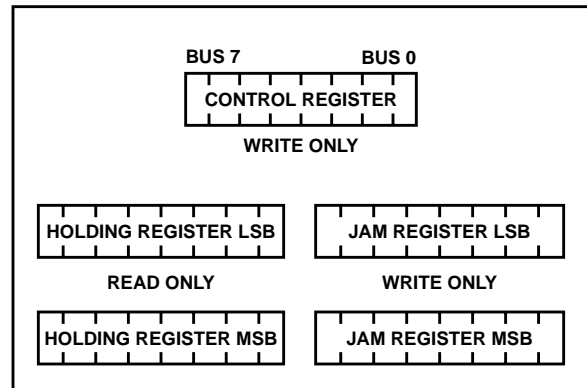
REGISTER TRUTH TABLE

ADDRESS			ACTIVE		REGISTER COUNTER
A2	A1	A0	TPB/W \overline{R}	R \overline{D}	
1	1	0	X		Write Counter A MSB
1	1	0		X	Read Counter A MSB
0	1	0	X		Write Counter A LSB
0	1	0		X	Read Counter A LSB
1	0	0	X		Control Register A
1	1	1	X		Write Counter B MSB
1	1	1		X	Read Counter B MSB
0	1	1	X		Write Counter B LSB
0	1	1		X	Read Counter B LSB
1	0	1	X		Control Register B
1	0	0		X	Interrupt Status Register
1	0	1		X	
0	0	0			Not Used
0	0	1			Not Used

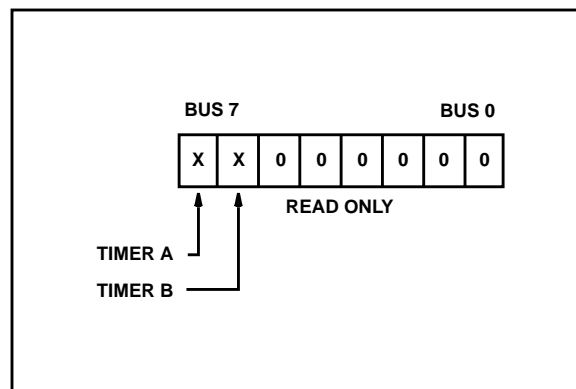
Programming Model



COUNTER A REGISTERS



COUNTER B REGISTERS



INTERRUPT STATUS REGISTER

Functional Description

The dual counter-timer consists of two programmable 16-bit down counters, separately addressable and controlled by two independent 8-bit control registers. The word in the control register determines the mode and type of operation that the counter-timer performs. Writing to or reading from a counter or register is enabled by selective addressing during a write or read cycle. The data is placed on the data bus by the microprocessor during the write cycle or read from the counter during the read cycle. Data to and from the counters and to the control registers is in binary format.

Each counter-timer consists of three parts. The first is the counter itself, a 16-bit down counter that is decremented on the trailing edge of the clock input. The second is the jam register that receives the data when the counter is written to. The word in the control register determines when the jam register value is placed into the counter. The third part is the holding register that places the counter value on the data bus when the counter is read.

When the counter has decremented to zero, three events occur. The first involves the common interrupt output pin that, if enabled, becomes active low. The second is the setting of a bit in the interrupt status register. This register can be read to determine which counter-timer has timed out. The third event is the logic change of the complemented output pins.

In addition to the clock input used to decrement the counter, a gate input is available to enable or initiate operation. The counter-timers are independent and can have different mode operations.

Write Operation

The counters and registers are separately addressable and are programmed via the data bus when the chip is selected with the TPB/ \overline{WR} pin active. Normal sequencing requires that the counter jam register be loaded first with the required value

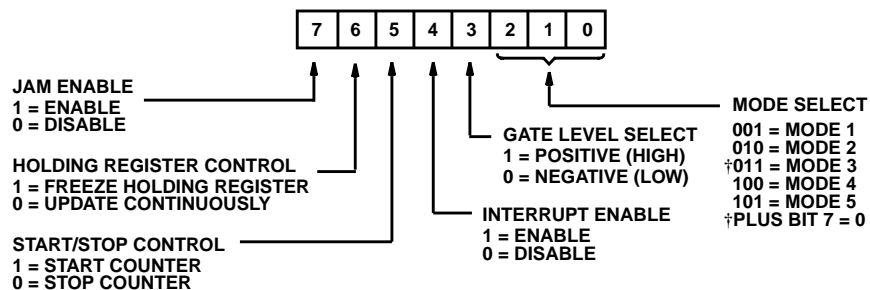
(most significant and least significant byte in any order), and then the control register be accessed and loaded with the control word. The trailing edge of the TPB/ \overline{WR} pulse will latch the control word into the control register. The trailing edge of the first clock to occur with gate valid will cause the counter to be jammed with its initial value. The counter will decrement on the trailing edge of succeeding clocks as long as the gate is valid, until it reaches zero. The output levels will then change, and if enabled, the interrupt output will become active and the appropriate timer bit will be set in the interrupt status register. The interrupt output and the interrupt status register can be cleared (to their inactive state) by addressing the control register with the TPB/ \overline{WR} line active. For example, if counter A times out, control register A must be accessed to reset the interrupt output high and reset the timer A bit in the status register low. Timer B bit in the status register will be unaffected.

Read Operation

Each counter has a holding register that is continuously being updated by the counter and is accessed when the counter is addressed during read cycles. Counter reads are accomplished by halting the holding register and then reading it, or by reading the holding register directly. If the holding register is read directly, data will appear on the bus if the counters are addressed with the \overline{RD} line active. However, if the clock decrements the counter between the two read operations (most and least significant byte), an inaccurate value will be read. To preclude this from happening, writing a "1" into bit 6 of the control register and then addressing and reading the counter will result in a stable reading. This operation prevents the holding register from being updated by the counter and does not affect the counter's operation.

The interrupt status register is read by addressing either control register with the RD line active. A "1" in bit 7 indicates Timer A has timed out and a "1" in bit 6 indicates Timer B has timed out. Bits 0-5 are zeros.

Control Register



Bits 0, 1 and 2

Mode Selects - See Mode Timing Diagrams (Figures 1, 2, 3, 4, and 5).

Note: When selecting a mode, the timer outputs TAO and TBO are set low, and \overline{TAO} and \overline{TBO} are set high. If bits 0, 1 and 2 are all zero's when the control register is loaded, no mode is selected, and the counter-timer outputs are unaffected. Issuing mode 6 will cause an indeterminate condition of the counter, issuing mode 7 is equivalent to issuing mode 5.

	BIT 7	BIT 2	BIT 1	BIT 0
Mode 1 - Timeout	-	0	0	1
Mode 2 - Timeout Strobe	-	0	1	0
Mode 3 - Gate Controlled One Shot	0	0	1	1
Mode 4 - Rate Generator	-	1	0	0
Mode 5 - Variable-Duty Cycle	-	1	0	1
No Mode selected. Counter outputs unaffected	-	0	0	0

Bit 3 - Gate Level Select - All modes require an enabling signal on the gate to allow counter operation. This enabling signal is either a level or a pulse (edge). Positive gate level or edge enabling is selected by writing a "1" into this bit and negative (low) enabling is selected when bit 3 is "0".

Bit 4 - Interrupt Enable - Setting this bit to "1" enables the $\overline{\text{INT}}$ output, and setting it to "0" disables it. When reset, the $\overline{\text{INT}}$ output is at a high level. If the interrupt enable bit in the control register is enabled and the counter decrements to zero, the $\overline{\text{INT}}$ output will go low and will not return high until the counter-timer is reset or the selected control register is written to. Example: If timer B times out, control register B must be accessed to reset the $\overline{\text{INT}}$ output high. If the interrupt enable bit is set to "0", the counter's timeout will have no effect on the $\overline{\text{INT}}$ output.

In mode 5, the variable-duty cycle mode, the $\overline{\text{INT}}$ pin will become active low when the MSB in the counter has decremented to zero.

Bit 5 - Start/Stop Control - This bit controls the clock input to the counter and must be set to "1" to enable it. Writing a "0" into this location will halt operation of the counter. Operation will not resume until the bit is set to "1".

Bit 6 - Holding Register Control - Since the counter may be decrementing during a read cycle, writing a "1" into this loca-

tion will hold a stable value in the hold register for subsequent read operations. Rewriting a "1" into bit 6 will cause an update in the holding register on the next trailing clock edge. If this location contains a "0", the holding register will be updated continuously by the value in the counter.

Bit 7 - Jam Enable - When this bit is set to "1" "during a write to the control register, the 16-bit value in the jam register will be available to the counter; TAO and TBO are reset low and $\overline{\text{TAO}}$ and $\overline{\text{TBO}}$ are set high. On the trailing edge of the first input clock signal with the gate valid this value will be latched in the counter, the counter outputs TAO and TBO will be set high and the $\overline{\text{TAO}}$ and $\overline{\text{TBO}}$ will be reset low. Setting bit 7 to "0" will leave the counter value unaffected. This location should be set to "0" any time a write to the control register must be performed without changing the present counter value. If the value in the jam register has not been changed, writing a "1" into bit 7 of the control register with zeros in bits 0,1, and 2 (mode select) will reload the counter with the old value and leave the mode unchanged. If the value in the jam register is changed, then the next write to the control register (with bit 7 a "1") must include a valid mode select (i.e., at least 1 of the bits 0,1, or 2 must be a "1").

In mode 3, the hardware start is enabled by writing a "0" into bit 7. If a "1" is written to bit 7, the timeout will start immediately and mode 3 will resemble mode 1.

Mode Descriptions

MODE		CONTROL REGISTER	GATE CONTROL																
1	Timeout	<table><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>1</td></tr><tr><td colspan="5">BUS 7</td><td colspan="3">BUS 0</td></tr></table>	X	X	X	X	X	0	0	1	BUS 7					BUS 0			Selectable High or Low Level Enables Operation
X	X	X	X	X	0	0	1												
BUS 7					BUS 0														

Mode 1

After the count is loaded into the jam register and the control register is written to with the jam-enable bit high on the trailing edge of the first clock after the gate is valid, TXO goes high and $\overline{\text{TXO}}$ goes low. The input clock decrements the counter as long as the gate remains valid. When it reaches zero TXO goes low and $\overline{\text{TXO}}$ goes high, and if enabled, the

interrupt output is set low. Writing to the counter while it is decrementing has no effect on the counter value unless the control register is subsequently written to with the jam-enable bit high. After timeout the counter remains at FFFF unless reloaded.

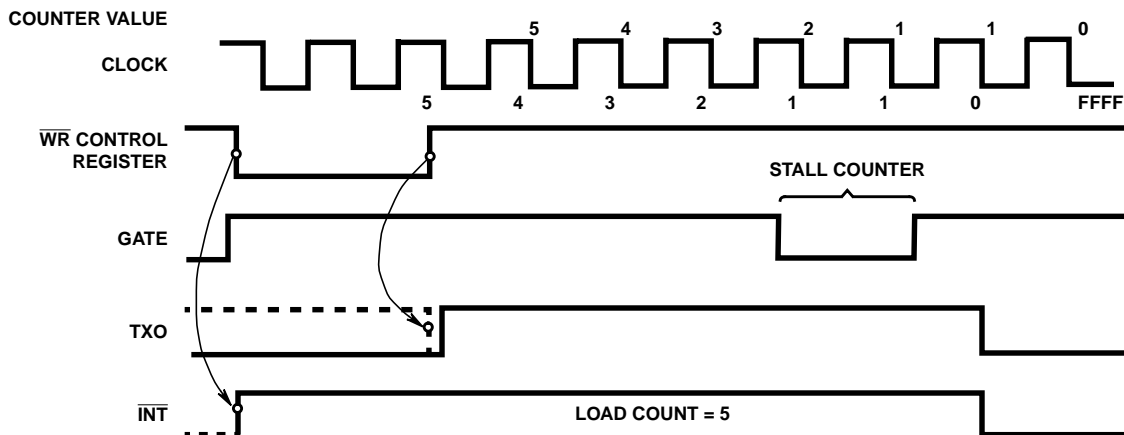


FIGURE 1. TIMEOUT (MODE 1) TIMING WAVEFORMS

MODE		CONTROL REGISTER	GATE CONTROL																
2	Timeout Strobe	<table><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>1</td><td>0</td></tr><tr><td colspan="5">BUS 7</td><td colspan="3">BUS 0</td></tr></table>	X	X	X	X	X	0	1	0	BUS 7					BUS 0			Selectable High or Low Level Enables Operation
X	X	X	X	X	0	1	0												
BUS 7					BUS 0														

Mode 2

Operation of this mode is the same as mode 1, except the outputs will change for one clock period only and then return to the condition of TXO high and $\overline{\text{TXO}}$ low, and the counter is reloaded

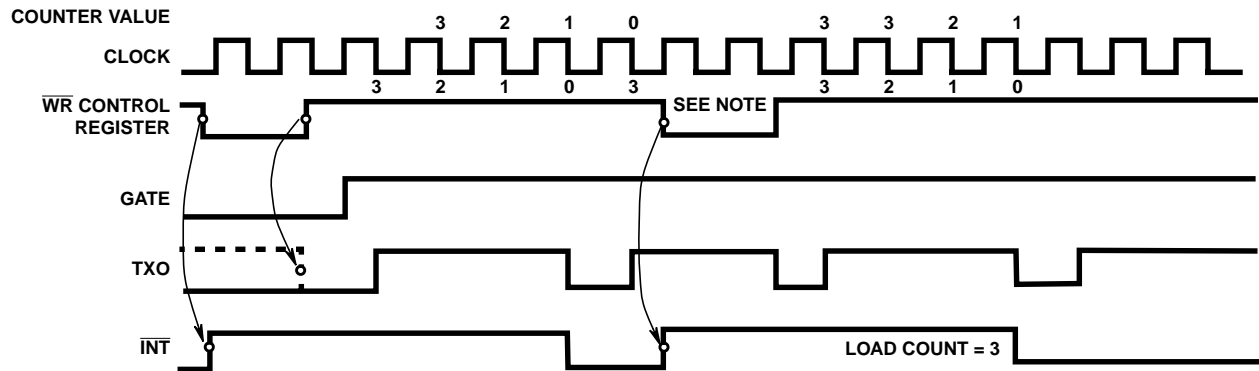


FIGURE 2. TIMEOUT STROBE (MODE 2) TIMING WAVEFORMS

NOTE: Write to control register with mode selects = 0

MODE		CONTROL REGISTER	GATE CONTROL																
3	Gate Controlled One-Shot	<table><tr><td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>1</td><td>1</td></tr><tr><td colspan="5">BUS 7</td><td colspan="3">BUS 0</td></tr></table>	0	X	X	X	X	0	1	1	BUS 7					BUS 0			<div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></d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0	X	X	X	X	0	1	1												
BUS 7					BUS 0														

Mode 3

After the jam register is loaded with the required value, the gate edge will initiate this mode. TXO will be set high, and $\overline{\text{TXO}}$ will be set low. The clock will decrement the counter. When zero is reached, TXO will go low and $\overline{\text{TXO}}$ will be high, and the interrupt output will be set low. The counter is retriggerable: While the counter is decrementing, a gate edge or write to the control register with the jam-enable bit high, will load the counter with the jam register value and restart the one-shot operation.

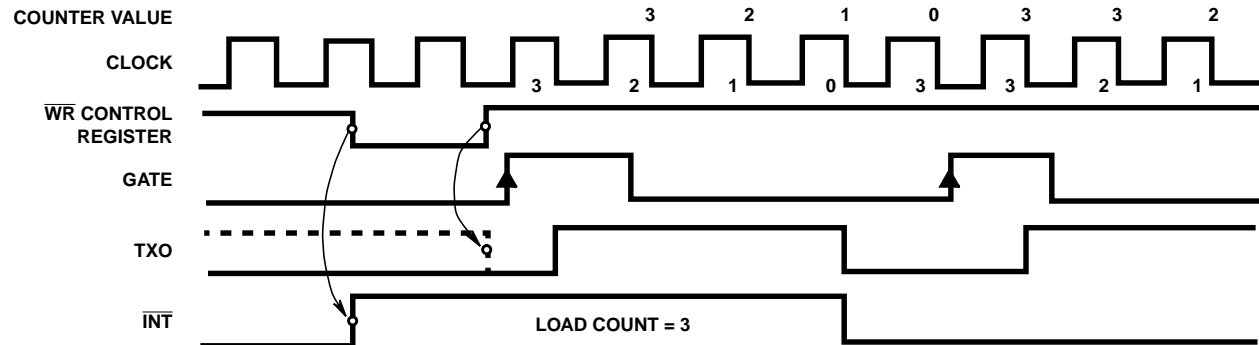


FIGURE 3. GATE CONTROLLED ONE-SHOT (MODE 3) TIMING WAVEFORMS

MODE		CONTROL REGISTER	GATE CONTROL																
4	Rate Generator	<table><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>1</td><td>0</td><td>0</td></tr><tr><td colspan="5">BUS 7</td><td colspan="3">BUS 0</td></tr></table>	X	X	X	X	X	1	0	0	BUS 7					BUS 0			Selectable High or Low Level Enables Operation
X	X	X	X	X	1	0	0												
BUS 7					BUS 0														

Mode 4

A repetitive clock-wide output pulse will be output, with the time between pulses equal to the counter's value, (trailing edge to leading edge). This model is software started with a write to the control register if the gate level is valid. If the counter is written to while decrementing, the new value will

not affect the counter's operation until the present timeout has concluded, unless the control register is written to with the jam-enable bit high. If the gate input (TAG or TBG) is used to start this mode, the first cycle following the gate going true is indeterminate.

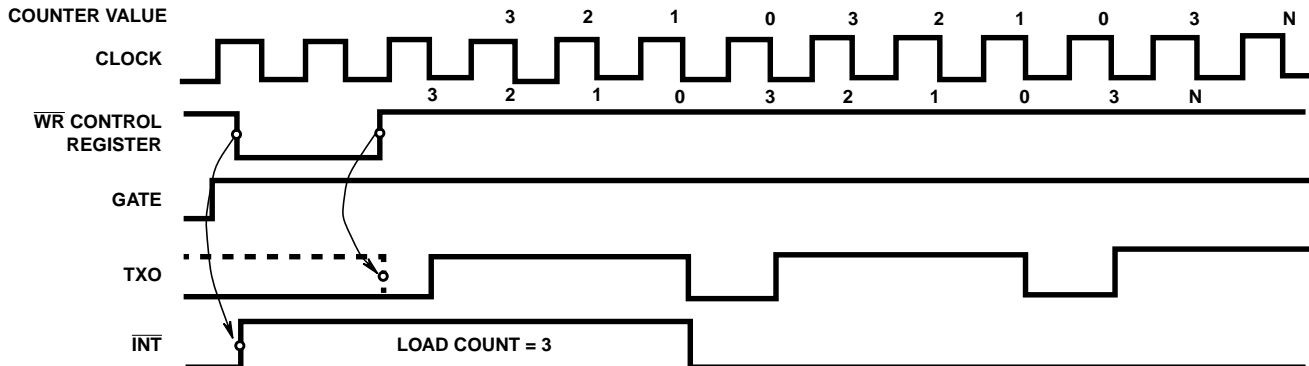


FIGURE 4. RATE GENERATORS (MODE 4) TIMING WAVEFORMS

MODE		CONTROL REGISTER	GATE CONTROL																
5	Variable Duty Cycle	<table><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>1</td><td>0</td><td>1</td></tr><tr><td colspan="5">BUS 7</td><td colspan="3">BUS 0</td></tr></table>	X	X	X	X	X	1	0	1	BUS 7					BUS 0			Selectable High or Low Level Enables Operation
X	X	X	X	X	1	0	1												
BUS 7					BUS 0														

Mode 5

After the mode is initiated, the outputs will remain at one level until the clock decrements the least significant byte of the counter to N+1. The outputs will then change level and the counter decrements the most significant byte to N+1. The process will then repeat, resulting in a repetitive output

with a duty cycle directly controlled by the value in the counter. The output period will be equal to $LSB+MSB+2$.

The interrupt output will become active after the MSB is loaded into the counter and decrements to zero.

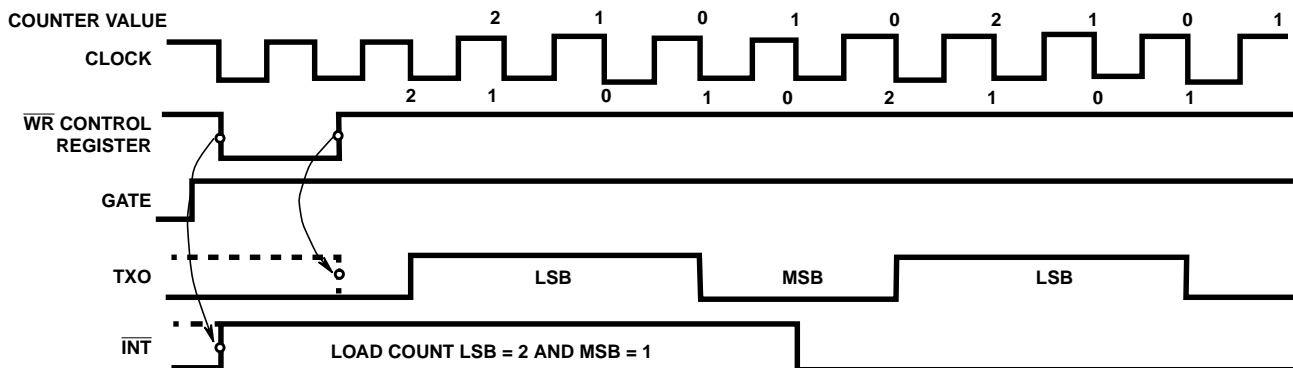


FIGURE 5. VARIABLE-DUTY CYCLE (MODE 5) TIMING WAVEFORMS

NOTE: In order to avoid unwanted starts when selecting mode 3 or 4, the gate signal must be set to the opposite level that will be programmed.

Setting the Control Register

The following will illustrate a counter write and subsequent reads that places stable, accurate values on the data bus from the counter-timer.

The counter is addressed and the required values are loaded with a write operation. The control register is addressed next and loaded with B9H.

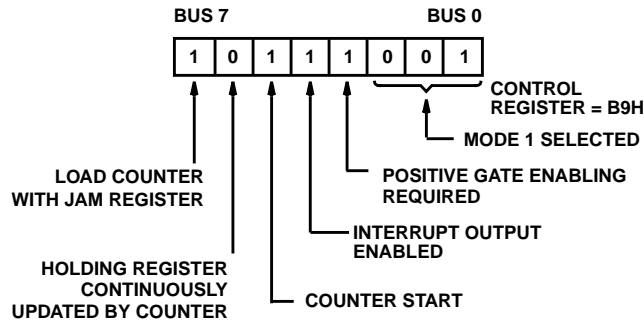


FIGURE 6.

The counter will now decrement with each input clock pulse while the gate is valid. Assuming the counter has not decremented to zero and its value is to be read without affecting the counter's operation, a write to the control register is performed. 78H is loaded into the control register.

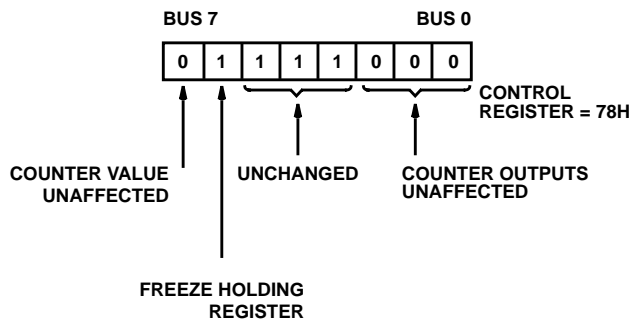


FIGURE 7.

The counter is addressed and read operations are performed.

Function Pin Description

DB7 - DB0 - 8-bit bidirectional bus used to transfer binary information between the microprocessor and the dual counter-timer.

VDD, VSS - Power and ground for device.

A0, A1, and A2 - Addresses used to select counters or registers.

TPB/ $\overline{\text{WR}}$, $\overline{\text{RD}}$ - Directional signals that determine whether data will be placed on the bus from a counter or the interrupt status register ($\overline{\text{RD}}$ active) (memory mapped), or data on the bus will be placed into a counter or control register (TPB/ $\overline{\text{WR}}$ active). The following connections are required between the microprocessor and the counter-timer in the CDP1800-series input/output mapping mode.

MICROPROCESSOR	COUNTER-TIMER
MRD	$\overline{\text{RD}}$
TPB	TPB/ $\overline{\text{WR}}$
TPA	TPA
N Lines	Address Lines

and IO/ $\overline{\text{MEM}}$ to VDD

During an output instruction, data from the memory is strobed into the counter-timer during TPB when $\overline{\text{RD}}$ is active, and latched on TPB's trailing edge. Data is read from the counter-timer when $\overline{\text{RD}}$ is not active between the trailing edges of TPA and TPB. See Figures 11, 12, and 13.

TACL, TBCL - Clocks used to decrement the counter.

TAG, TBG - Gate inputs used to control counter.

TAO, $\overline{\text{TAO}}$ - Complemented outputs of Timer A.

TBO, $\overline{\text{TBO}}$ - Complemented outputs of Timer B.

INT - Common interrupt output. Active when counter decrements to zero.

RESET - Active low signal that resets counter outputs (TAO, TBO low, $\overline{\text{TAO}}$, $\overline{\text{TBO}}$ high). The interrupt output is set high and the status register is cleared.

IO/MEM - Tied high in CDP1800-series input/output mode, otherwise tied low.

TPA - Tied to TPA of the CDP1800-series microprocessors. During memory mapping, it is used to latch the high order address bit for the chip select. In the CDP1800 input/output mode, it is used to gate the N lines. When the counter-timer is used with other microprocessors, or when the high order address of the CDP1800-series microprocessors is externally latched, it is connected to VDD.

CS - An active high signal that enables the device.

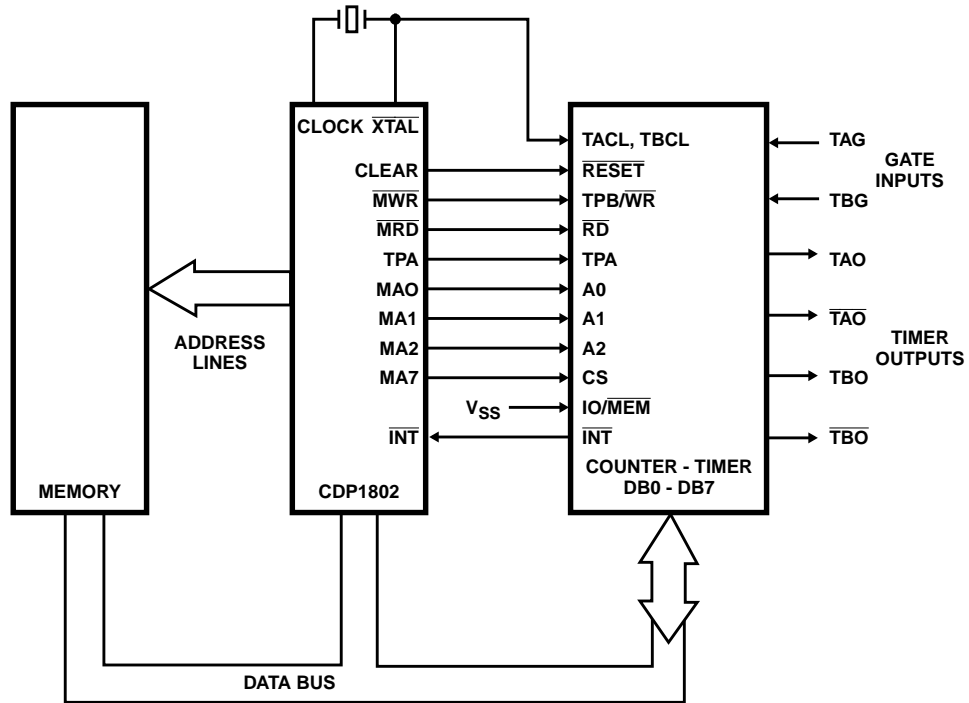


FIGURE 8. TYPICAL CDP1802 MEMORY-MAPPED SYSTEM

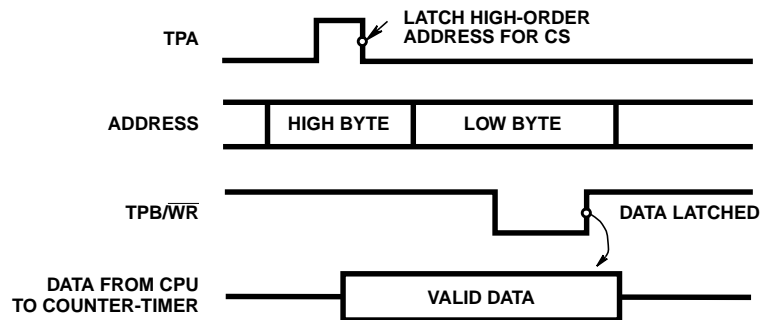


FIGURE 9. CDP1800-SERIES MEMORY-MAPPING WRITE CYCLE TIMING WAVEFORMS

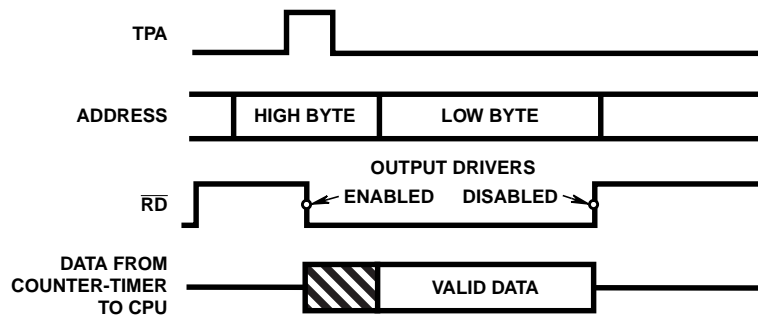


FIGURE 10. CDP1800-SERIES MEMORY-MAPPING READ CYCLE TIMING WAVEFORMS

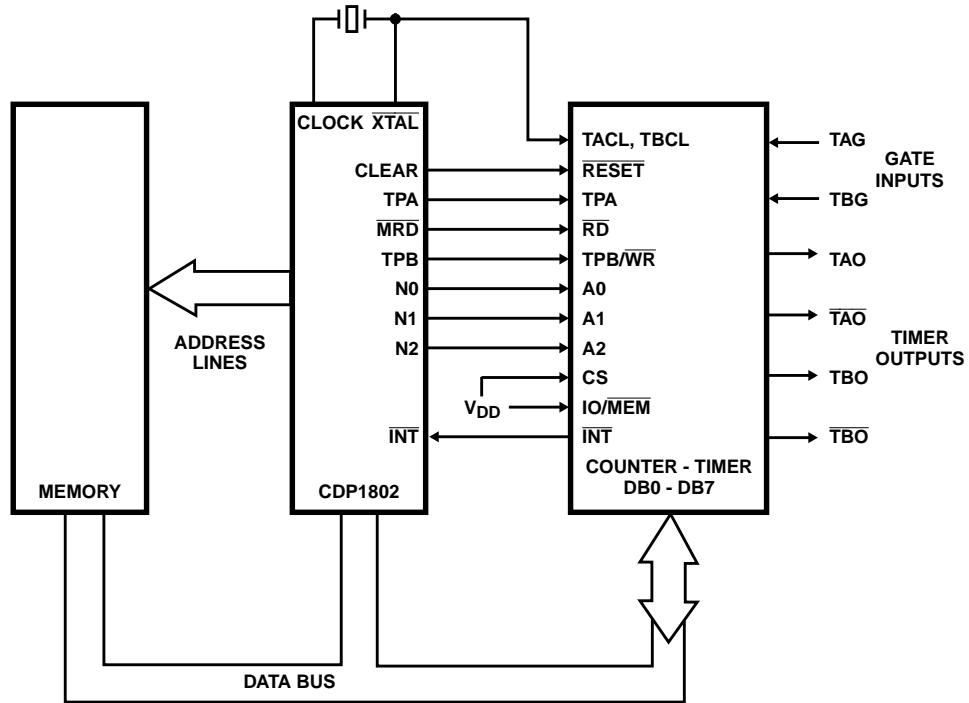


FIGURE 11. TYPICAL CDP1802 INPUT/OUTPUT-MAPPED SYSTEM

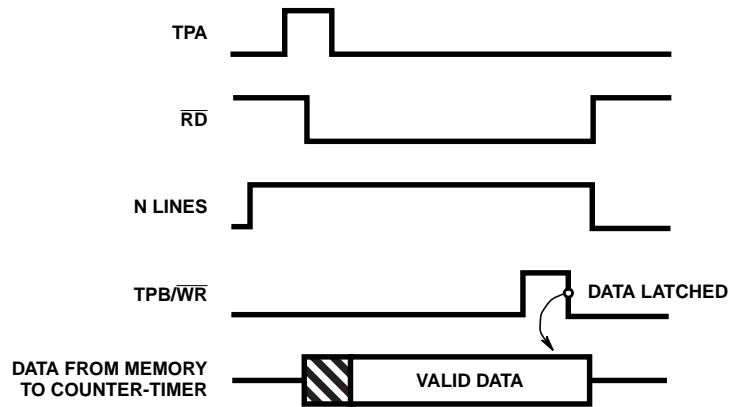


FIGURE 12. CDP1800-SERIES INPUT/OUTPUT-MAPPING TIMING WAVEFORMS WITH OUTPUT INSTRUCTION

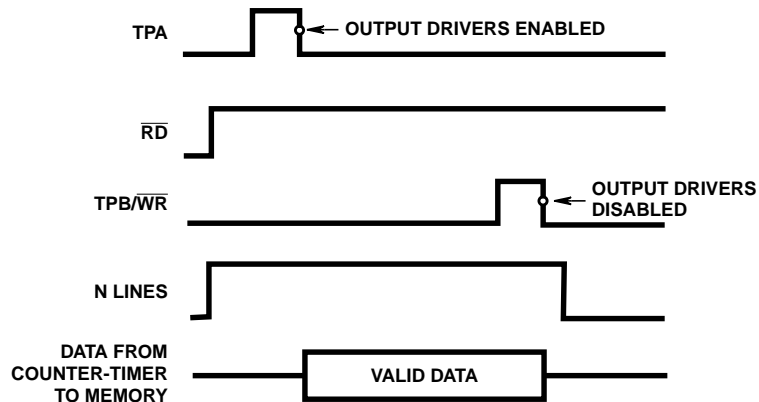


FIGURE 13. CDP1800-SERIES INPUT/OUTPUT-MAPPING TIMING WAVEFORMS WITH INPUT INSTRUCTION

Dynamic Electrical Specifications at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = 5V \pm 5\%$, Input $t_R, t_F = 10\text{ns}$, $C_L = 50\text{pF}$ and 1 TTL Load

PARAMETER	SYMBOL	(NOTE 1) MIN	(NOTE 2) TYP	MAX	UNITS
READ CYCLE TIMES (See Figure 14)					
Data Access from Address	t_{DA}	-	350	-	ns
Read Pulse Width	t_{RD}	400	-	-	ns
Data Access from Read	t_{DR}	-	250	-	ns
Address Hold after Read	t_{RH}	0	-	-	ns
Output Hold after Read	t_{DH}	50	-	-	ns
Chip Select Setup to TPA	t_{CS}	50	-	-	ns

NOTES:

1. Time required be a limit device to allow for the indicated function.
2. Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

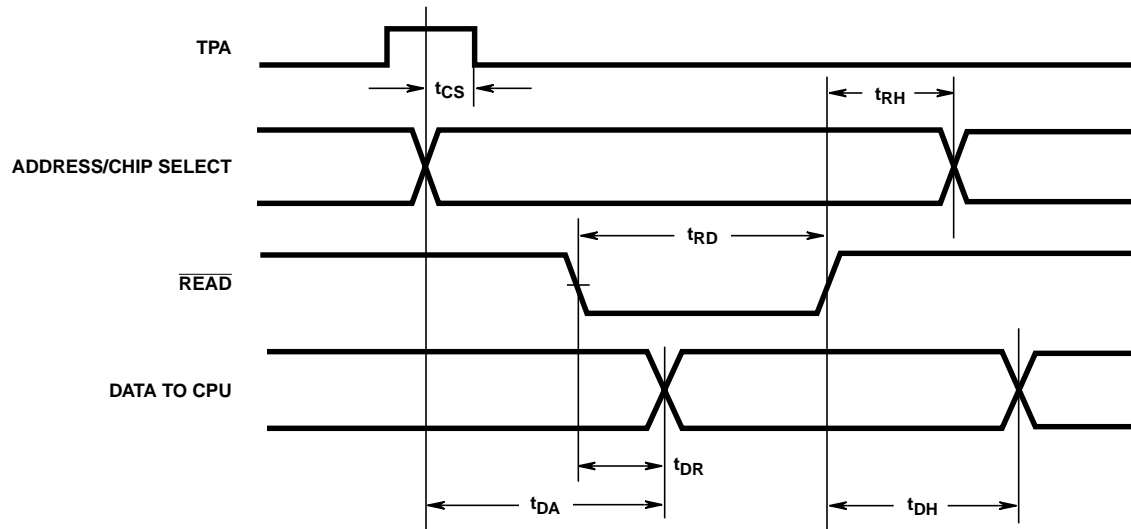


FIGURE 14. READ CYCLE TIMING WAVEFORMS

Dynamic Electrical Specifications at $T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = 5V \pm 5\%$, Input $t_R, t_F = 10\text{ns}$, $C_L = 50\text{pF}$ and 1 TTL Load

PARAMETER	SYMBOL	(NOTE 1) MIN	(NOTE 2) TYP	MAX	UNITS
WRITE CYCLE TIMES (See Figure 15)					
Address Setup to $\overline{\text{Write}}$	t_{AS}	150	-	-	ns
$\overline{\text{Write}}$ Pulse Width	t_{WR}	150	-	-	ns
Data Setup to $\overline{\text{Write}}$	t_{DS}	200	-	-	ns
Address Hold after $\overline{\text{Write}}$	t_{AH}	50	-	-	ns
Data Hold after $\overline{\text{Write}}$	t_{WH}	50	-	-	ns
Chip Select Setup to TPA	t_{CS}	50	-	-	ns

NOTES:

1. Time required by a limit device to allow for the indicated function.
2. Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

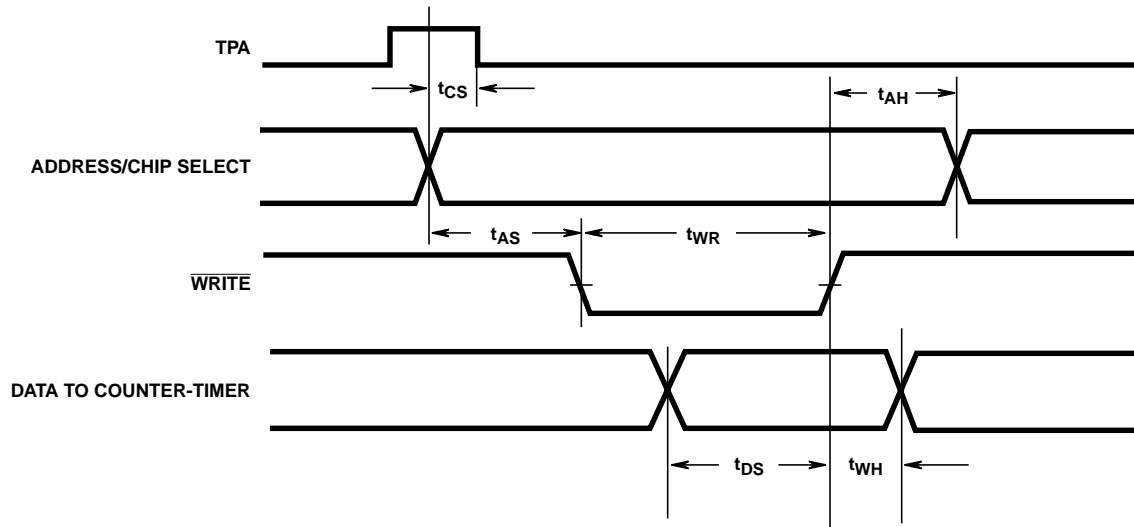


FIGURE 15. WRITE CYCLE TIMING WAVEFORMS

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