HS-3282

REFERENCE AN400

March 1997

CMOS ARINC Bus Interface Circuit

Features

- **ARINC Specification 429 Compatible**
- **Data Rates of 100 Kilobits or 12.5 Kilobits**
- **Separate Receiver and Transmitter Section**
- **Dual and Independent Receivers, Connecting Directly to ARINC Bus**
- **Serial to Parallel Receiver Data Conversion**
- **Parallel to Serial Transmitter Data Conversion**
- **Word Lengths of 25 or 32 Bits**
- **Parity Status of Received Data**
- **Generate Parity of Transmitter Data**
- **Automatic Word Gap Timer**
- **Single 5V Supply**
- **Low Power Dissipation**
- **Full Military Temperature Range**

Ordering Information

PACKAGE	TEMP. RANGE	PART NUMBER	PKG. NO.
CERDIP	-55^{o}C to +125^{o}C	HS1-3282-8	F40.6
SMD#		5962-8688001QA	F40.6
CLCC	-40^{o}C to +85^{o}C	HS4-3282-9+	J44.A
	-55^{o}C to +125^{o}C	HS4-3282-8	J44.A
SMD#		5962-8688001XA	J44.A

Description

The HS-3282 is a high performance CMOS bus interface circuit that is intended to meet the requirements of ARINC Specification 429, and similar encoded, time multiplexed serial data protocols. This device is intended to be used with the HS-3182, a monolithic DI bipolar differential line driver designed to meet the specifications of ARINC 429. The ARINC 429 bus interface circuit consists of two (2) receivers and a transmitter operating independently as shown in Figure 1. The two receivers operate at a frequency that is ten (10) times the receiver data rate, which can be the same or different from the transmitter data rate. Although the two receivers operate at the same frequency, they are functionally independent and each receives serial data asynchronously. The transmitter section of the ARINC bus interface circuit consists mainly of a First-In First-Out (FIFO) memory and timing circuit. The FIFO memory is used to hold up to eight (8) ARINC data words for transmission serially. The timing circuit is used to correctly separate each ARINC word as required by ARINC Specification 429. Even though ARINC Specification 429 specifies a 32-bit word, including parity, the HS-3282 can be programmed to also operate with a word length of 25 bits. The incoming receiver data word parity is checked, and a parity status is stored in the receiver latch and output on Pin BD08 during the 1st word. [A logic “0” indicates that an odd number of logic “1” s were received and stored; a logic “1” indicates that an even number of logic “1”s were received and stored]. In the transmitter the parity generator will generate either odd or even parity depending upon the status of PARCK control signal. A logic “0” on BD12 will cause odd parity to be used in the output data stream.

Versatility is provided in both the transmitter and receiver by the external clock input which allows the bus interface circuit to operate at data rates from 0 to 100 kilobits. The external clock must be ten (10) times the data rate to insure no data ambiguity.

The ARINC bus interface circuit is fully guaranteed to support the data rates of ARINC specification 429 over both the voltage (±5%) and full military temperature range. It interfaces with UL, CMOS or NMOS support circuitry, and uses the standard 5-volt V_{CC} supply.

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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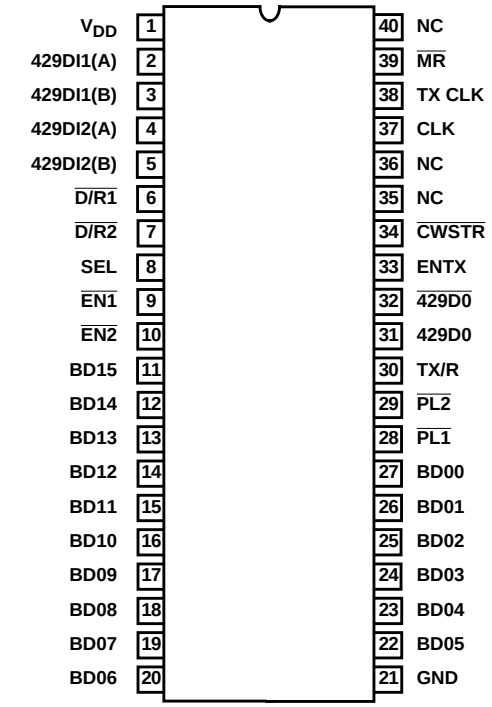
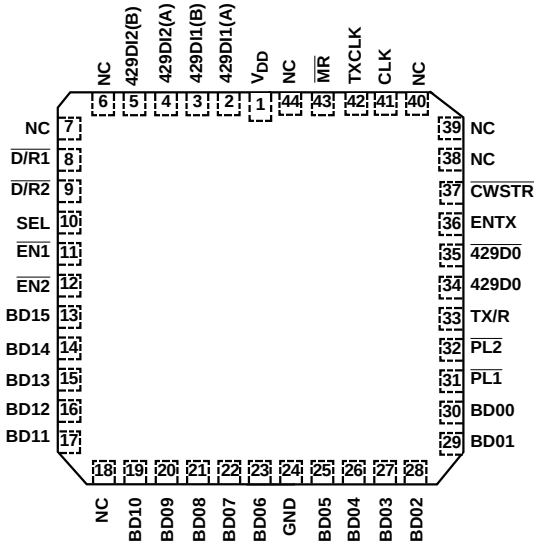
Pinouts

HS-3282 (CERDIP)
TOP VIEW



HS-3282 (CLCC)
TOP VIEW



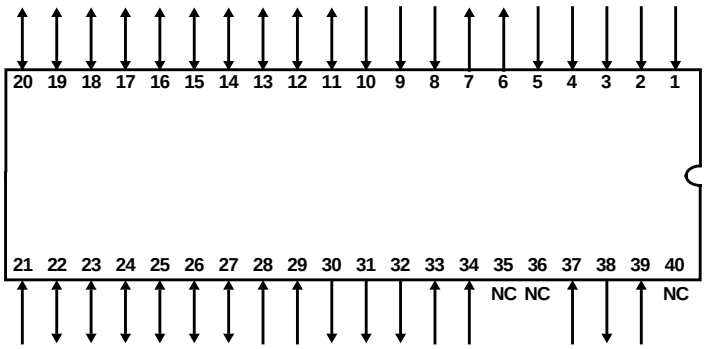
Pin Description

PIN	SYMBOL	SECTION	DESCRIPTION
1	V_{CC}	Recs/Trans	Supply pin 5 volts ±5%.
2	429 DI1 (A)	Receiver	ARINC 429 data input to Receiver 1.
3	429 DI1 (B)	Receiver	ARINC 429 data input to Receiver 1.
4	429 DI2 (A)	Receiver	ARINC 429 data input to Receiver 2.
5	429 DI2 (B)	Receiver	ARINC 429 data input to Receiver 2.
6	$\overline{D/R1}$	Receiver	Device ready flag output from Receiver 1 indicating a valid data word is ready to be fetched.
7	$\overline{D/R2}$	Receiver	Device ready flag output from Receiver 2 indicating a valid data word is ready to be fetched.
8	SEL	Receiver	Bus Data Selector - Input signal to select one of two 16-bit words from either Receiver 1 or 2.
9	$\overline{EN1}$	Receiver	Input signal to enable data from Receiver 1 onto the data bus.
10	$\overline{EN2}$	Receiver	Input signal to enable data from Receiver 2 onto the data bus.
11	BD15	Recs/Trans	Bi-directional data bus for fetching data from either of the Receivers, or for loading data into the Transmitter memory or control word register. See Control Word Table for description of Control Word bits.
12	BD14	Recs/Trans	See Pin 11.
13	BD13	Recs/Trans	See Pin 11.
14	BD12	Recs/Trans	See Pin 11.
15	BD11	Recs/Trans	See Pin 11.
16	BD10	Recs/Trans	See Pin 11.
17	BD09	Recs/Trans	See Pin 11.
18	BD08	Recs/Trans	See Pin 11.
19	BD07	Recs/Trans	See Pin 11.
20	BD06	Recs/Trans	See Pin 11.
21	GND	Recs/Trans	Circuit Ground.
22	BD05	Recs/Trans	See Pin 11.
23	BD04	Recs/Trans	See Pin 11. Control Word function not applicable.
24	BD03	Recs/Trans	See Pin 11. Control Word function not applicable.
25	BD02	Recs/Trans	See Pin 11. Control Word function not applicable.
26	BD01	Recs/Trans	See Pin 11. Control Word function not applicable.
27	BD00	Recs/Trans	See Pin 11. Control Word function not applicable.
28	$\overline{PL1}$	Transmitter	Parallel load input signal loading the first 16-bit word into the Transmitter memory.
29	$\overline{PL2}$	Transmitter	Parallel load input signal loading the first 16-bit word into the Transmitter memory and initiates data transfer into the memory stack.
30	TX/R	Transmitter	Transmitter flag output to indicate the memory is empty.

Pin Description (Continued)

PIN	SYMBOL	SECTION	DESCRIPTION
31	429D0	Transmitter	Data output from Transmitter
32	$\overline{429D0}$	Transmitter	Data output from Transmitter.
33	ENTX	Transmitter	Transmitter Enable input signal to initiate data transmission from FIFO memory.
34	$\overline{CWSTR}$	Recs/Trans	Control word input strobe signal to latch the control word from the databus into the control word register.
35	-	-	No connection. Must be left open.
36	-	-	No connection. Must be left open or tied low but never tied high.
37	CLK	Recs/Trans	External clock input. May be either ten (10) or eighty (80) times the data rate. If using both ARINC data rates it must be ten (10) times the highest data rate, (typically 1MHz).
38	TXCLK	Transmitter	Transmitter Clock output. Delivers a clock frequency equal to the transmitter data rate.
39	$\overline{MR}$	Recs/Trans	Master Reset. Active low pulse used to reset FIFO, bit counters, gap timer, word count signal, TX/R and various other flags and controls. Master reset does not reset the control word register. Usually only used on Power-Up or System Reset.
40	-	-	No Connection.

Pinout



Operational Description

The HS-3282 is designed to support ARINC Specification 429 and other serial data protocols that use a similar format by collecting the receiving, transmitting, synchronizing, timing and parity functions on a single, low power LSl circuit. It goes beyond the ARINC requirements by providing for either odd or even parity, and giving the user a choice of either 25 or 32-bit word lengths. The receiver and transmitter sections operate independently of each other. The serial-to-parallel conversion required of the receiver and the parallel-to-serial conversion requirements of the transmitter have been incorporated into the bus interface circuit.

Provisions have been made through the external clock input to provide data rate flexibility. This requires an external clock that is 10 times the data rate.

To obtain the flexibility discussed above, a number of external control signals are required, To reduce the pin count requirements, an internal control word register is used. The control word is latched from the data bus into the register by the $\overline{\text{Control}}$ $\overline{\text{Word}}$ $\overline{\text{Strobe}}$ ($\overline{\text{CWSTR}}$) signal going to a logic “1”. Eleven (11) control functions are used, and along with the Bus Data (BD) line are listed below:

Control Word

PIN NAME	SYMBOL	FUNCTION
BD05	SLFTST	Connects the self test signal from the transmitter directly to the receiver shift registers, bypassing the input receivers. Receiver 1 receives Data True and Receiver 2 receives Data Not. Note that the transmitter output remains active. (Logic “0” on SLFTST Enables Self Test).
BD06	SDENB1	Signal to Activate the Source/Destination (S/D) Decoder for Receiver 1. (Logic “1” activates S/D Decoder).
BD07	X1	If SDENB1 = “1” then this bit is compared with ARINC Data Bit #9. If Y1 also matches (see Y1), the word will be accepted by the Receiver 1. If SDENB1 = “0” this bit becomes a don’t care.
BD08	Y1	If SDENBI = “1” then this bit is compared with ARINC Data Bit #10. If X1 also matches (see X1), the word will be accepted by the Receiver 1. If SDENB1 = “0” this bit becomes a don’t care.
BD09	SDENB2	Signal to activate the Source/Destination (S/D) Decoder for Receiver 2. (Logic “1” activates S/D Decoder).
BD10	X2	If SDENB2 = “1” then this bit is compared with ARINC Data Bit #9. If Y2 also matches (see Y2), the word will be accepted by the Receiver 2. If SDENB2 = “0” this bit becomes a don’t care.
BD11	Y2	If SDENB2 = “1” then this bit is compared with ARINC Data Bit #10. If X2 also matches (see X2), the word will be accepted by the Receiver 2. If SDENB2 = “0” this bit becomes a don’t care.
BD12	PARCK	Signal used to invert the transmitter parity bit for test of parity circuits. Logic “0” selects normal odd parity. Logic “I” selects even parity.
BD13	TXSEL	Selects high or low Transmitter data rate. If TXSEL = “0” then transmitter data rate is equal to the clock rate divided by ten (10). If TXSEL = “1” then transmitter data rate is equal to the clock rate divided by eighty (80).
BD14	RCVSEL	Selects high or low Receiver data rate. If RCVSEL = “0” then the received data rate should be equal to the clock rate divided by ten (10), if RCVSEL = “1 “then the received data rate should be equal to the clock rate divided by eighty (80).
BD15	WLSEL	Selects word length. If WLSEL = “0” a 32-bit word format will be selected. If WLSEL = “1” a 25-Bit word format will be selected.

ARINC 429 DATA FORMAT as input to the Receiver and output from the Transmitter is as follows:

TABLE 1. ARINC 429 32-BIT DATA FORMAT

ARINC BIT #	FUNCTION
1 - 8	Label
9 - 10	SDI or Data
11	LSB
12 - 27	Data
28	MSB
29	Sign
30, 31	SSM
32	Parity Status

This format is shuffled when seen on the sixteen bidirectional input/outputs. The format shown below is used from the receivers and input to the transmitter:

TABLE 2A. WORD 1 FORMAT

BI-DIRECTIONAL BIT #	FUNCTION	ARINC BIT #
15, 14	Data	13, 12
13	LSB	11
12, 11	SDI or Data	10, 9
10, 9	SSM Status	31, 30
8	Parity Status	32
7 - 00	Label	1 - 8

TABLE 2B. WORD 2 FORMAT

BI-DIRECTIONAL BIT#	FUNCTION	ARINC BIT#
15	Sign	29
14	MSB	28
13 - 00	Data	27 - 14

Receiver Parity Status:

0 = Odd Parity

1 = Even Parity

If the receiver input data word string is broken before the entire data word is received, the receiver will reset and ignore the partially received data word.

If the transmitter is used to transmit consecutive data words, each word will be separated by a four (4) bit “null” state (both positive and negative outputs will maintain a zero (0) volt level.)

TABLE 3. ARINC 25-BIT DATA FORMAT

ARINC BIT #	FUNCTION
1 - 8	Label
9	LSB
11 - 23	Data
24	MSB
25	Parity Status

TABLE 4A. WORD 1 FORMAT

BI-DIRECTIONAL BIT#	FUNCTION	ARINC BIT#
15 - 9	Don’t Care	XXX
8	Parity Status	25
7 - 0	Label	1 - 8

TABLE 4B. WORD 2 FORMAT

BI-DIRECTIONAL BIT#	FUNCTION	ARINC BIT#
15	MSB	24
14 - 1	Data	23 -10
0	LSB	9

Receiver Parity Status:

0 = Odd Parity

1 = Even Parity

No Source/Destination (S/D) in 25-Bit format.

Receiver Operation

Since the two receivers are functionally identical, only one will be discussed in detail, and the block diagram will be used for reference in this discussion. The receiver consists of the following circuits:

- The **Line Receiver** functions as a voltage level translator. It transforms the 10 volt differential line voltage, ARINC 429 format, into 5 volt internal logic level.
- The output of the Line Receiver is one of two inputs to the **Self-Test Data Selector (SEL)**. The other input to the Data Selector is the Self-Test Signal from the Transmitter section.
- The incoming data, either Self-Test or ARINC 429, is double sampled by the **Word Gap Timer** to generate a Data Clock. The Receiver sample frequency (RCVCLK), 1MHz, or 125kHz, is generated by the Receiver/Transmitter Timing Circuit. This sampling frequency is ten times the Data Rate to ensure no data ambiguity.
- The derived data clock then shifts the data down a 32-Bit long **Data Shift Register** (Data S/RI). The Data Word Length is selectable for either 25 Bits or 32 Bits long by the Control Signal (WLSEL). As soon as the data word is completely received, an internal signal (WDCNT1) is generated by the Word Gap Timer Circuit.
- The Source/Destination (S/D) Decoder compares the user set code (X and Y) with Bits 9 and 10 of the Data Word. If the two codes are matched, a positive signal is generated to enable the WDCNT1 signal to latch in the received data. Otherwise, the data word is ignored and no latching action takes place. The S/D Decoder can be Enabled and Disabled by the control signal S/D ENB. If the data word is latched, an indicator flag ($\overline{D/R1}$) is set. This indicates a valid data word is ready to be fetched by the user.
- After the receiver data has been shifted down the shift register, it is placed in a holding register. The device ready flag will then be set indicating that data is ready to be fetched. If the data is ignored and left in the holding register, it will be written over when the next data word is received.
- The received data in the 32-bit holding register is placed on the bus in the form of two (2)16-bit words regardless of whether the format is for 32 or 25-bit data words. Either word can be accessed first or repeatedly until the next received data word falls into the holding register.
- The parity of the incoming word is checked and the status (i.e., logic “0” for odd parity and logic “1” for even parity) stored in the receiver latch and output on BD08 during the Word No. 1.
- Assuming the user desires to access the data, he first sets the Data Select Line (SEL) to a Logic “0” level and pulses the Enable ($\overline{EN1}$) line. This action causes the Data Selector (SELl) to select the first-data word, which contains the label field and Enable it onto the Data Bus. To obtain the second data word, the user sets the SEL line to a Logic “1” level and pulse the Enable ($\overline{EN1}$) line again. The Enable pulse duration is matched to the user circuit requirement needed to read the Data Word from the Data Bus. The second Enable pulse is also used to reset the Device Ready ($\overline{D/R1}$) flip-flop. This completes a receiving cycle.

Transmitter Operation

The Transmitter section consists of an 8-word deep by 31-Bit long FIFO Memory, Parity Generator, Transmitter Word Gap Timing Circuit and Driver Circuit.

- The FIFO Memory is organized in such a way that data loaded in the input register is automatically transferred to the output register for Serial Data Transmission. This eliminates a large amount of data managing time since the data need not be clocked from the input register to the output register. The FIFO input register is made up of two sets of 16 D-type flip-flops, which are clocked by the two parallel load signals ($\overline{PL1}$ and $\overline{PL2}$). $\overline{PL1}$ must always precede $\overline{PL2}$. Multiple $\overline{PL1}$'s may occur and data will be written over. As soon as $\overline{PL2}$ is received, data is transferred to the FIFO. The data from the Data Bus is clocked into the D-type flip-flop on the positive going edge of the PL signals. If the FIFO memory is initially empty, or the stack is not full, the data will be automatically transferred down the Memory Stack and into the output register or to the last empty FIFO storage register. If the Transmitter Enable signal (ENTX) is not active, a Logic "0", the data remains at the output register. The FIFO Memory has storage locations to hold eight 31-bit words. If the memory is full and the new data is again strobed with $\overline{PL}$, the old data at the input register is written over by the new data. Data will remain in the Memory until ENTX goes to a Logic "1". This activates the FIFO Clock and data is shifted out serially to the Transmitter Driver. Data may be loaded into the FIFO only while ENTX is inactive (low). It is not possible to write data into the FIFO while transmitting. WARNING: If $\overline{PL1}$ or $\overline{PL2}$ is applied while ENTX is high, i.e., while transmitting, the FIFO may be disrupted such that it would require a $\overline{MR}$ (Master Reset) signal to recover.
- The Output Register of the FIFO is designed such that it can shift out a word of 24 Bits long or 31 Bits long. This word length is again controlled by the WLSEL bit. The TX word Gap Timer Circuit also automatically inserts a gap equivalent to 4-Bit Times between each word. This gives a minimum requirement of 29-Bit time or 36-Bit time for each word transmission. Assuming the signal, ENTX, remains at a Logic "1", a transfer to stack signal is generated to transfer the data down the Memory Stack one position. This action is continued until the last word is shifted out of the FIFO memory. At this time a Transmitter Ready (TX/R) flag is generated to signal the user that the Transmitter is ready to receive eight more data words. During transmission, if ENTX is taken low then high again, transmission will cease leaving a portion of the word untransmitted, and the data integrity of the FIFO will be destroyed.
- A Bit Counter is used to detect the last Bit shifted out of the FIFO memory and appends the Parity Bit generated by the Parity Generator. The Parity Generator has a control signal, Parity Check (PARCK), which establishes whether odd or even parity is used in the output data word. PARCK set to a logic "0" will result in odd parity and when set to a logic "1" will result in even parity.

Sample Interface Technique

From Figure 1, one can see that the Data Bus is time shared between the Receiver and Transmitter. Therefore, bus controlling must be synchronously shared between the Receiver and the Transmitter.

Figure 2 shows the typical interface timing control of the ARINC Chip for Receiving function and for Transmitting function. Timing sequence for loading the Transmitter FIFO Memory is shown in Timing Interval A. A transmitter Ready (TX/R) Flag signals the user that the Transmitter Memory is empty. The user then Enables the Transmitter Data, a 16-Bit word, on the Data Bus and strobes the Transmitter with a Parallel Load ($\overline{PL1}$) Signal. The second part of the 32-Bit word is similarly loaded into the Transmitter with $\overline{PL2}$, which also initiates data transfer to stack. This is continuous until the Memory is full, which is eight 31-Bit words. The user must keep track of the number of words loaded into the Memory to ensure no data is written over by other data. During the time the user is loading the Transmitter, he does not have to service the Receiver, even if the Receiver flags the user with the signal $\overline{D/R1}$ that a valid received word is ready to be fetched. This is shown by the Timing interval B. If the user decides to obtain the received data before the Transmitter is completely loaded, he sets the two parallel load signals ($\overline{PL1}$ and $\overline{PL2}$) at a Logic "1" state, and strobes $\overline{EN1}$ while the signal SEL is at a Logic "0" state. After the negative edge of $\overline{EN1}$, the first 16-Bit segment of the received word becomes valid on the Data Bus. At the positive edge of $\overline{EN1}$, the user should toggle the signal SEL to ready the Receiver for the second 16-Bit word. Strobing the Receiver with $\overline{EN1}$, the second time, enables the second 16-Bit word and resets the Receiver Ready Flag $\overline{D/R1}$. The user should now reset the signal SEL to a Logic "0" state to ready the Receiver for another Read Cycle. During the time period that the user is fetching the received words, he can load the transmitter. This is done by interlacing the $\overline{PL}$ signals with the $\overline{EN}$ signals as shown in the Timing Interval B. Servicing the Receiver 2 is similar and is illustrated by Timing interval C. Timing interval D shows the rest of the Transmitter loading sequence and the beginning of the transmission by switching the signal TX Enable to a Logic "1" state. Timing interval E is the time it takes to transmit all data from the FIFO Memory, either 288 Bit times or 232 Bit times.

Repeater Operation

This mode of operation allows a data word that has been received to be placed directly in the FIFO for transmission. A timing diagram is shown in Figure 7. A 32-bit word is used in this example. The data word is shifted into the shift register and the $\overline{D/R}$ flag goes low. A logic "0" is placed on the SEL line and $\overline{EN1}$ is strobed. This is the same as the normal receiver operation and places half the data word (16 bits) on the data bus. By strobing $\overline{PL1}$ at the same time as $\overline{EN1}$, these 16 bits will be taken off the bus and placed in the FIFO. SEL is brought back high and $\overline{EN1}$ is strobed again for the second 16 bits of the data word. Again by strobing $\overline{PL2}$ at the same time the second 16 bits will be placed in the FIFO. The parity bit will have been stripped away leaving the 31-bit data word in the FIFO ready for transmission as shown in Figure 6.

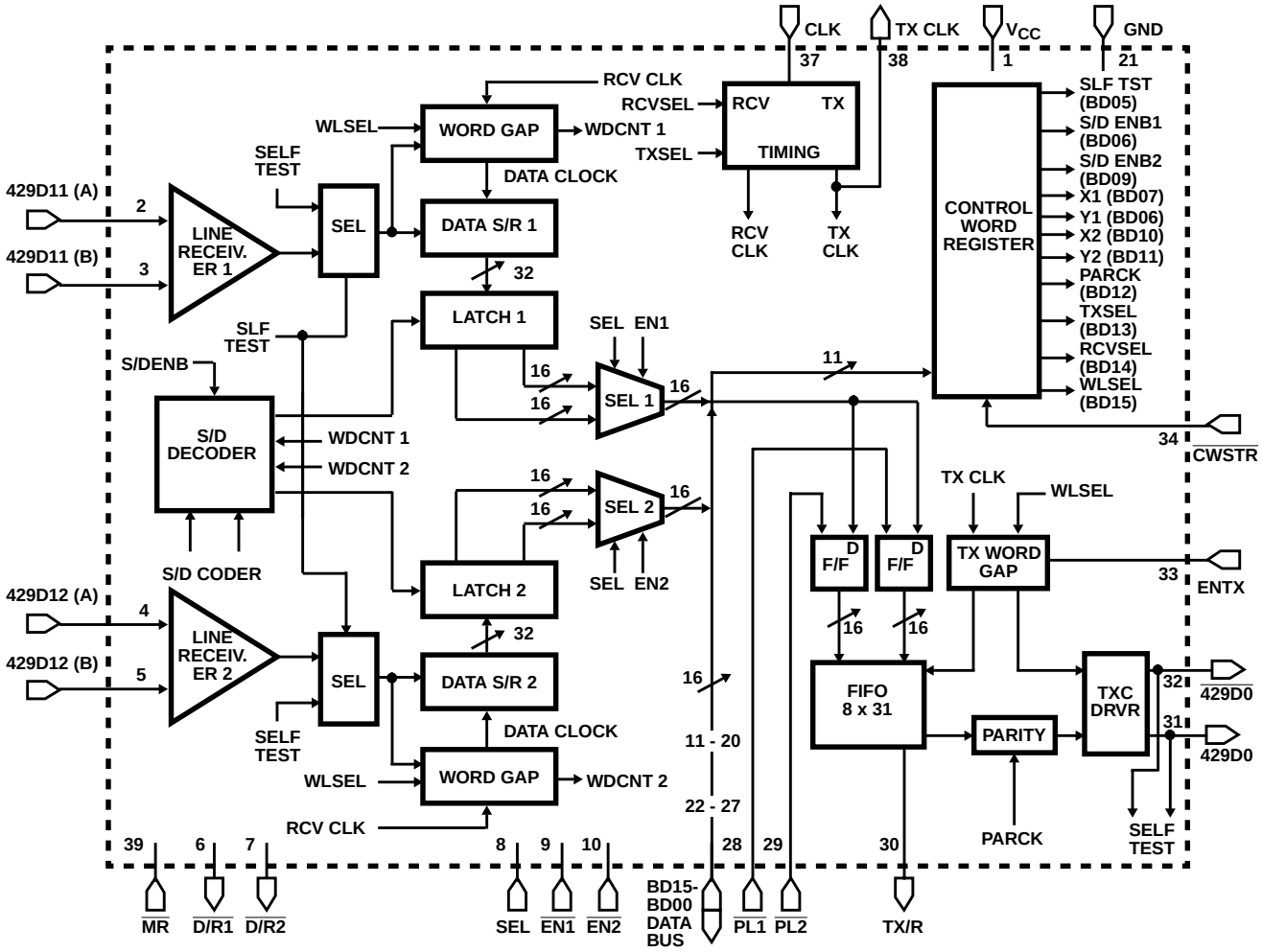


FIGURE 1. SINGLE CHIP ARINC 429 INTERFACE FUNCTIONAL BLOCK DIAGRAM

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage Applied
(Except Pins 2 - 5) . . . . . GND -0.3V to V_{DD} +0.3V
Input Voltage Applied (Pins 2 - 5) . . . . . -29V to +29V
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.75V to +5.25V
Operating Temperature Range
HS-3282-5. . . . . 0^oC to $+70^oC$
HS-3282-8. . . . . -55^oC to $+125^oC$

Thermal Information

Thermal Resistance	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CDIP Package	35	8
CLCC Package	55	12

Maximum Junction Temperature . . . . . $+175^oC$
Maximum Storage Temperature Range . . . . . -65^oC to $+150^oC$
Maximum Lead Temperature (Soldering 10s) . . . . . $+300^oC$

Die Characteristics

Gate Count . . . . . 2632 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Performance Specifications

V_{DD} = 5V ±5%, T_A = 0^oC to $+70^oC$ (HS-3282-5), T_A = -55^oC to $+125^oC$ (HS-3282-8)

PARAMETER	SYMBOL	CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
ARINC INPUTS Pins 2-3,4-5					
Logic "1" Input Voltage	V_{IH}	V_{DD} = 5.25V	6.7	13.0	V
Logic "0" Input Voltage	V_{IL}	V_{DD} = 5.25V	-13.0	-6.7	V
Null Input Voltage	V_{NUL}	V_{DD} = 4.75V, 5.25V	-2.5	+2.5	V
Common Mode Voltage	V_{CH}	V_{DD} = 4.75V, 5.25V	-5.0	+5.0	V
Input Leakage	I_{IH}	V_{DD} = 5.25V, V_{IN} = ±6.5V	-	200	µA
Input Leakage	I_{IL}	V_{DD} = 5.25V, V_{IN} = 0.0V	-450	-	µA
Differential Input Impedance	RI	V_{DD} = 5.25V, V_{IN} = +5V, -5V	12	-	kΩ
Input Impedance to V_{DD}	RH	V_{DD} = 5.25V, V_{IN} = 0V	12	-	kΩ
Input Impedance to GND	RG	V_{DD} = Open, V_{IN} = 5.0V	12	-	kΩ
BIDIRECTIONAL INPUTS Pins 11-20, 22-27					
Logic "1" Input Voltage	V_{IH}	V_{DD} = 5.25V	2.1	-	V
Logic "0" Input Voltage	V_{IL}	V_{DD} = 4.75V	-	0.7	V
Input Leakage	I_{IH}	V_{DD} = 5.25V,V_{IN} = 5.25V	-	1.5	µA
Input Leakage	I_{IL}	V_{DD} = 5.25V, V_{IN} = 0.0V	-1.5	-	µA
ALL OTHER INPUTS Pins 8-10, 28, 29, 33, 34, 37, 39					
Logic "1" Input Voltage	V_{IH}	V_{DD} = 5.25V	3.5	-	V
Logic "0" Input Voltage	V_{IL}	V_{DD} = 4.75V	-	0.7	V
Input Leakage	I_{IH}	V_{DD} = 5.25V, V_{IN} = 5.25V	-	10	µA
Input Leakage	I_{IL}	V_{DD} = 5.25V, V_{IN} = 0.0V	-75	-	µA
OUTPUTS Pins 6, 7, 11-20, 22-27, 30-32, 38, Supply Pin 1					
Logic "1" Output Voltage	V_{OH}	V_{DD} = 4.75V, I_{OH} = -1.5mA	2.7	-	V
Logic "0" Output Voltage	V_{OL}	V_{DD} = 4.75V I_{OL}= 1.8mA	-	0.4	V
Standby Supply Current	I_{CC1}	V_{DD} = 5.25V, V_{IN} = 0V Except 9,10, 29 = 5.25V	-	20	mA
Operating Supply Current	I_{CC2}	V_{DD} = 5.25V, V_{IN} = 5.25V Except 8, 33 = 0.0V, CLK = 1MHz	-	20	mA

AC Electrical Performance Specifications V_{DD} = 5V ±5%, T_A = 0°C to +70°C (HS-3282-5), T_A = -55°C to +125°C (HS-3282-8)

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Clock Frequency	FC	V_{DD} = 4.75V, 5.25V	-	1	MHz
Data Rate 1/	FD	V_{DD} = 4.75V, 5.25V	-	100	kHz
Data Rate 2/	FD	V_{DD} = 4.75V, 5.25V	-	12.5	kHz
Master Reset Pulse Width	TMR	V_{DD} = 4.75V, 5.25V	200	-	ns
RECEIVER TIMING					
Receiver Ready Time From 32nd Bit 1/	TD/R2	V_{DD} = 4.75V, 5.25V	-	16	µs
Receiver Ready Time From 32nd Bit 2/	TD/R2	V_{DD} = 4.75V, 5.25V	-	128	µs
Device Ready to Enable Time	TD/REN	V_{DD} = 4.75V, 5.25V	0	-	ns
Data Enable Pulse Width	TEN	V_{DD} = 4.75V, 5.25V	200	-	ns
Data Enable to Data Enable Time	TENEN	V_{DD} = 4.75V, 5.25V	50	-	ns
Data Enable to Device Ready Reset Time	TEND/R	V_{DD} = 4.75V, 5.25V	-	200	ns
Output Data Valid to Enable Time	TENDATA	V_{DD} = 4.75V, 5.25V	-	200	ns
Data Enable to Data Select Time	TENSEL	V_{DD} = 4.75V, 5.25V	20	-	ns
Data Select to Data Enable Time	TSELEN	V_{DD} = 4.75V, 5.25V	20	-	ns
Output Data Disable Time	TDATAEN	V_{DD} = 4.75V, 5.25V	-	80	ns
CONTROL WORD TIMING					
Control Word Strobe Pulse Width	TCWSTR	V_{DD} = 4.75V, 5.25V	130	-	ns
Control Word Setup Time	TCWSET	V_{DD} = 4.75V, 5.25V	130	-	ns
Control Word Hold Time	TCWHLD	V_{DD} = 4.75V, 5.25V	0	-	ns
TRANSMITTER FIFO Write Timing					
Parallel Load Pulse Width	TPL	V_{DD} = 4.75V, 5.25V	200	-	ns
Parallel Load to Parallel Load 2 Delay	TPL12	V_{DD} = 4.75V, 5.25V	0	-	ns
Transmitter Ready Delay Time	TTX/R	V_{DD} = 4.75V, 5.25V	-	840	ns
Data Word Setup Time	TDWSET	V_{DD} = 4.75V, 5.25V	110	-	ns
Data Word Hold Time	TDWHLD	V_{DD} = 4.75V, 5.25V	0	-	ns
TRANSMITTER Output Timing					
Enable Transmit to Output Data Valid Time 1/	TENDAT	V_{DD} = 4.75V, 5.25V	-	25	µs
Enable Transmit to Output Data Valid Time 2/	TENDAT	V_{DD} = 4.75V, 5.25V	-	200	µs
Output Data Bit Time 1/	TBIT	V_{DD} = 4.75V, 5.25V	4.95	5.05	µs
Output Data Bit Time 2/	TBIT	V_{DD} = 4.75V, 5.25V	39.6	40.4	µs
Output Data Null Time 1/	TNULL	V_{DD} = 4.75V, 5.25V	4.95	5.05	µs
Output Data Null Time 2/	TNULL	V_{DD} = 4.75V, 5.25V	39.6	40.4	µs

AC Electrical Performance Specifications V_{DD} = 5V ±5%, T_A = 0°C to +70°C (HS-3282-5), T_A = -55°C to +125°C (HS-3282-8) **(Continued)**

PARAMETER	SYMBOL	CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Data Word Gap Time 1/	TGAP	V_{DD} = 4.75V, 5.25V	39.6	40.4	µs
Data Word Gap Time 2/	TGAP	V_{DD} = 4.75V, 5.25V	316.8	323.2	µs
Data Transmission Word to TX/R Set Time	TDTX/R	V_{DD} = 4.75V, 5.25V	-	400	ns
Enable Transmit Turnoff Time	TENTX/R	V_{DD} = 4.75V, 5.25V	0	-	ns
REPEATER OPERATION TIMING					
Data Enable to Parallel Load Delay Time	TENPL	V_{DD} = 4.75V, 5.25V	0	-	ns
Data Enable Hold for Parallel Load Time	TPLEN	V_{DD} = 4.75V, 5.25V	0	-	ns
Enable Transmit Delay Time	TTX/REN	V_{DD} = 4.75V, 5.25V	0	-	ns

NOTES:

1. 100kHz Data Rate.
2. 12.5kHz Data Rate.

Electrical Performance Specifications V_{DD} = 5V ±5%, T_A = 0°C to +70°C (HS-3282-5), T_A = -55°C to +125°C (HS-3282-8)

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Differential Input Capacitance	CD	V_{DD} = Open, f = 1MHz, Note 2, 3	-	20	pF
Input Capacitance to V_{DD}	CH	V_{DD} = GND, f = 1MHz, Note 2, 3	-	20	pF
Input Capacitance to GND	CG	V_{DD} = Open, f = 1MHz, Note 2, 3	-	20	pF
Input Capacitance	CI	V_{DD} = Open, f = 1MHz, Note 2, 4	-	15	pF
Output Capacitance	CO	V_{DD} = Open, f = 1MHz, Note 2, 5	-	15	pF
Clock Rise Time	TLHC	CLK = 1MHz, From 0.7V to 3.5V	-	10	ns
Clock Fall Time	THLC	CLK = 1MHz, From 3.5V to 0.7V	-	10	ns
Input Rise Time	TLHI	From 0.7V to 3.5V, Note 6	-	15	ns
Input Fall Time	THLI	From 3.5V to 0.7V, Note 6	-	15	ns

NOTES:

1. The parameters listed in this table are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes affecting these parameters.
2. All measurements are referenced to device GND.
3. Pins 2-3, 4-5.
4. Pins 8-10, 28, 29, 33, 34, 37, 39.
5. Pins 6, 7, 11-20, 22-27, 30-32, 38.
6. Pins 8-20, 22-29, 33, 34.

Timing Waveforms

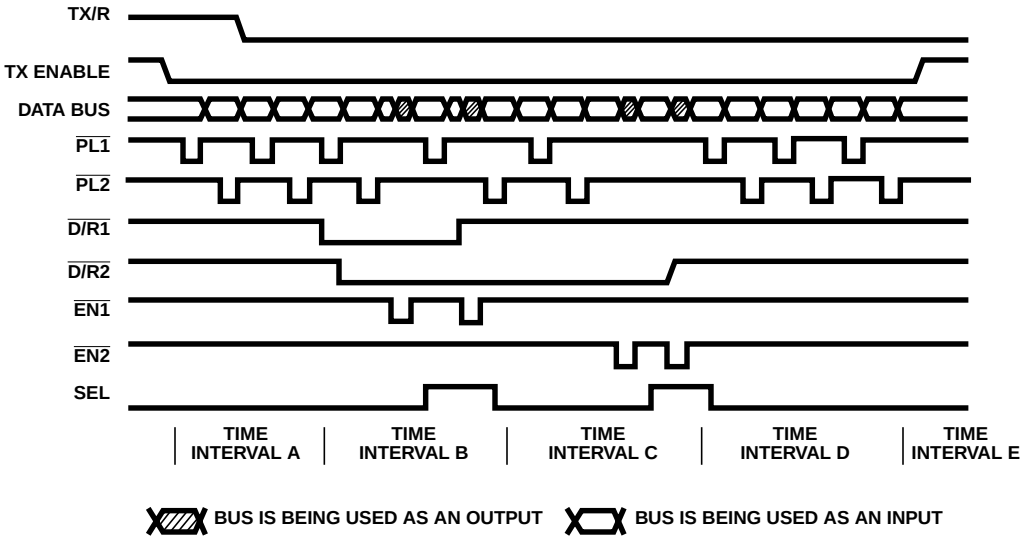


FIGURE 2. TYPICAL INTERFACE TIMING SEQUENCE

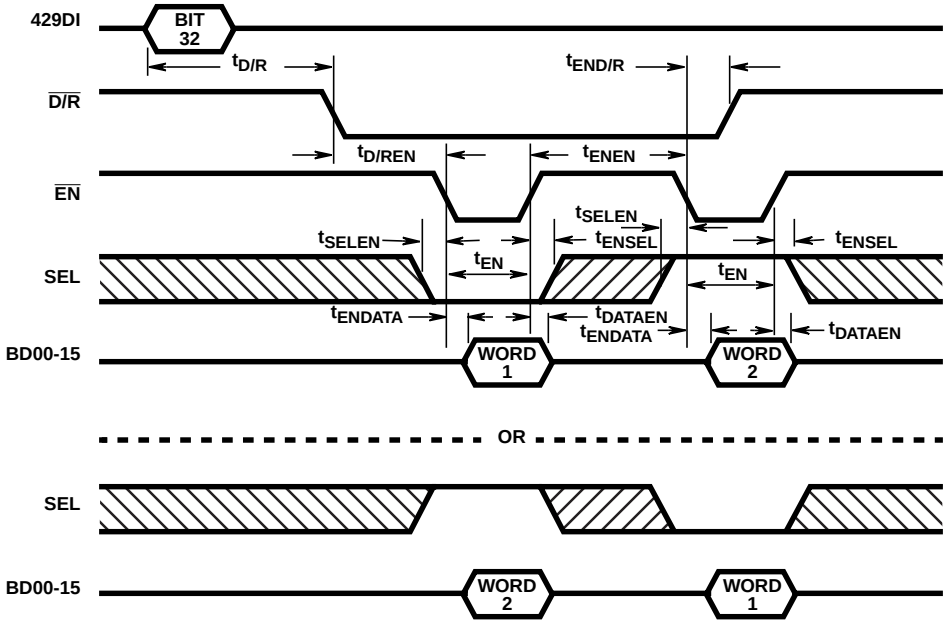


FIGURE 3. RECEIVER TIMING

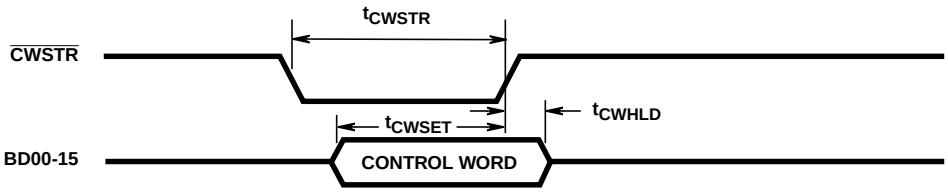


FIGURE 4. CONTROL WORD TIMING

Timing Waveforms (Continued)

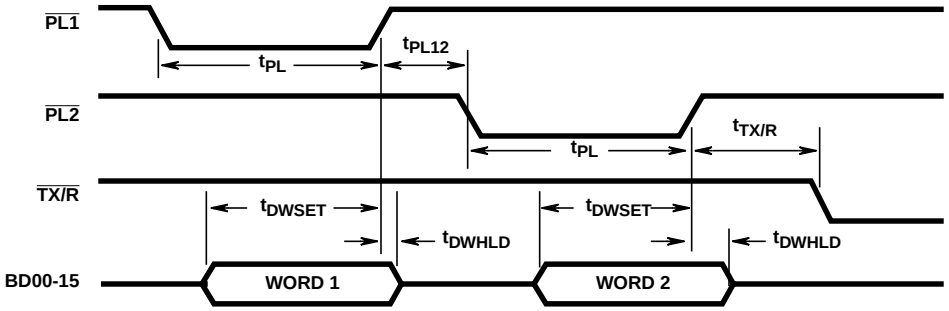


FIGURE 5. TRANSMITTER FIFO WRITE TIMING

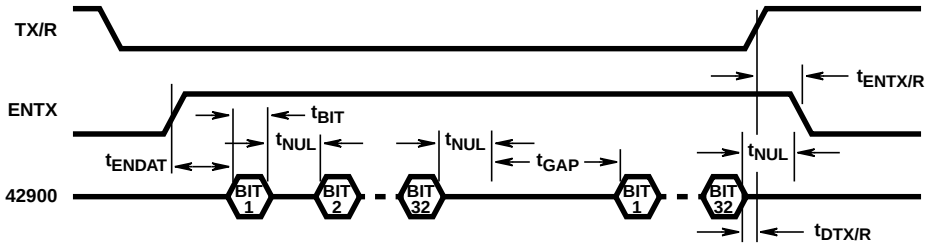


FIGURE 6. TRANSMITTER OUTPUT TIMING

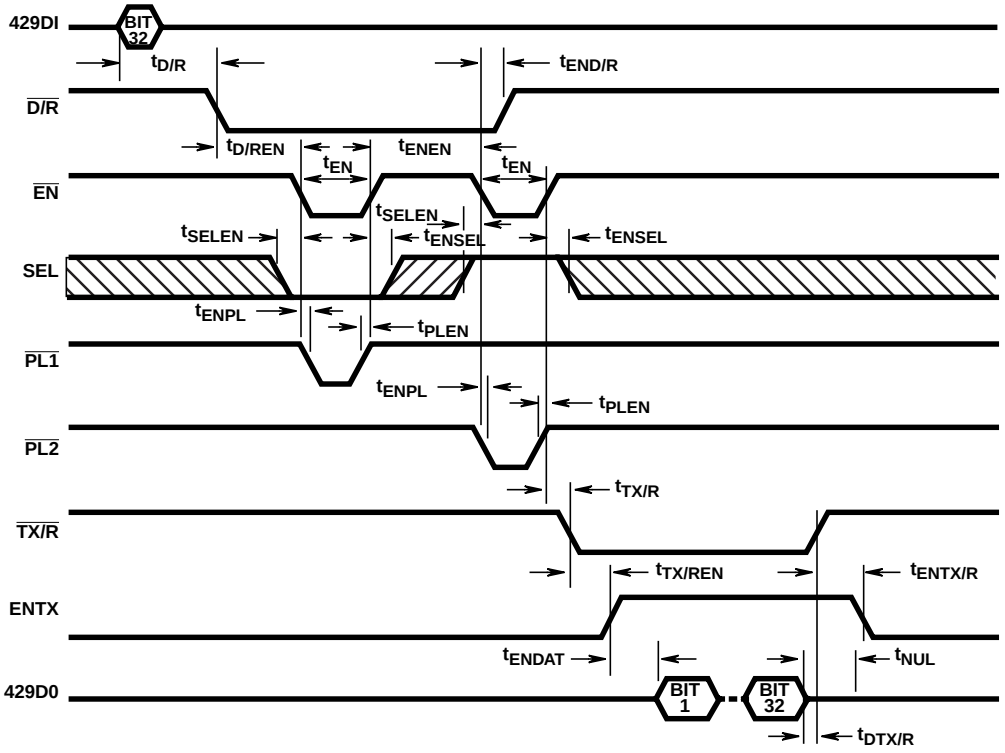
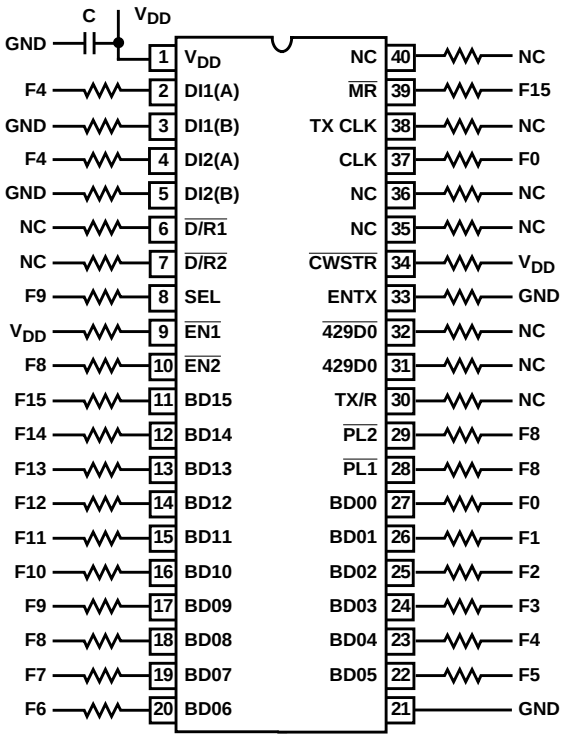


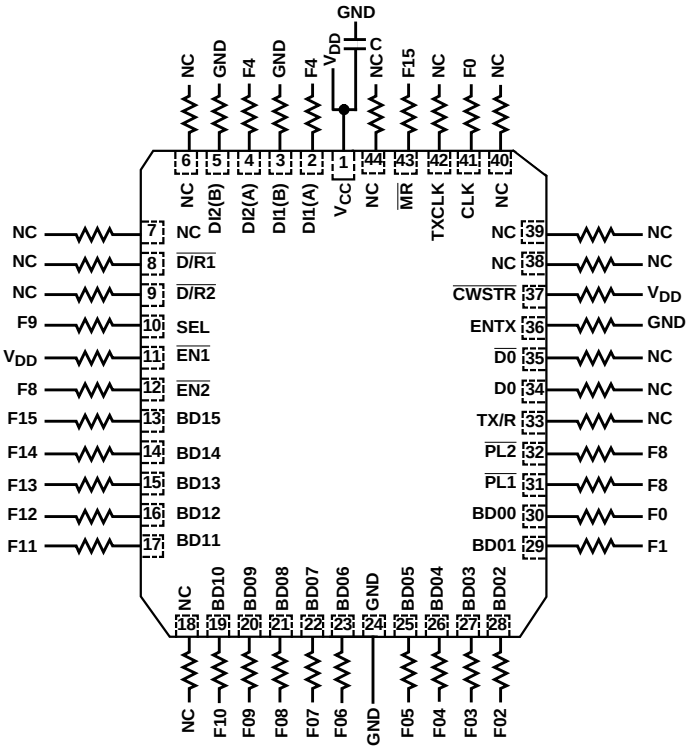
FIGURE 7. REPEATER OPERATION TIMING

Burn-In Circuits

HS-3282 CERDIP



HS-3282 CLCC



NOTES:

1. Resistors = 47kΩ, 5%, 1/4W (Min)
2. GND = Ground
3. V_{DD} = +5.5V, ±0.5V
4. C = 0.01mF/Socket (Min)
5. F0 = 100kHz, F1 = F0/2, . . . F15 = F14/2

Die Characteristics

DIE DIMENSIONS:
246 x 224 x 19 mils)
(6250 x 5700 x 483µm)

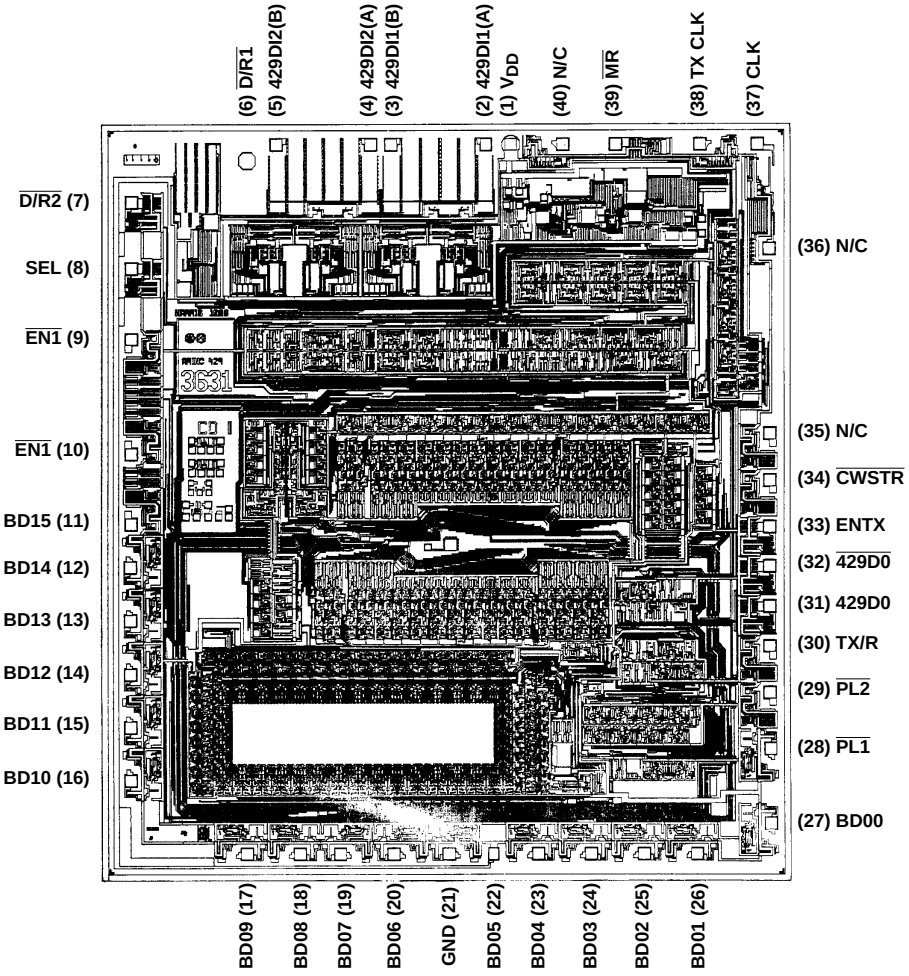
METALLIZATION:
Type: Si-Al
Thickness: 11kÅ ±2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kA ±1kÅ

WORST CASE CURRENT DENSITY:
2 x 10^5 A/cm^2

Metallization Mask Layout

HS-3282



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