CDP68HC05J3

December 1994

8-Bit Microcontroller Series

Features

The following are some of the hardware and software highlights of the CDP68HC05J3 family of HCMOS Microcomputers.

HARDWARE FEATURES

- **HCMOS Technology**
- **8-Bit Architecture**
- **Power-Saving STOP, WAIT, and Data Retention Modes**
- **Fully Static Operation**
- **On-Chip Memory**
  - **2,352 bytes of ROM**
  - **128 bytes of RAM**
- **12 Bidirectional I/O Lines**
  - **8 Software Programmable as Open Drain**
  - **4 Interruptible Inputs**
- **Internal 16-Bit Timer**
  - **Output Compare**
  - **Input Capture**
  - **Separate Timer Oscillator Allows:**
    - **Timing During Power Saving Mode**
    - **Counting of External Events**
- **Self-Check Mode**
- **External, Timer, and Port B Interrupts**
- **Master Reset and Power-On Reset**
- **On-Chip Oscillator with RC or Crystal Mask Options**
- **CDP68HC05J3**
  - **4.2MHz Operating Frequency (2.1MHz Internal Bus Frequency) at 5V; 2.0MHz at 3.0V**
  - **Single 3.0V to 8.0V Supply (2.0V Data Retention)**
- **CDP68HCL05J3**
  - **Lower Supply Current, I_{DD} in RUN, WAIT and STOP Modes at 5.5V, 3.6V and 2.4V**
  - **Single 2.4V to 6.0V Supply (2V Data Retention)**
- **CDP68HSC05J3**
  - **8.0MHz Operating Frequency (4.0MHZ Internal Bus Frequency)**
  - **Single 3.0V to 6.0V Supply (2.0V Data Retention)**

SOFTWARE FEATURES

- **Supports Full CDP68HC05 Instruction Set**
- **8 x 8 Unsigned Multiply Instruction**
- **True Bit-Manipulation**
- **Two Power Saving Standby Modes**
- **Efficient Use of Program Space**
- **Memory Mapped I/O**

Description

The CDP68HC05J3 HCMOS Microcomputer is a member of the CDP68HC05 family of single chip microcomputers. This 8-bit microcomputer unit (MCU) contains a CPU, 128 bytes of RAM, 2,352 bytes of masked ROM, a flexible 16-bit timer with input capture and output compare features, 12 bidirectional I/O lines (eight programmable as open drain outputs and four programmable as interruptible inputs), an on-chip oscillator, and an optional, independent oscillator for the 16-bit timer. The fully static design allows operation at frequencies down to DC, further reducing the already low, power consumption.

The timer can be used for pulse width measurements, timing, or event counting. Optionally, the timer can run off an oscillator that is independent of (and typically at a lower frequency than) the CPU oscillator. The dedicated timer oscillator allows timekeeping functions to be maintained during the low power STOP mode.

In conjunction with the open drain outputs, the four interruptible Port B lines can be used for switch scanning.

The interruptible port lines provide additional interrupts and can be used to exit the power down modes.

The CDP68HCL05J3 MCU device is a low-power version of the CDP68HC05J3 with lower power consumption in the RUN, WAIT, and STOP modes; and low voltage operation down to 2.4V.

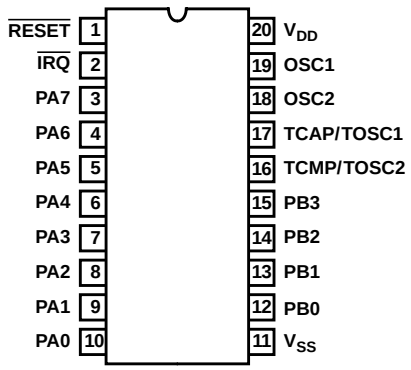
The CDP68HSC05J3 MCU device is a high-speed version of the CDP68HC05J3 with up to 8.0MHz operation.

The CDP68HC05J3 family supports the full CDP68HC05 instruction set. Development can be performed with tools supplied by Intersil or offered by numerous third party vendors. Available tools include assemblers, C compilers, and ICE systems.

The CDP68HC05J3 is supplied in a 20 lead dual-in-line plastic package (E suffix) and in a 20 lead small outline plastic package (M suffix).

Pinout

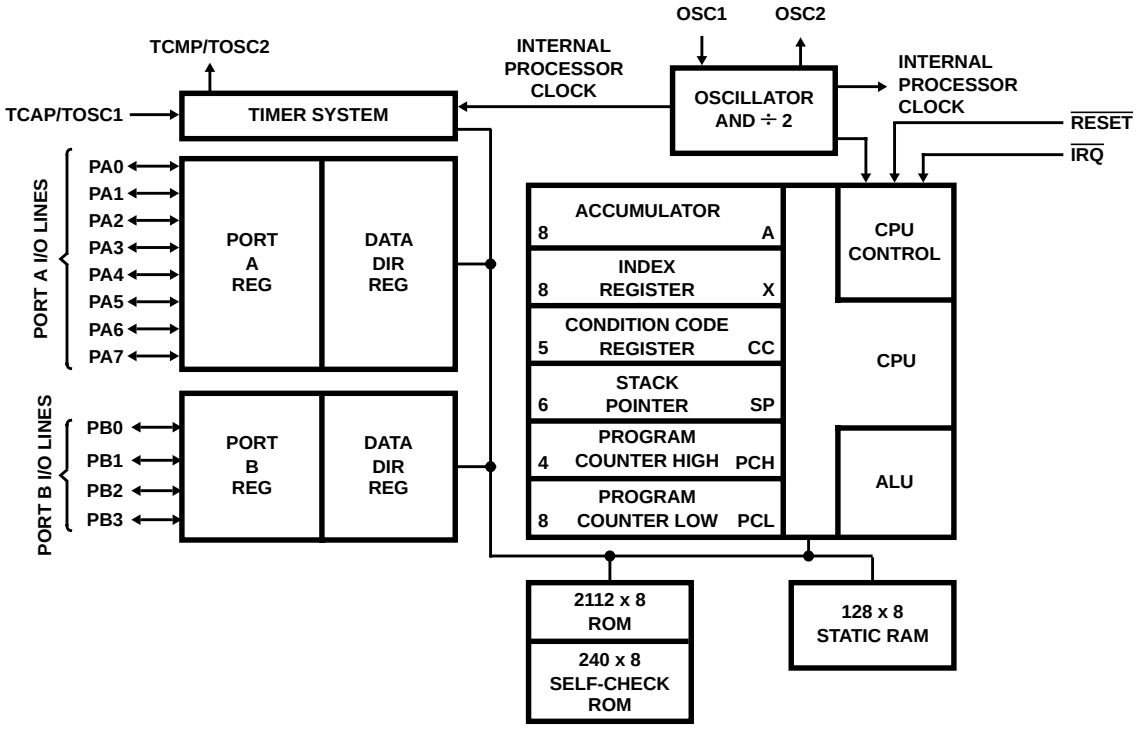
CDP68HC05J3 (SOIC, PDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

File Number **2757.2**

Block Diagram



Power Considerations

The average chip-junction temperature, T_J, in ^oC can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad \text{(EQ. 1)}$$

Where: T_A = Ambient Temperature, ^oC
θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, $^oC/W$
$P_D = P_{INT} + P_{I/O}$
$P_{INT} = I_{CC} \times V_{CC}$, Watts - Chip Internal Power
$P_{I/O}$ = Power Dissipation on Input and Output Pins - User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

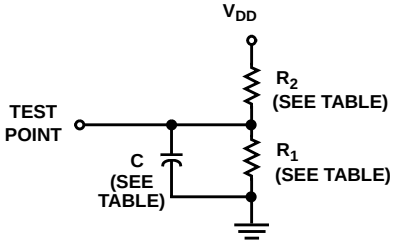
$$P_D = K \div (T_J + 273^oC) \quad \text{(EQ. 2)}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \bullet (T_A + 273^oC) + \theta_{JA} \bullet P_D 2 \quad \text{(EQ. 3)}$$

Where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

PINS	R1	R2	C
V_{DD} = 4.5V: PA0-7, PB0-3	3.26Ω	2.38Ω	50pF
V_{DD} = 3.0V: PA0-7, PB0-3	10.19Ω	6.32Ω	50pF



EQUIVALENT TEST LOAD

Absolute Maximum Ratings

Supply Voltage (V_{DD}) . . . . . -0.5V to +7.0V
Input Voltage (V_{IN}) . . . . . V_{SS} -0.3V to V_{DD} +0.3V
Self-Check Mode (V_{IN})
  $\overline{IRQ}$ Pin Only . . . . . V_{SS} -0.3V to 2 x V_{DD} +0.3V
Current Drain Per Pin (I)
  Excluding V_{DD} and V_{SS} 25mA
Storage Temperature Range (T_{STG}) . . . . . -65^oC to $+150^oC$

Thermal Information

Thermal Resistance θ_{JA}
  Plastic DIP Package . . . . . $60^oC/W$
  Plastic SOIC Package . . . . . $75^oC/W$
Junction Temperature . . . . . $+150^oC$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range (T_A) . . . . . -40^oC to $+125^oC$
  Low Power . . . . . 0^oC to $+70^oC$
  High Speed . . . . . 0^oC to $+70^oC$

Input High Voltage . . . . . .($0.8 \bullet V_{DD}$) to V_{DD}

DC Electrical Specifications

V_{DD} = 5V ±10%, V_{SS} = 0V, T_A = -40^oC to $+125^oC$, Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	V_{OL}	I_{LOAD} <10µA	-	-	0.1	V
	V_{OH}		V_{DD} -0.1	-	-	V
Output High Voltage: PA0-7, PB0-3, TCMP	V_{OH}	I_{LOAD} = -0.8mA	V_{DD} -0.8	-	-	V
Output Low Voltage: PA0-7, PB0-3, TCMP	V_{OL}	I_{LOAD} = 1.6mA	-	-	0.4	V
Input High Voltage: PA0-7, PB0-3, OSC1, TCAP/TOSC1	V_{IH}		-	$0.5 \bullet V_{DD}$	$0.7 \bullet V_{DD}$	V
Input High Voltage: $\overline{RESET}$, $\overline{IRQ}$	V_{IH}		-	$0.5 \bullet V_{DD}$	3.5	V
Input Low Voltage: PA0-7, PB0-3, OSC1, TCAP/TOSC1	V_{IL}		$0.3 \bullet V_{DD}$	$0.5 \bullet V_{DD}$	-	V
Input Low Voltage: $\overline{RESET}$, $\overline{IRQ}$	V_{IL}		0.8	$0.3 \bullet V_{DD}$	-	V
Input Hysteresis Voltage: $\overline{RESET}$, $\overline{IRQ}$	V_{HYS}		0.5	1.0	-	V
Data Retention Voltage	VRM	0^oC to $+70^oC$	2	-	-	V
Supply Current (Notes 1, 2)						
RUN	I_{RUN}		-	2.0	4.0	mA
WAIT	I_{WAIT}		-	0.8	1.6	mA
STOP	I_{STOP}	T_A = -40^oC to $+125^oC$	-	20	40	µA
I/O Ports Hi-Z Leakage Current: PA0-7, PB0-3	I_{IL}		-	-	±10	µA
Input Current: $\overline{RESET}$, $\overline{IRQ}$, TCAP/TOSC1, OSC1	I_{IN}		-	-	±1	µA
Capacitance: (Note 2)	C_{OUT}		-	-	12	pF
$\overline{RESET}$, $\overline{IRQ}$, TCAP/TOSC1, OSC1, PA0-7, PB0-3	C_{IN}		-	-	8	pF

NOTES:

1. This device contains circuitry to protect the inputs against damage due to high static voltages of electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to the range $V_{SS} < (V_{IN}$ or $V_{OUT}) < V_{DD}$. Reliability of operation is enhanced if unused inputs except OSC2 are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).
2. Includes Ports used as Input/Output Pins, Ports used as Input only Pins; Ports used as Output only Pins.

DC Electrical Specifications

V_{DD} = 3.3V_{DC} ±10%, V_{SS} = 0V_{DC}, T_A = -40°C to +125°C, Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	V_{OL}	I_{LOAD} <10µA	-	-	0.1	V
	V_{OH}		V_{DD} -0.1	-	-	V
Output High Voltage: PA0-7, PB0-3, TCMP	V_{OH}	I_{LOAD} = -0.2mA	V_{DD} -0.3	-	-	V
Output Low Voltage: PA0-7, PB0-3, TCMP	V_{OL}	I_{LOAD} = 0.4mA	-	-	0.3	V
Input High Voltage: PA0-7, PB0-3, OSC1, TCAP/TOSC1	V_{IH}		-	0.5•V_{DD}	0.7•V_{DD}	V
Input High Voltage: $\overline{RESET}$, $\overline{IRQ}$	V_{IH}		-	0.5•V_{DD}	2.5	V
Input Low Voltage: PA0-7, PB0-3, OSC1, TCAP/TOSC1	V_{IL}		0.2•V_{DD}	0.5•V_{DD}	-	V
Input Low Voltage: $\overline{RESET}$, $\overline{IRQ}$	V_{IL}		0.5	0.3•V_{DD}	-	V
Input Hysteresis Voltage: $\overline{RESET}$, $\overline{IRQ}$	V_{HYS}		0.3	0.6	-	V
Data Retention Voltage	V_{RM}	0°C to +70°C	2	-	-	V
Supply Current (Notes 1, 2)						
RUN	I_{RUN}		-	1.2	2.4	mA
WAIT	I_{WAIT}		-	0.5	1.0	mA
STOP	I_{STOP}	T_A = -40°C to +125°C	-	10	20	µA
I/O Ports Hi-Z Leakage Current: PA0-7, PB0-3	I_{IL}		-	-	±10	µA
Input Current: $\overline{RESET}$, $\overline{IRQ}$, TCAP/TOSC1, OSC1	I_{IN}		-	-	±1	µA
Capacitance: (Note 2)	C_{OUT}		-	-	12	pF
$\overline{RESET}$, $\overline{IRQ}$, TCAP/TOSC1, OSC1, PA0-7, PB0-3	C_{IN}		-	-	8	pF

NOTES:

1. This device contains circuitry to protect the inputs against damage due to high static voltages of electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to the range V_{SS} < (V_{IN} or V_{OUT}) < V_{DD}. Reliability of operation is enhanced if unused inputs except OSC2 are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).
2. Includes Ports used as Input/Output Pins, Ports used as Input only Pins; Ports used as Output only Pins.

Control Timing

V_{DD} = 5V ±10%, V_{SS} = 0V, T_A = -40°C to +125°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Of Operation						
Crystal Option	f_{OSC}		-	-	4.2	MHz
External Clock Option	f_{OSC}		DC	-	4.2	MHz
Internal Operating Frequency						
Crystal (f_{OSC} + 2)	f_{OP}		-	-	2.1	MHz
External Clock (f_{OSC} + 2)	f_{OP}		DC	-	2.1	MHz
Cycle Time	t_{CYC}		480	-	-	ns
Crystal Oscillator Start-Up Time for AT-Cut Crystal	t_{OXOV}		-	-	100	ms

Control Timing V_{DD} = 5V ±10%, V_{SS} = 0V, T_A = -40°C to +125°C **(Continued)**

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Stop Recovery Start-Up Time (AT-Cut Crystal Oscillator)	t_{ILCH}		-	-	100	ms
$\overline{\text{RESET}}$ Pulse Width	t_{RL}		1.5	-	-	t_{CYC}
Timer						
Resolution (Note 1)	t_{RES}		4.0	-	-	t_{CYC}
Input Capture Pulse Width	t_{TH}, t_{TL}		125	-	-	ns
Input Capture Pulse Period	t_{TLTL}		(Note 2)	-	-	t_{CYC}
Interrupt Pulse Width Low (Edge-Triggered)	t_{ILIH}		125	-	-	ns
Interrupt Pulse Period	t_{ILIH}		(Note 3)	-	-	t_{CYC}
OSC1 Pulse Width	t_{OH}, t_{OL}		90	-	-	ns

NOTES:

1. Since a 2-bit prescaler in the timer must count four internal cycles (t_{CYC}), this is the limiting minimum factor in determining the timer resolution.
2. The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{CYC}.
3. The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{CYC}.

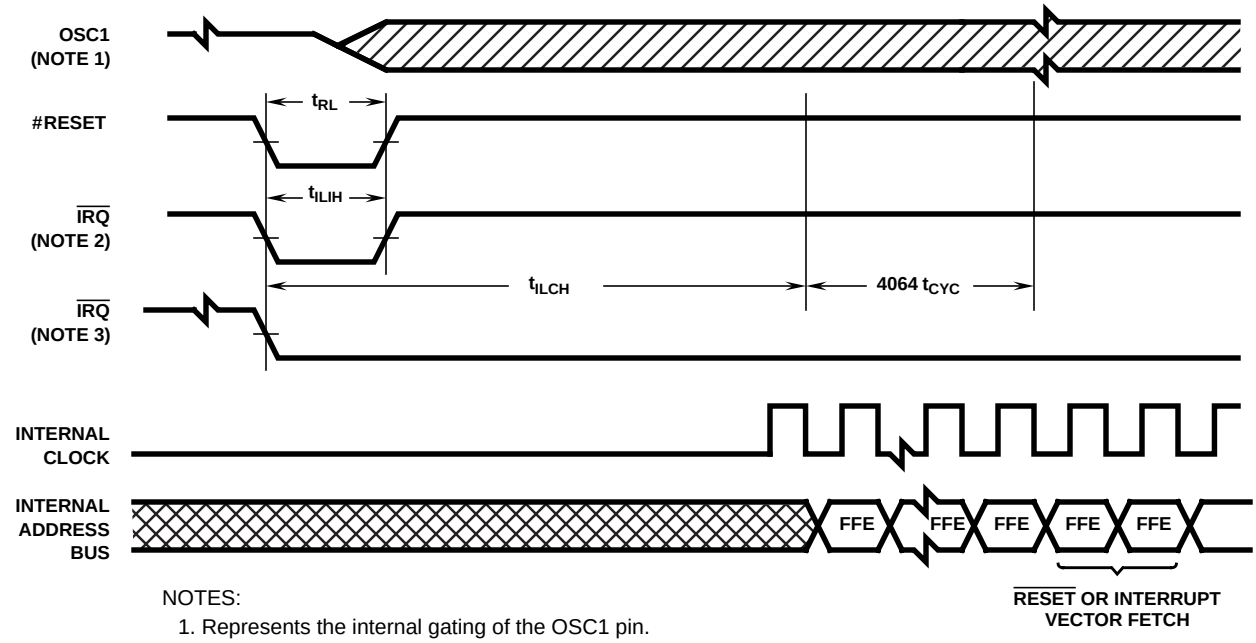
Control Timing V_{DD} = 3.3V ±10%, V_{SS} = 0V, T_A = -40°C to +125°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Of Operation						
Crystal Option	f_{OSC}		-	-	2.0	MHz
External Clock Option	f_{OSC}		DC	-	2.0	MHz
Internal Operating Frequency						
Crystal (f_{OSC} + 2)	f_{OP}		-	-	1.0	MHz
External Clock (f_{OSC} + 2)	f_{OP}		DC	-	1.0	MHz
Cycle Time	t_{CYC}		1000	-	-	ns
Crystal Oscillator Start-up Time for AT-cut Crystal	t_{OXOV}		-	-	100	ms
Stop Recovery Start-up Time (AT-cut Crystal Oscillator)	t_{ILCH}		-	-	100	ms
$\overline{\text{RESET}}$ Pulse Width	t_{RL}		1.5	-	-	t_{CYC}
Timer						
Resolution (Note 1)	t_{RES}		4.0	-	-	t_{CYC}
Input Capture Pulse Width	t_{TH}, t_{TL}		250	-	-	ns
Input Capture Pulse Period	t_{TLTL}		(Note 2)	-	-	t_{CYC}
Interrupt Pulse Width Low (Edge-Triggered)	t_{ILIH}		250	-	-	ns
Interrupt Pulse Period	t_{ILIH}		(Note 3)	-	-	t_{CYC}
OSC1 Pulse Width	t_{OH}, t_{OL}		200	-	-	ns

NOTES:

1. Since a 2-bit prescaler in the timer must count four internal cycles (t_{CYC}), this is the limiting minimum factor in determining the timer resolution.
2. The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{CYC}.
3. The minimum period t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{CYC}.

Control Timing Diagrams



NOTES:

1. Represents the internal gating of the OSC1 pin.
2. $\overline{IRQ}$ pin edge-sensitive mask option.
3. $\overline{IRQ}$ pin level and edge-sensitive mask option.

FIGURE 1. STOP RECOVERY TIMING DIAGRAM

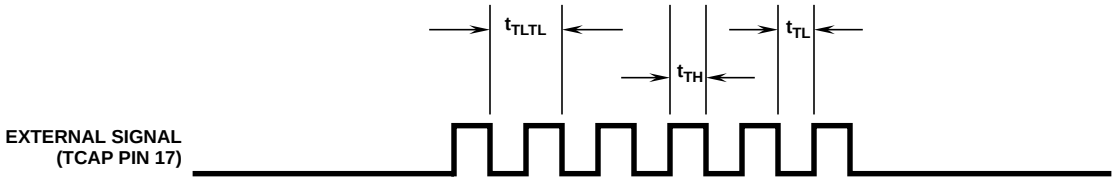


FIGURE 2. TIMER RELATIONSHIPS

Functional Pin Description, Input/Output Programming, Memory, CPU Registers, and Self-Check

This section provides a description of the functional pins, input/output programming, memory, CPU registers, and self-check features of the CDP68HC05J3.

FUNCTIONAL PIN DESCRIPTION

V_{DD} and V_{SS}

Power is supplied to the MCU using these two pins. V_{DD} is a positive voltage with respect to V_{SS} (ground).

$\overline{IRQ}$ (Maskable Interrupt Request)

$\overline{IRQ}$ is a programmable option which provides two different choices of interrupt triggering sensitivity. These options are:

1. negative edge-sensitive triggering only, or
2. both negative edge-sensitive and level-sensitive triggering.

In the latter case, either type of input to the $\overline{IRQ}$ pin will produce an interrupt. The MCU completes the current instruction before it responds to the interrupt request. When the $\overline{IRQ}$ pin goes low for at least one t_{ILIH}, a logic one is latched internally to signify an interrupt has been requested. When the MCU completes its current instruction, the interrupt latch is tested. If the interrupt latch contains a logic one, and the interrupt mask bit (I bit) in the condition code register is clear, the MCU then begins the interrupt sequence.

If the option is selected to include level-sensitive triggering, then the $\overline{IRQ}$ input can be connected to V_{DD} via an external resistor to permit "wire ORed" operation. See **INTERRUPTS** for more detail concerning $\overline{IRQ}$ interrupts.

$\overline{RESET}$

The $\overline{RESET}$ input is not required for start-up but can be used to reset the MCU internal state and provide an orderly software start-up procedure. Refer to **RESETS** for a detailed description.

TCAP/TOSCIN

The TCAP input controls the input capture feature for the on-chip programmable timer system. Refer to **Input Capture Register** for additional information. If bit 3 of the Oscillator Control Register (OCR) is set, then TOSCIN is used as the clock source for the internal timer. If bit 4 of the OCR is set then TOSCIN together with TOSCOUT can be used to create a crystal oscillator.

TCMP/TOSCOUT

The TCMP pin provides an output for the output compare feature of the on-chip timer system. Refer to **Output Compare Register** for additional information. If bit 4 of the Oscillator Control Register (OCR) is set, then TOSCOUT is used together with TOSCIN to create a crystal oscillator circuit.

OSCIN, OSCOUT

The CDP68HC05J3 family of MCUs can be configured, during device manufacturing, to accept either a crystal or an RC network to control the internal oscillator. The internal clocks are derived by a divide-by-two of the external oscillator frequency (f_{OSC}).

Crystal

The circuit shown in Figure 3C is recommended when using a crystal. The internal oscillator is designed to interface with an AT-Cut parallel resonant quartz crystal resonator in the frequency range specified for f_{OSC} in Control Timing. Use of an external CMOS oscillator is recommended when crystals outside the specified ranges are to be used. The crystal and components should be mounted as close as possible to the input pins to minimize output distortion and start-up stabilization time. Refer to **ELECTRICAL SPECIFICATIONS** for V_{DD} specifications.

	2MHz	4MHz	UNITS
R_S (Max)	400	75	Ω
C_0	5	7	pF
C_1	0.008	0.012	pF
C_{OSC1}	15-40	15-30	pF
C_{OSC2}	15-30	15-25	pF
R_P	10	10	MΩ
Q	30	40	K

FIGURE 3A. CRYSTAL RESONATOR PARAMETERS

Ceramic Resonator

A ceramic resonator may be used in place of the crystal in cost sensitive applications. The circuit in Figure 3C is recommended when using a ceramic resonator. Figure 3B lists the recommended capacitance and feedback resistance values. The manufacturer of the particular ceramic resonator being considered should be consulted for specific information.

	2MHz - 4MHz	UNITS
R_S (Typical)	10	Ω
C_0	40	pF
C_1	4.3	pF
C_{OSC1}	30	pF
C_{OSC2}	30	pF
R_P	1-10	MΩ
Q	1250	-

FIGURE 3B. CRYSTAL RESONATOR PARAMETERS

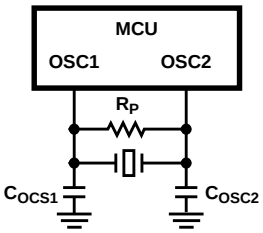


FIGURE 3C. CRYSTAL OSCILLATOR CONNECTIONS

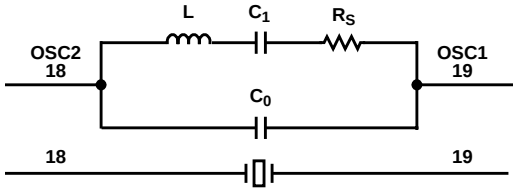


FIGURE 3D. EQUIVALENT CRYSTAL CIRCUIT

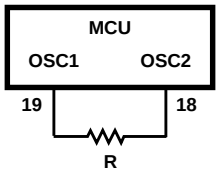


FIGURE 3E. RC OSCILLATOR CONNECTIONS

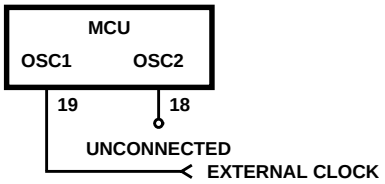


FIGURE 3F. EXTERNAL CLOCK SOURCE CONNECTIONS

FIGURE 3. OSCILLATOR CONNECTIONS

RC

If the RC oscillator option is selected, then a resistor is connected to the oscillator pins as shown in Figure 3E.

External Clock

An external clock should be applied to the OSCIN input with the OSCOUT output not connected, as shown in Figure 3F. An external clock may be used with either the RC or crystal oscillator option. The t_{OXOV} or t_{ILCH} specifications do not apply when using an external clock input. The equivalent specification of the external clock source should be used in lieu of t_{OXOV} or t_{ILCH}.

PA0-PA7

These eight I/O lines comprise port A. The function of any pin is software programmable to be an input, an output, or an open drain output. All port A lines are configured as inputs during power-on or reset. Refer to Input/Output Programming for a detailed description of I/O programming.

PB0-PB3

These four lines comprise port B. The function of any pin is software programmable to be an input or an output. Additionally, each pin can be individually programmed to generate an interrupt when the pin is low. All port B lines are configured as inputs during power-on or reset. Refer to Input/Output Programming for a detailed description of I/O programming.

INPUT/OUTPUT PROGRAMMING

Parallel Ports

The 12 I/O lines associated with Ports A and B may be individually programmed as an input or an output. The direction of each pin is determined by the state of the corresponding bit in the port data direction register (DDR). A port pin is configured as an output if its corresponding DDR bit is set to a logic one. A pin is configured as an input if its corresponding DDR bit is cleared to a logic zero. At power-on or RESET, all DDRs are cleared, which configures all port A and B pins as inputs. The data direction registers are capable of being written to or read by the processor. Refer to Figure 4, Figure 5 and Table 1. During the programmed output state, a read of the data register actually reads the value of the output latch and not the I/O pin. As an example, if a port bit is set to be a high output and it is pulled low by an external load, reading the port will provide a high reading for that bit.

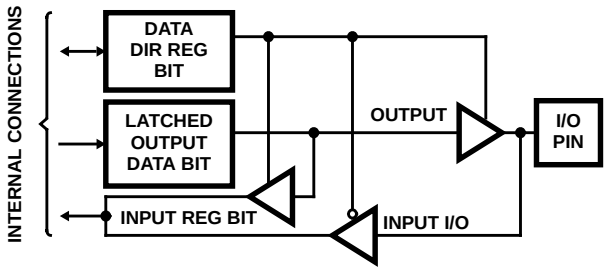


FIGURE 4A.

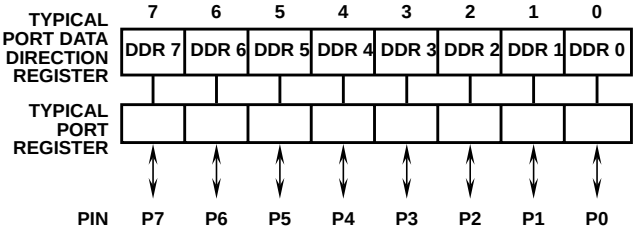
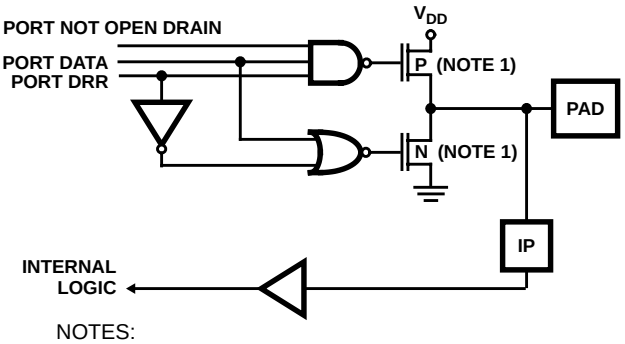


FIGURE 4B.



NOTES:
1. Denotes devices have same physical size, and are enhancement type.
2. IP = Input Protection.
3. Latch-up protection not shown.

FIGURE 4C.

FIGURE 4. TYPICAL PARALLEL I/O CIRCUITRY

TABLE 1. PORT A TRUTH TABLE

(NOTE 1) R/$\overline{W}$	DDR	I/O PIN FUNCTION
0	0	The I/O pin is in input mode. Data is written into the output data latch
0	1	Data is written into the output data latch and output to the I/O pin.
1	0	The state of the I/O pin is read.
1	1	The I/O pin is in output mode. The output data latch is read.

NOTE:

1. R/$\overline{W}$ is an internal signal.

Port A0-A7

The Port A Data Register (DR) is located at $000 and the Port A Data Direction Register (DDR) is located at $002. In addition to data direction control provided by the Port A DDR, Port A I/O pins can be individually configured as open-drain N-FETs. Setting a bit in the Port A Open Drain Register (ODR, location $004), configures the corresponding Port A output pin as an open drain, if the pin is set as an output in the Port A DDR. Setting a bit in the Port A ODR has no effect on pins that are programmed as inputs in the DDR, unless the pin is subsequently programmed as an output. A pin that is open drain will be high impedance when the Port A DR bit is high and it will be active low when the Port A DR bit is low.

All bits in the Port A DDR and ODR are cleared by power-on and RESET. Bits in the Port A DR are unaffected by power-on and RESET.

Port B0-B3

The Port B Data Register (DR) is located at $001 and the Port B Data Direction Register (DDR) is located at $003. In addition to data direction control provided by the Port B DDR, Port B I/O pins can be individually configured as low level sensitive interrupt inputs. Associated with each of the four pins of Port B is a bit in the Port B Interrupt Enable Register (IER, location $005) and the Port B Interrupt Flag Register (IFR, location $006).

Whenever a Port B pin is brought low (either pulled low by an external source, when the pin is programmed as an input, or set low in the Port B DR, when the pin is programmed as an output) the associated flag in the Port B IFR will be set. Even when the pin returns to a high level the IFR bit will remain set. The IFR bits can only be cleared by RESET or by explicitly writing a 0 to the bit in the IFR.

When interrupts are not enabled the IFR can be used to “capture” low going pulses on the Port B pins for later processing. Since even a narrow low pulse will set the IFR bit, the user can be assured not to miss a low event if the IFR is examined. Once the Port B DR bit returns high, the IFR bit should be cleared to “rearm” the IFR to capture the next pulse.

If a bit in the IFR is set, a Port B interrupt will be generated if the associated bit in the Port B IER is set and the CPU has enabled interrupts by clearing the I mask bit. See **INTERRUPTS** for more information. Generally the user will want to clear the appropriate IFR bit(s) before setting the Port B IER bit(s). This will insure only future events will trigger interrupts and not a past event which was “captured” by the IFR.

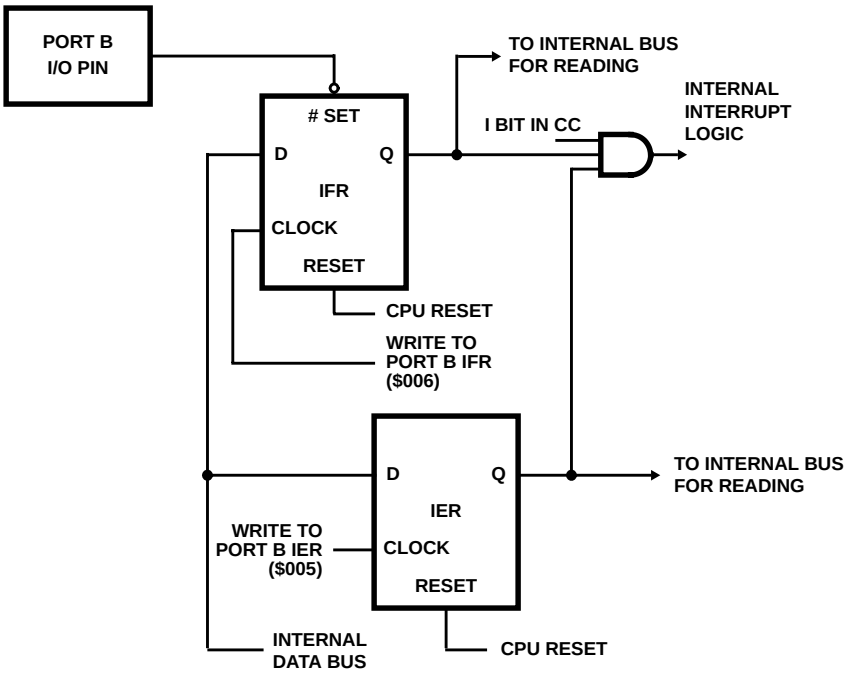


FIGURE 5. PORT B INTERRUPT LOGIC FUNCTIONAL DIAGRAM

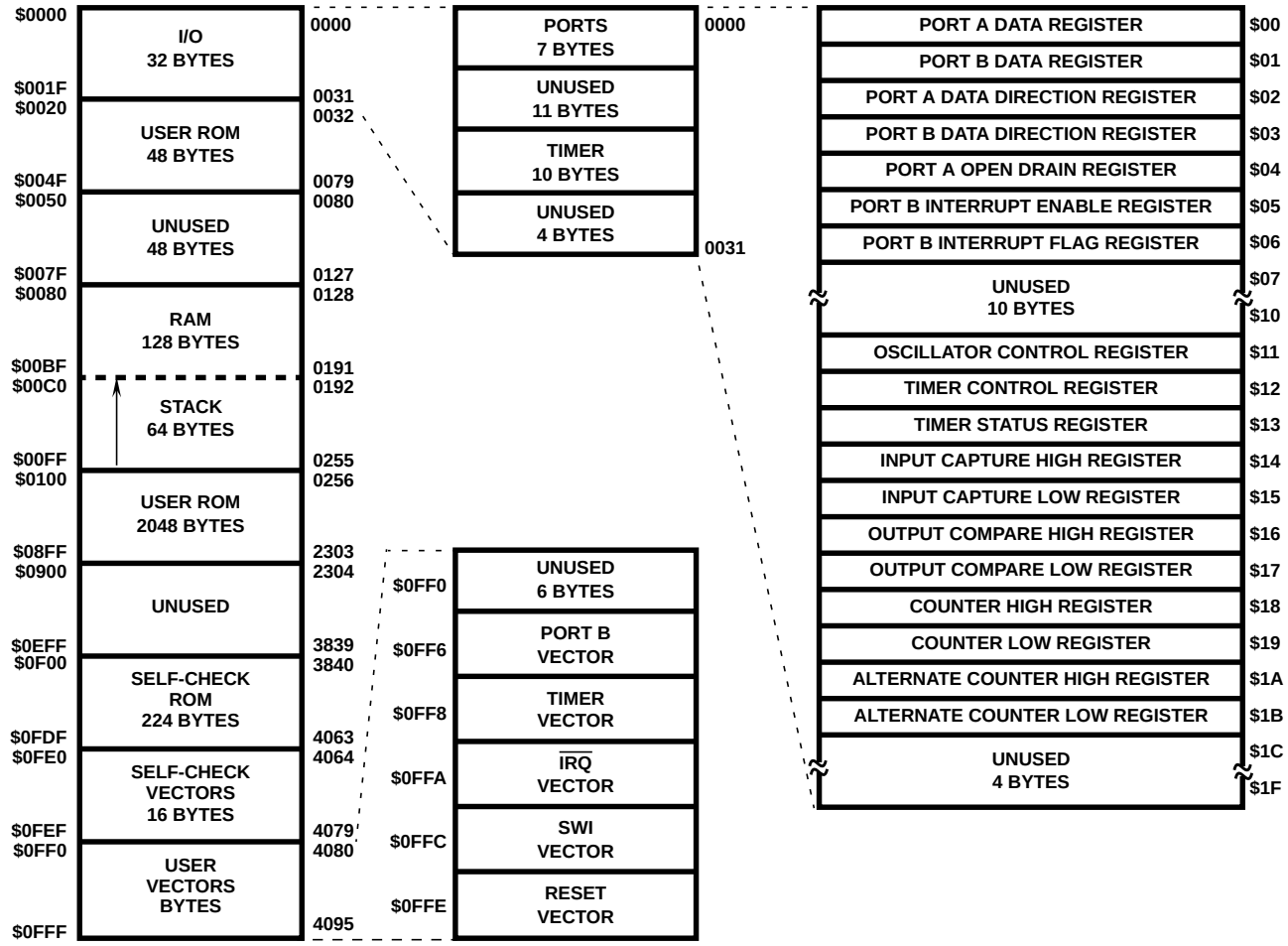


FIGURE 6. ADDRESS MAP

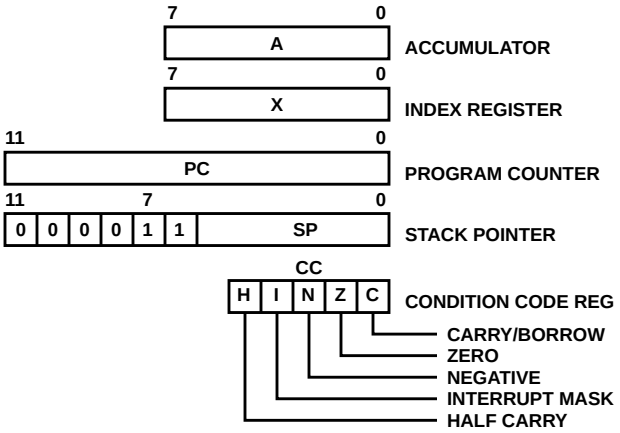


FIGURE 7. PROGRAMMING MODEL

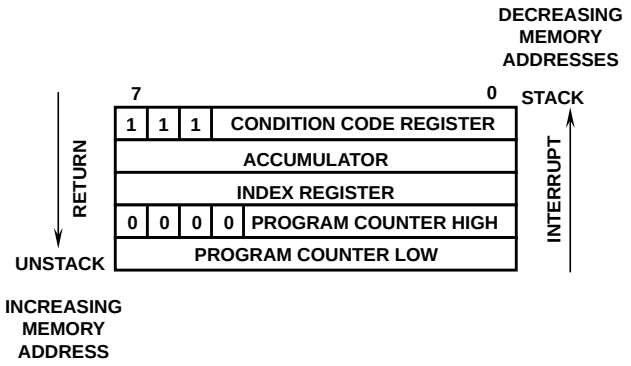


FIGURE 8. STACKING ORDER

A Port B interrupt can be cleared by clearing the enable bit in the IER or by resetting the corresponding bit in the IFR low. In the first case, since the IFR has not been cleared, setting the IER bit high, at any future time, will cause a Port B interrupt, unless the IFR bit is first cleared. In the second case, if the source of the interrupt is still exerting a low on the Port B pin, a new interrupt will immediately be forced, unless the IER bit was also cleared, prior to the IFR bit.

All bits in the Port B IFR, IER, and DDR are cleared by power-up and RESET. The Port B DR is unaffected by power-up and RESET. All unused bits in the Port B registers are read as 0's.

MEMORY

Figure 6 illustrates the address map of the J3. As shown the memory consists of 128 bytes of RAM between $080 and $0FF. The upper 64 bytes of RAM is used for a system stack which grows from higher addresses towards lower addresses. Locations $100 through $900 contain 2048 bytes of ROM for user code. A 240 byte “SelfCheck” routine is located from $F00 through $FF0 (see Selfcheck).

CPU REGISTER MODEL

The CPU contains five registers, as shown in the programing model of Figure 7. The interrupt stacking order is shown in Figure 8.

NOTE: Since the Stack Pointer decrements during pushes, the PCL is stacked first, followed by PCH, etc. Pulling from the stack is in the reverse order.

Accumulator (A)

The accumulator is an 8-bit general purpose register used to hold operands, results of the arithmetic calculations, and data manipulations.

Index Register (X)

The X register is an 8-bit register which is used during the indexed modes of addressing. It provides an 8-bit value which is used to create an effective address. The index register is also used for data manipulations with the read-modify-write type of instructions and as a temporary storage register when not performing addressing operations.

Program Counter (PC)

The program counter is a 12-bit register that contains the address of the next instruction to be executed by the processor.

Stack Pointer (SP)

The stack pointer is a 12-bit register containing the address of the next free location on the pushdown/popup stack. When accessing memory, the most significant bits are permanently configured to 000011. These bits are appended to the six least significant register bits to produce an address within the range of $0FF to $0C0. The stack area of RAM is used to store the return address on subroutine calls and the machine state during interrupts. During external or power-on reset, and during a reset stack pointer (RSP) instruction, the stack pointer is set to its upper limit ($0FF). Nested interrupt and/or subroutines may use up to 64 (decimal) locations. When the 64 locations are exceeded, the stack pointer wraps around and points to its upper limit ($0FF), thus, overwriting the previously stored information. A subroutine call occupies two RAM bytes on the stack, while an interrupt uses five RAM bytes.

Condition Code Register (CC)

The condition code register is a 5-bit register which indicates the results of the instruction just executed as well as the state of the processor. These bits can be individually tested by a program and specified action taken as a result of their state. Each bit is explained in the following paragraphs.

Half Carry Bit (H)

The H bit is set to a one when a carry occurs between bits 3 and 4 of the ALU during an ADD or ADC instruction. The H bit is useful in binary coded decimal subroutines.

Interrupt Mask Bit (I)

When the I bit is set, all interrupts are disabled. Clearing this bit enables the interrupts. If an external interrupt occurs while the I bit is set, the interrupt is latched and processed after the I bit is next cleared; therefore, no interrupts are lost because of the I bit being set. An internal interrupt can be lost if it is cleared while the I bit is set (refer to **Programmable Timer Section** for more information).

Negative (N)

When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation is negative (bit 7 in the result is a logic one).

Zero (Z)

When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation is zero.

Carry/Borrow (C)

Indicates that a carry or borrow out of the arithmetic logic unit (ALU) occurred during the last arithmetic operation. This bit is also affected during bit test and branch instructions, shifts, and rotates.

SELFCHECK

The selfcheck capability of the CDP68HC05J3 MCU provides an internal check to determine if the device is functional. Selfcheck is performed using the circuit shown in the schematic diagram of Figure 9. As shown in the diagram, Port A pins PA0-PA3 are connected to light emitting diodes which display the result of the test. The selfcheck mode is entered by applying a $9V_{DC}$ input (through a 4.7kΩ resistor) to the $\overline{IRQ}$ pin (2) and a $5V_{DC}$ input (through a 4.7kΩ resistor) to the TCAP pin (17) and then depressing the reset switch to execute a reset. After reset, the PA0 pin is first tested for a logic 1 (supplied by the LED) then the following seven tests are performed automatically:

I/O Test

Functionally exercises ports A and B.

RAM Test

Tests each RAM byte by incrementing from $00 to $FF then incrementing twice more to $01. The value in the RAM location is tested after each increment.

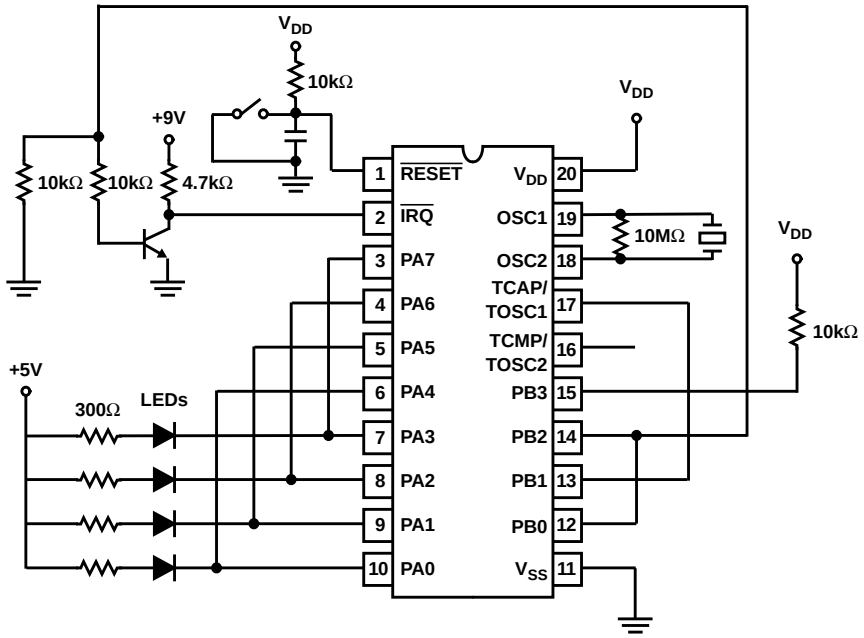
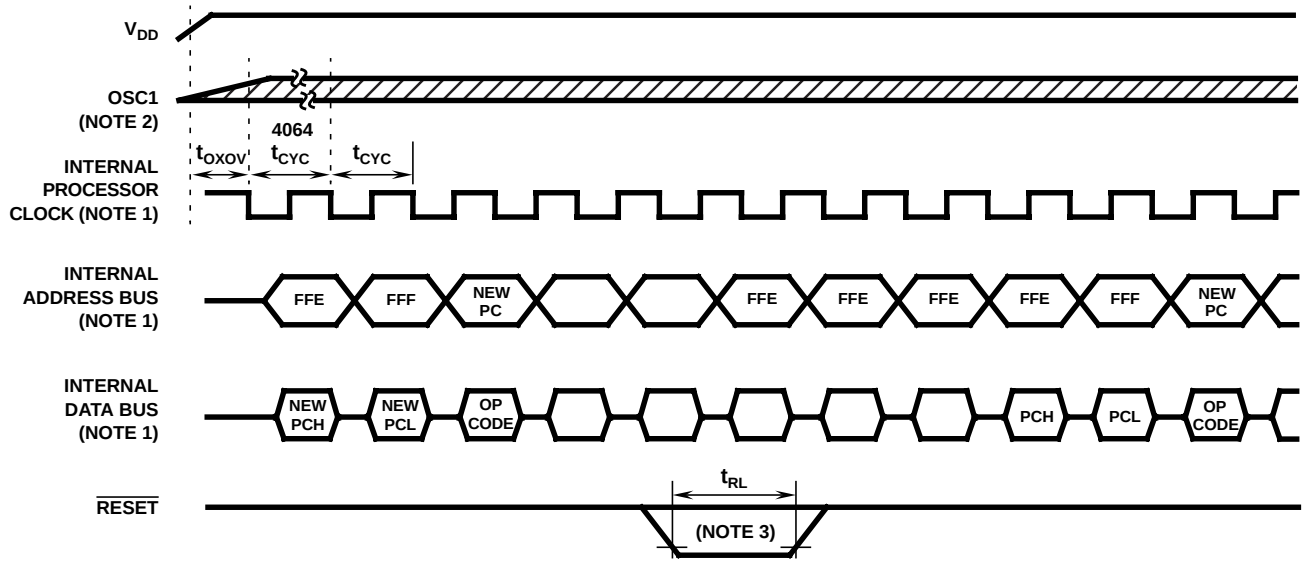


FIGURE 9. SELFCHECK CIRCUIT SCHEMATIC DIAGRAM



NOTES:

1. Internal timing signal and bus information is not available externally.
2. OSC1 line is not meant to represent frequency. It is only meant to represent time.
3. The next rising edge of the internal processor clock following the rising edge of $\overline{\text{RESET}}$ initiates the reset sequence.

FIGURE 10. POWER-ON RESET AND $\overline{\text{RESET}}$

Port B Interrupt Tests

Tests for proper operation of interrupts on each of the four, Port B inputs.

Timer Test

Verifies counter register is properly advancing and checks OCF flags.

External Timer Clock Test

Verifies proper counting via the external oscillator pin (17).

ROM Test

Exclusive OR of all ROM locations with odd one's parity result.

Interrupts Test

Tests SWI, external, timer, and Port B interrupts.

Selfcheck results (using the LEDs as monitors) are shown in Table 2. The following subroutines are available to user programs and do not require any external hardware.

TABLE 2. SELFCHECK RESULTS

PA3	PA2	PA1	PA0	REMARKS
1	0	1	0	Failed RAM Test
1	0	1	1	Failed Port B Interrupt Tests
1	1	0	0	Failed 16-bit Timer Tests
1	1	0	1	Bad External Timer Oscillator
1	1	1	0	Failed ROM Checksum Test
1	1	1	1	Failed Interrupt Tests
Flashing				Good Device
All Others				Bad port A or B or Unknown Failure

0 Indicates LED is On; 1 Indicates LED is Off

Timer Test Subroutine

This subroutine returns with the Z bit cleared if any error is detected; otherwise, the Z bit is set. This subroutine is called at location $FBC. The output compare register is first set to the current timer state. Because the timer is free running and has only a divide-by-four prescaler, each timer count cannot be tested. The test tracks the counter until the timer wraps around, triggering the output compare flag in the timer status register. RAM locations $080 and $081 are overwritten. Upon return to the user's program, X = 40. If the test passed, A = 0 and Z = 1.

Rom Checksum Test Subroutine

This subroutine returns with the Z bit cleared if any error is detected; otherwise, the Z bit is set. This subroutine is called at location $F86 with RAM location $083 equal to $01 and A = 0. A short routine is set up and executed in RAM to compute a checksum of the entire ROM pattern. Upon return to the user's program, X = 0. If the test passed, A = 0 and Z = 1. RAM locations $080 through $083 are overwritten.

Resets, Interrupts, and Low Power Modes

RESETS

The MCU has two reset modes: an active low external reset pin ($\overline{\text{RESET}}$) and a power-on reset function; refer to Figure 10.

RESET Pin

The $\overline{\text{RESET}}$ input pin is used to reset the MCU to provide an orderly software start-up procedure. When using the external reset mode, the $\overline{\text{RESET}}$ pin must stay low for a minimum of one and one half t_{CYC}. The $\overline{\text{RESET}}$ pin contains an internal Schmitt Trigger as part of its input to improve noise immunity.

Power-On Reset

The power-on reset occurs when a positive transition is detected on V_{DD}. The power-on reset is used strictly for power turn-on conditions and should not be used to detect any drops in the power supply voltage. There is no provision for a power-down reset.

If the crystal oscillator option is chosen, the power-on circuitry provides for a 4064 t_{CYC} delay from the time that the oscillator becomes active. If the external $\overline{\text{RESET}}$ pin is low at the end of the 4064 t_{CYC} time out, the processor remains in the reset condition until $\overline{\text{RESET}}$ goes high.

If the RC oscillator option is chosen, the power-on circuitry provides a 2 t_{CYC} delay from the time that the oscillator becomes active. If the external $\overline{\text{RESET}}$ pin is low at the end of the 2 t_{CYC} time out, the processor remains in the reset condition until $\overline{\text{RESET}}$ goes high. Table 3 shows the actions of the two resets on internal circuits, but not necessarily in order of occurrence (X indicates that the condition occurs for the particular reset).

INTERRUPTS

Systems often require that normal processing be interrupted so that some external event may be serviced. The CDP68HC05J3 may be interrupted by one of four different methods: either one of three maskable hardware interrupts (IRQ, Port B, or Timer) and one non-maskable software interrupt (SWI). Interrupts such as Timer and Port B have several flag and status bits which control the interrupt. Generally, interrupt flags are located in read-only status register, whereas their equivalent enable bits are located in associated control registers. The interrupt flags and enable bits are never contained in the same register. If the enable bit is a logic zero it blocks the interrupt from occurring but does not inhibit the flag from being set. Reset clears all enable bits to preclude interrupts during the reset procedure.

Generally, interrupt flags are located in read-only status register, whereas their equivalent enable bits are located in associated control registers. The interrupt flags and enable bits are never contained in the same register. If the enable bit is a logic zero it blocks the interrupt from occurring but does not inhibit the flag from being set. Reset clears all enable bits to preclude interrupts during the reset procedure.

The general sequence for clearing an interrupt is a software sequence of first accessing the status register while the interrupt flag is set, followed by a read or write of an associ-

ated register. When any of these interrupts occur, and if the enable bit is a logic 1, normal processing is suspended at the end of the current instruction execution. Interrupts cause the processor registers to be saved on the stack (see Figure 8) and the interrupt mask (I bit) set to prevent additional interrupts. The appropriate interrupt vector then points to the starting address of the interrupt service routine (refer to Figure 6for vector location). Upon completion of the interrupt service routine, the RTI instruction (which is normally a part of the service routine) causes the register contents to be recovered from the stack followed by a return to normal processing. The stack order is shown in Figure 8.

A discussion of interrupts, plus a table listing vector addresses for all interrupts, including RESET, of the MCU is provided in Table 4.

Hardware Controlled Interrupt Sequence

The following three functions (RESET, STOP, and WAIT) are not in the strictest sense an interrupt; however, they are acted upon in a similar manner. Flowcharts for hardware interrupts are shown in Figure 11, and for STOP and WAIT are provided in Figure 12. A discussion is provided below.

(a) RESET - A low input on the $\overline{\text{RESET}}$ input pin causes the program to vector to its starting address which is specified by the contents of memory locations $FFE and $FFF. The I bit in the condition code register is also set. Much of the MCU is configured to a known state during this type of reset as previously described in RESETS paragraph.

(b) STOP - The STOP instruction causes the oscillator to be turned off and the processor to “sleep” until an external interrupt (IRQ or Port B interrupt) or a RESET or a TIMER interrupt occurs. Note that TIMER interrupts can only be generated if the external clock for the TIMER is enabled.

(c) WAIT - The WAIT instruction causes all processor clocks to stop, but leaves the Timer running. This “rest” state of the processor can be cleared by RESET, an external interrupt (IRQ), Timer interrupt, or Port B interrupt.

TABLE 3. RESET ACTION ON INTERNAL CIRCUIT

CONDITION	$\overline{\text{RESET}}$ PIN	POWER-ON RESET
Oscillator Start-Up Delay Set to 4064 t_{CYC} (8128 Oscillator Cycles)	Note 1	X
Timer Prescaler Reset to Zero State	X	X
Timer Counter Configured to $FFFC	X	X
Timer Output Compare (TCMP) Bit Reset to Zero	X	X
All Timer Interrupt Enable Bits Cleared (ICIE, OCIE, and TOIE) to Disable Timer Interrupts	X	X
Timer OLVL Bit is Cleared to Zero	X	X
All Oscillator Control Register Bits (EC, EOE, and NDEL) Cleared to Zero	X	X
Both Port A and Port B Data Direction Registers Cleared to Zero Configuring All Port Pins as Inputs	X	X
Port A Open Drain Register Cleared to Zero	X	X
All Port B Interrupt Enable Register Bits Cleared to Zero to Disable Interrupts	X	X
All Port B Interrupt Flag Register Bits Cleared (If a Pin is Low it’s Bit Will Immediately Be Set)	X	X
Configure Stack Pointer to $0FF	X	X
Force Internal Address to the RESET Vector ($FFE)	X	X
Set Bit in Condition Code Register to a Logic One to Disable All Interrupts Except SWI	X	X
Clear External Interrupt Latch	X	X
Clear WAIT Latch	X	X
Clear Stop Latch	X (Note 2)	X

NOTES:

1. A delay of 2 t_{CYC} (4 oscillator cycles) is introduced when restarting with RESET, except from STOP mode.
2. 4064 t_{CYC} oscillator start-up time-out occurs.

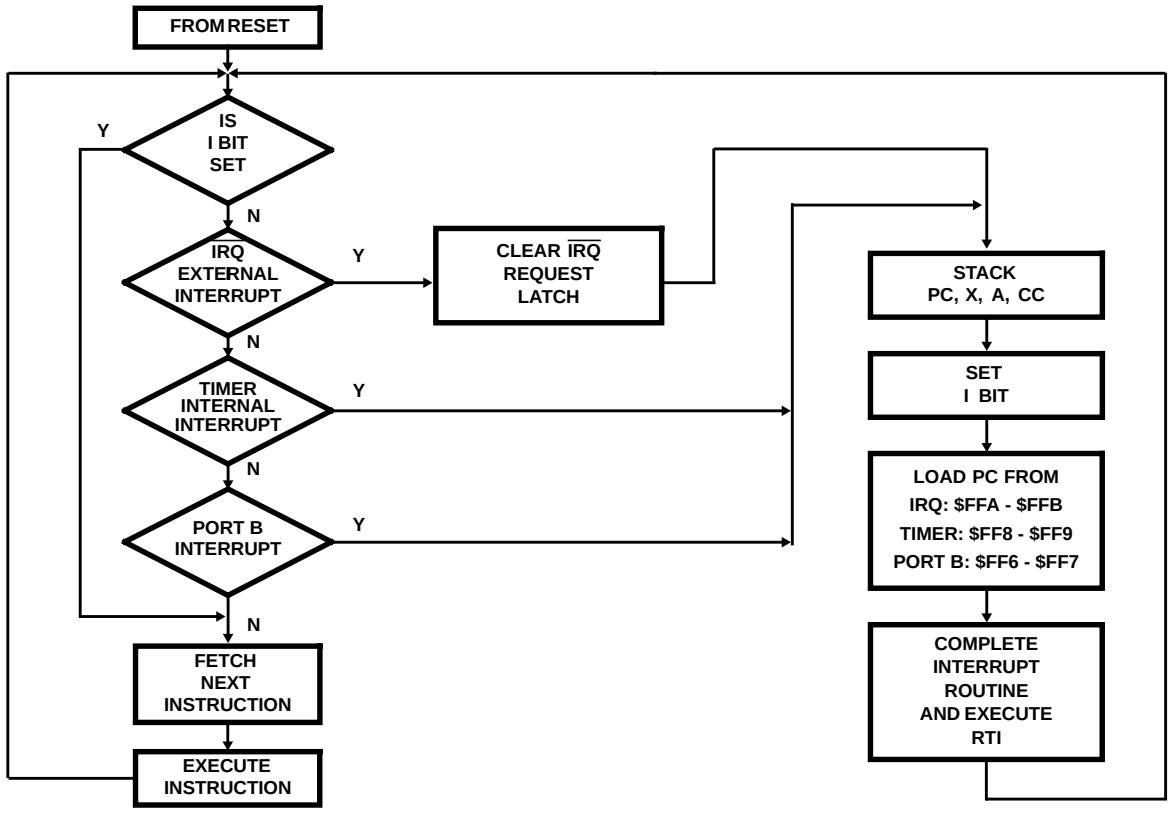


FIGURE 11. HARDWARE INTERRUPT FLOWCHART

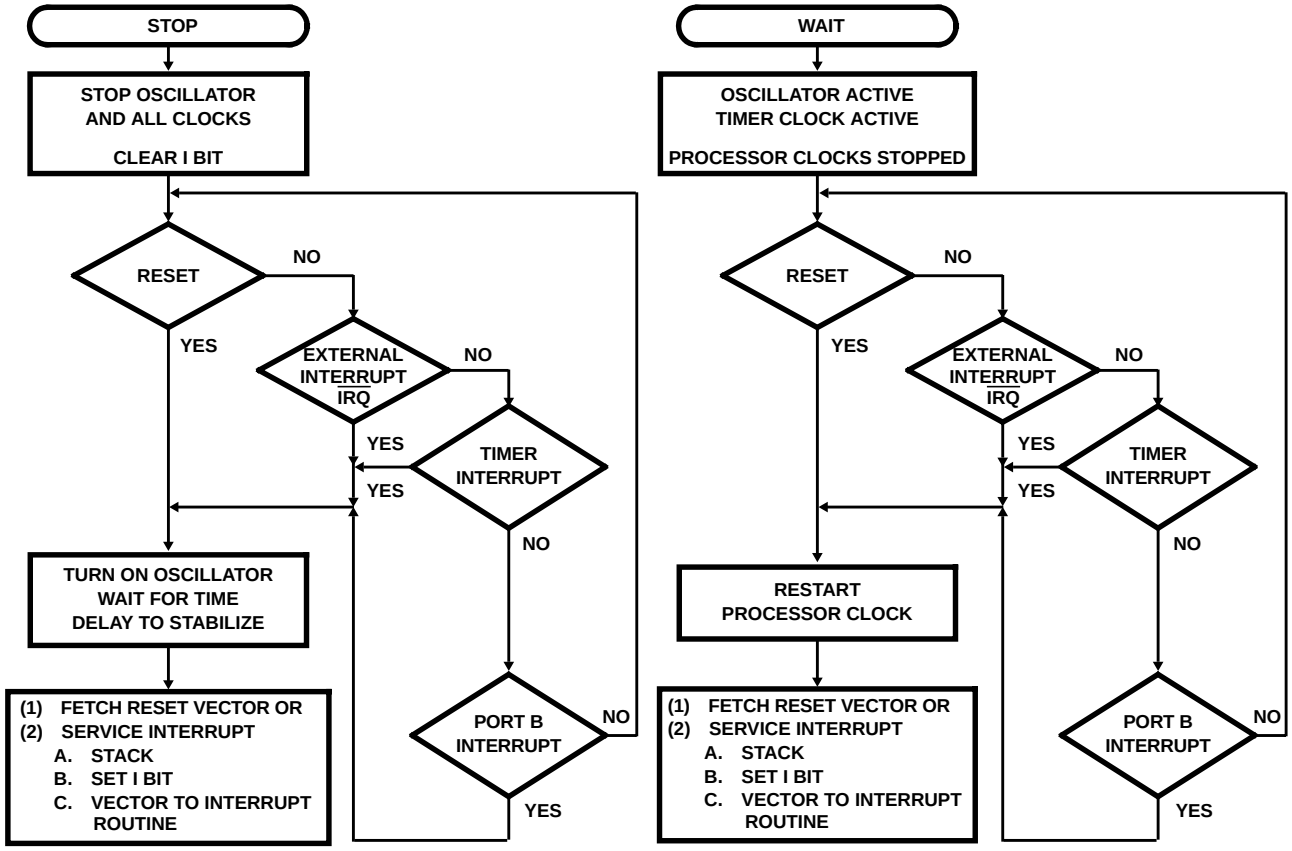


FIGURE 12. STOP/WAIT FLOWCHARTS

TABLE 4. VECTOR ADDRESSES FOR INTERRUPTS AND RESET

REGISTER	FLAG NAME	INTER-RUPTS	CPU INTERRUPT	VECTOR ADDRESS
N/A	N/A	Reset	$\overline{\text{RESET}}$	$FFE-$FFF
N/A	N/A	Software	SWI	$FFC - $FFD
N/A	N/A	External Interrupt	$\overline{\text{IRQ}}$	$FFA - $FFB
Timer Status (TCR)	ICF OCF TOF	Input Capture Output Compare Timer Overflow	TIMER	$FF8 - $FF9
Port B Interrupt Flag Register (IRF)	Bit 0-3	Port B0-3 Interrupt	Port B0-B3	$FF6 - $FF7

There are no special “WAIT” or “STOP” vectors for the interrupts. When the processor is released from the WAIT or STOP state, the same RESET and interrupt vectors are used as at all other times. The processor provides no indication that a WAIT or STOP state has been exited.

Software Interrupt (SWI)

The software interrupt is an executable instruction. The action of the SWI instruction is similar to the hardware interrupts. The SWI is executed regardless of the state of the interrupt mask (I bit) in the condition code register. The interrupt service routine address is specified by the contents of memory location $FFC and $FFD.

External Interrupt

If the interrupt mask (I bit) of the condition code register has been cleared and the external interrupt pin ($\overline{\text{IRQ}}$) has gone low, then the external interrupt is recognized. When the interrupt is recognized, the current state of the CPU is pushed onto the stack and the I bit is set. This masks further interrupts until the present one is serviced. The interrupt service routine address is specified by the contents of memory location $FFA and $FFB. Either a level-sensitive and negative edge-sensitive trigger, or a negative edge sensitive only trigger are available as a mask option. Figure 13 shows both a functional and mode timing diagram for the interrupt line. The timing diagram shows two different treatments of the interrupt line ($\overline{\text{IRQ}}$) to the processor. The first method shows single pulses on the interrupt line spaced far enough apart to be serviced. The minimum time between pulses is a function of the number of cycles required to execute the interrupt service routine plus 21 cycles. Once a pulse occurs, the next pulse should not occur until the MCU software has exited the routine (an RTI occurs). The second configuration shows several interrupt lines “wire-ORed” to form the interrupts at the processor. Thus, if after servicing one interrupt the interrupt line remains low, then the next interrupt is recognized.

NOTE: The internal interrupt latch is cleared in the first part of the service routine; therefore, one (and only one) external interrupt pulse could be latched during t_{ILIL} and serviced as soon as the I bit is cleared.

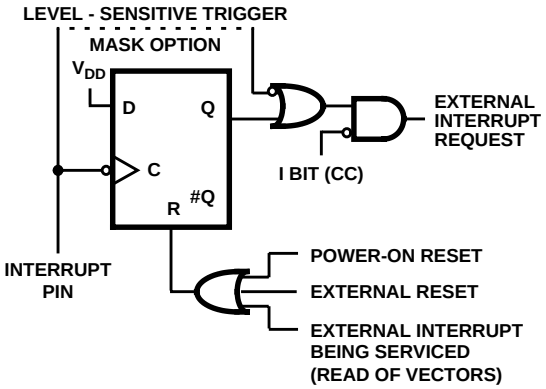
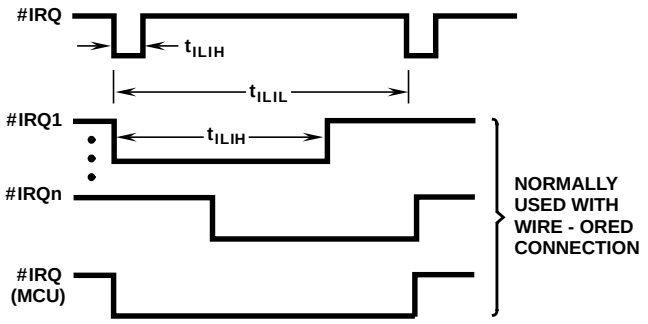


FIGURE 13A. EXTERNAL INTERRUPT FUNCTION DIAGRAM



NOTE:
Edge-Sensitive Trigger Condition - The minimum pulse width (t_{ILIH}) is either 125ns (V_{DD} = 5V) or 250ns (V_{DD} = 3V). The period t_{ILIL} should be less than the number of t_{CYC} cycles it takes to execute the interrupt service routine plus 21 t_{CYC} cycles.

Level-Sensitive Trigger Condition - If after servicing an interrupt the #IRQ remains low, then the next interrupt is recognized.

FIGURE 13B. EXTERNAL INTERRUPT MODE DIAGRAM

FIGURE 13.

Timer Interrupt

There are three different timer interrupt flags that will cause a timer interrupt whenever they are set and enabled. These three interrupt flags are found in the three most significant bits of the timer status register (TSR, location $13) and all three will vector to the same interrupt service routine ($FF8 - $FF9). All interrupt flags have corresponding enable bits (ICE, OCIE, and TOIE) in the timer control register (TCR, location $12). Reset clears all enable bits, thus preventing an interrupt from occurring during the reset time period. The actual processor interrupt is generated only if the I bit in the condition code register is also cleared. When the interrupt is recognized, the current machine state is pushed onto the stack and I bit is set. This masks further interrupts until the present one is serviced.

The interrupt service routine address is specified by the contents of memory locations $FF8 and $FF9. The general sequence for clearing an interrupt is a software sequence of accessing the status register while the flag is set, followed by a read or write of an associated register. Refer to **Programmable Timer** for additional information about the timer circuitry.

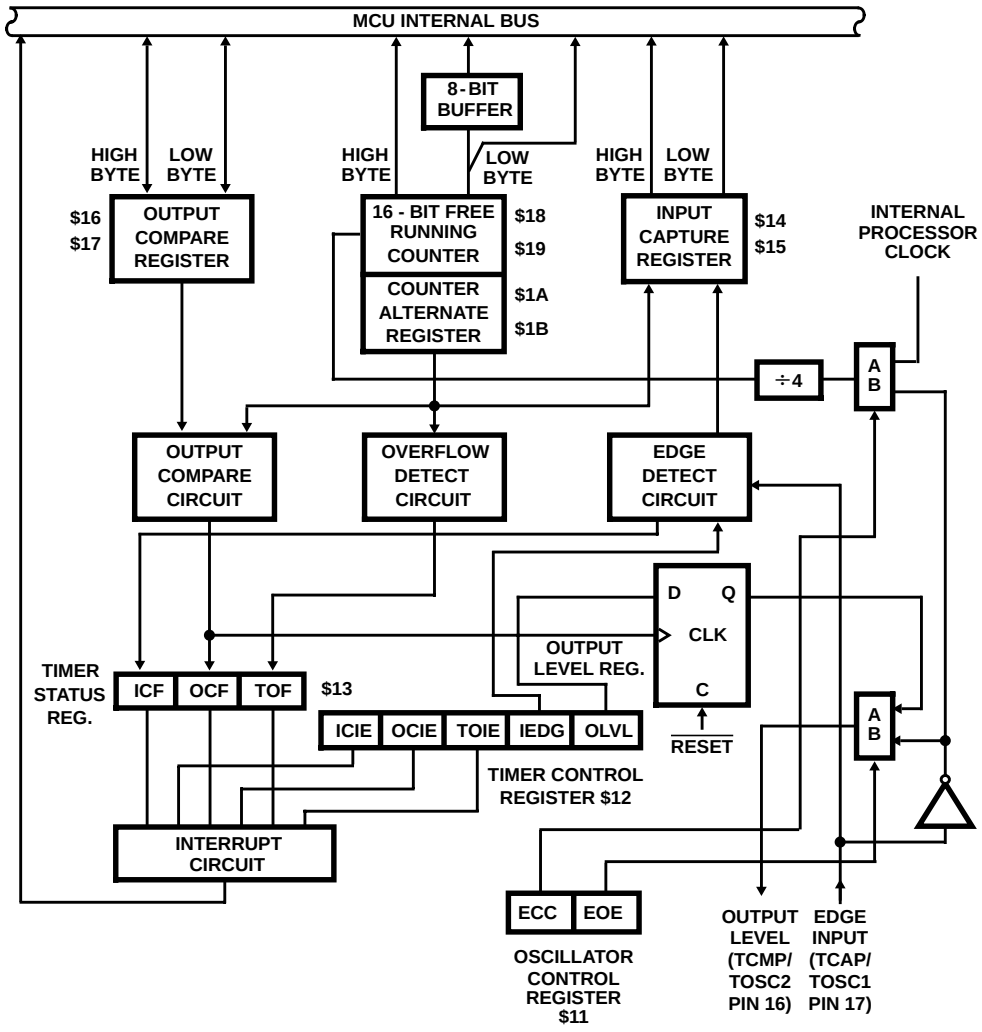
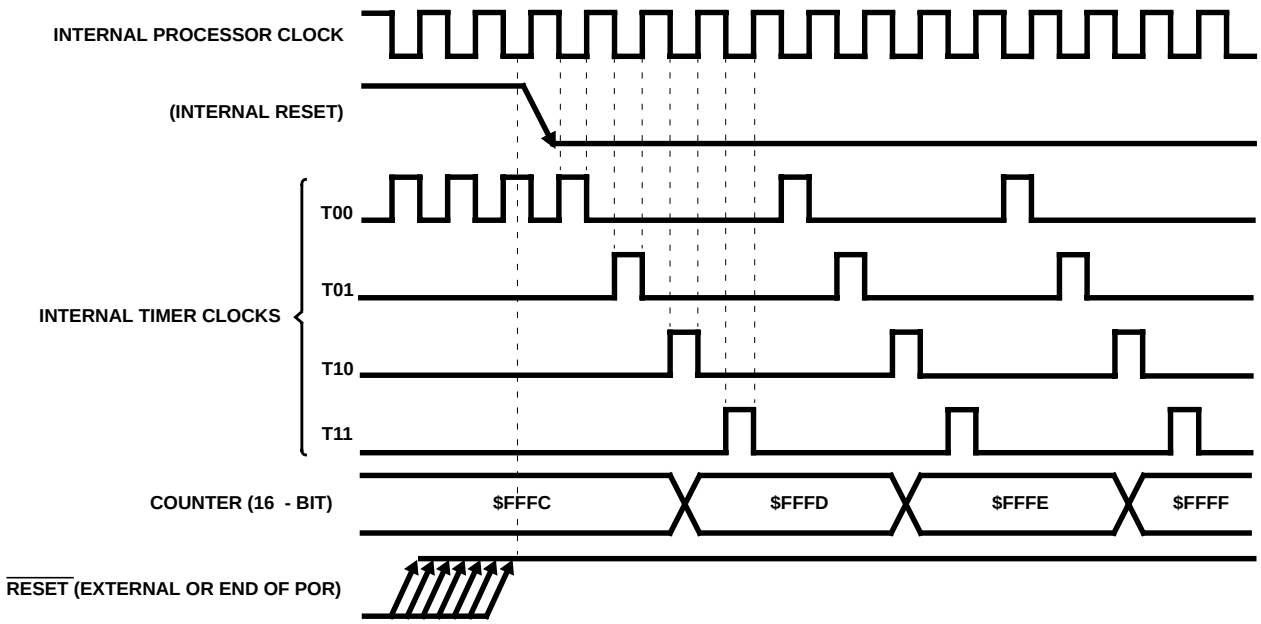


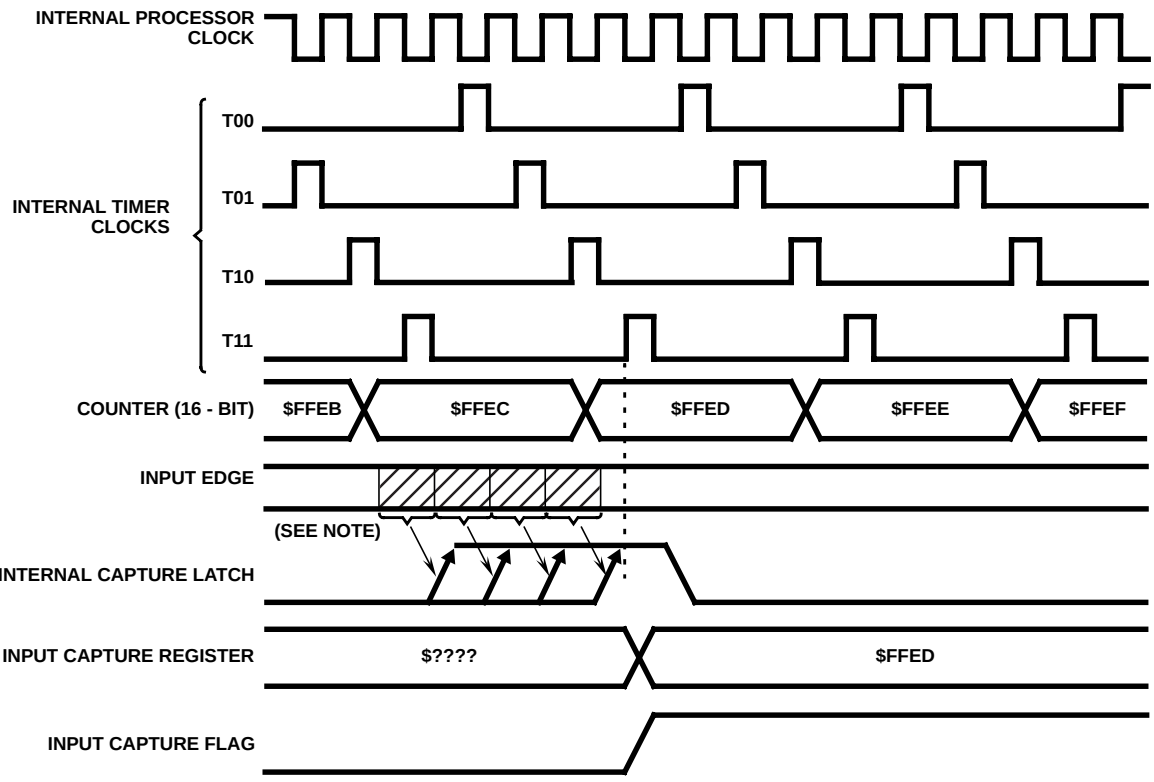
FIGURE 14. PROGRAMMABLE TIMER BLOCK DIAGRAM



NOTE:

1. The Counter Register and the Timer Control Register are the only ones affected by $\overline{\text{RESET}}$.

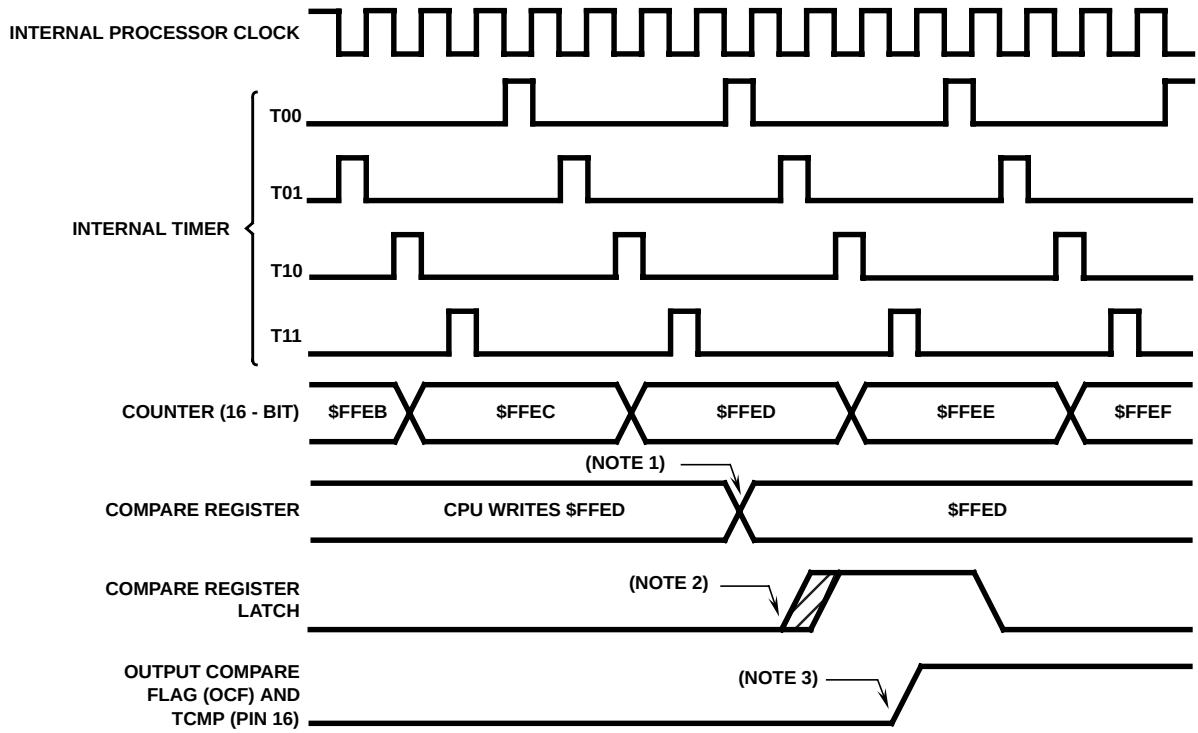
FIGURE 15. TIMER STATE DIAGRAM FOR RESET



NOTE:

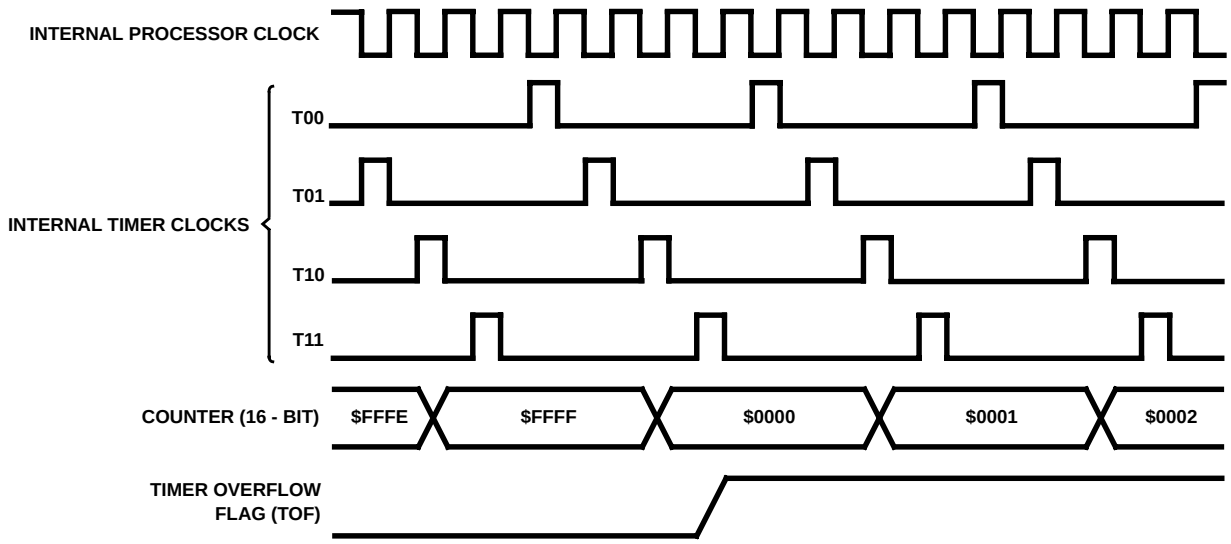
1. If the input edge occurs in the shaded area from one timer state T10 to the other timer state T10 the input capture flag is set during the next state T11.

FIGURE 16. TIMER STATE TIMING DIAGRAM FOR INPUT CAPTURE



NOTES:
1. The CPU write to the Compare Register may take place at any time, but a compare only occurs at timer state T01. Thus a 4 cycle difference may exist between the write to the Compare Register and the actual compare.
2. Internal compare takes place during timer state T01.
3. OCF is set at the timer state T11 which follows the comparison match ($FFED in this example).

FIGURE 17. TIMER STATE TIMING DIAGRAM FOR OUTPUT COMPARE



NOTE:
1. The TOF bit is set at timer state T11 (transition of the counter from $FFFF to $0000). It is cleared by a read of the Timer Status Register during the internal processor clock high time followed by a read of the Counter Low Register.

FIGURE 18. TIMER STATE DIAGRAM FOR TIMER OVERFLOW

Port B Interrupts

The four lines of the Port B can be used as level-sensitive interrupt inputs. The four lines share a common interrupt vector ($FF6-$FF7). To allow identification of the source of the interrupt, the Port B Interrupt Flag Register (IFR) is provided. The flag register contains a bit corresponding to each bit of Port B. The flags are set by applying a low level to the associated Port B pin. The source of the low level can either be external, when the pin is programmed as an input in the Port B DDR, or internal, when the pin is programmed as an output and the bit is set low in the Port B Data Register. The flags can only be cleared by explicitly writing to the IFR or by RESET or power-on. The flags are valid whether Port B interrupts are enabled or not.

Enabling Port B interrupts can be done for individual pins by setting the appropriate bit in the Port B Interrupt Enable Register (IER) high. If a Port B line has been enabled to generate interrupts and the interrupt mask (I bit) is clear, whenever the IFR flag goes high, an interrupt will be generated. The interrupt can be removed by clearing the IER bit or by clearing the IFR bit. After clearing the IFR bit, if the low is still present on the Port B pin, the interrupt will be immediately regenerated since the Port B interrupts are level-sensitive. For more information refer to Figure 5.

Low-Power Modes

STOP Instruction

The STOP instruction places the MCU in its lowest power consumption mode. In the STOP mode the internal oscillator is turned off, causing all internal processing to be halted' refer to Figure 12. During the STOP mode, the I bit in the condition code register is cleared to enable external interrupts (Port B interrupts must be enabled by setting the appropriate bits in the IER prior to entering STOP). All other registers and memory remain unaltered and all input/output lines remain unchanged. This continues until an external interrupt ($\overline{IRQ}$ or Port B) or a RESET is sensed, at which time the internal oscillator is turned on. If the external clock for the TIMER is enabled then TIMER overflow or compare interrupts can also release the CPU from STOP mode. The external interrupt or RESET causes the program counter to load a vector from memory locations $FF6-FF7, $FF8-FF9, $FFA-FFB, or $FFE-FFF which contain the starting address of the interrupt or RESET service routine.

WAIT Instruction

The WAIT instruction places the MCU in a low power consumption mode, but the WAIT mode consumes somewhat more power than the STOP mode. In the WAIT mode, the internal clock remains active, and all CPU processing is stopped; however, the programmable timer system remains active. Refer to Figure 12. During the WAIT mode, the I bit in the condition code register is cleared to enable all interrupts (Port Band Timer interrupts must be enabled by setting the appropriate bits in the IER or TCR prior to entering WAIT). All other registers and memory remain unaltered and all parallel input/output lines remain unchanged. This continues until any interrupt or RESET is sensed. At this time the program counter loads a vector from the memory location ($FF6 through $FFF) which contains the starting address of the interrupt or RESET service routine.

Data Retention Mode

The contents of RAM and CPU registers are retained at supply voltages as low as $2V_{DC}$. This is referred to as the Data Retention mode, where the data is held, but the device is not guaranteed to operate.

Programmable Timer

INTRODUCTION

The programmable timer, which is preceded by a fixed divide-by-four prescaler, can be used for many purposes, including input waveform measurements while simultaneously generating an output waveform. Pulse widths can vary from several microseconds to many seconds. A block diagram of the timer is shown in Figure 14 and timing diagrams are shown in Figures 15 through 18.

Because the timer has a 16-bit architecture, each specific functional segment (capability) is represented by two registers. These registers contain the high and low byte of that functional segment. Generally, accessing the low byte of a specific timer function allows full control of that function; however, an access of the high byte inhibits that specific timer function until the low byte is also accessed.

NOTE: The I bit in the condition code register should be set while manipulating both the high and low byte register of a specific timer function to ensure that an interrupt does not occur. This prevents interrupts from occurring between the time that the high and low byte are accessed.

The programmable timer capabilities are provided by using the following ten addressable 8-bit registers (note the high and low represent the significance of the byte). A description of each register is provided below.

Timer Control Register (TCR) location $12,

Timer Status Register (TSR) location $13,

Input Capture High Register location $14,

Input Capture Low Register location $15,

Output Compare High Register location $16,

Output Compare Low Register location $17,

Counter High Register location $18,

Counter Low Register location $19,

Alternate Counter High Register location $1A, and

Alternate Counter Low Register location $1B.

COUNTER

The key element in the programmable timer is a 16-bit free running counter, or counter register, preceded by a prescaler which divides the internal processor clock by four. The prescaler gives the timer a resolution of 2.0µs if the internal processor clock is 2.0MHz. The counter is clocked to increasing values during the low portion of the internal processor clock. Software can read the counter at any time without affecting its value.

The double byte free running counter can be read from either of two locations $18 - $19 (called counter register at this location), or $1A - $1B (counter alternate register at this location). If a read sequence containing only a read of the least signifi-

cant byte of the free running counter or counter alternate register first addresses the most significant byte ($18, $1A) it causes the least significant byte ($19, $1B) to be transferred to a buffer. This buffer value remains fixed after the first most significant byte “read” even if the user reads the most significant byte several times. This buffer is accessed when reading the free running counter or counter alternate register, if the most significant byte is read, the least significant byte must also be read in order to complete the sequence.

The free running counter is configured to $FFFC during reset and is always a read-only register. During a power-on-reset (POR), the counter is also configured to $FFFC and begins running after the oscillator start-up delay. Because the free running counter is 16 bits preceded by a fixed divide-by-four prescaler, the value in the free running counter repeats every 262,144 MPU internal processor clock cycles. When the counter rolls over from $FFFF to $0000, the timer overflow flag (TOF) bit is set. An interrupt can also be enabled when counter rollover occurs by setting its interrupt enable bit (TOIE).

OUTPUT COMPARE REGISTER

The output compare register is a 16-bit register, which is made up of two 8-bit registers at locations $16 (most significant byte) and $17 (least significant byte). The output compare register can be used for several purposes such as, controlling an output waveform or indicating when a period of time has elapsed. The output compare register is unique in that all bits are readable and writable and are not altered by the timer hardware. Reset does not affect the contents of this register and if the compare function is not utilized, the two bytes of the output compare register can be used as storage locations.

The contents of the output compare register are compared with the contents of the free running counter once during every four internal processor clocks. If a match is found, the corresponding output compare flag (OCF) bit is set and the corresponding output level (OLVL) bit is clocked (by the output compare circuit pulse) to an output level register. The values in the output compare register and the output level bit should be changed after each successful comparison in order to control an output waveform or establish a new elapsed time-out. An interrupt can also accompany a successful output compare provided the corresponding interrupt enable bit, OCIE, is set.

After a processor write cycle to the output compare register containing the most significant byte ($16), the output compare function is inhibited until the least significant byte ($17) is also written. The user must write both byte (locations) if the most significant byte is written first. A write made only to the least significant byte ($17) will not inhibit the compare function. The free running counter is updated every four internal processor clock cycles due to the internal prescaler. The minimum time required to update the output compare register is a function of the software program rather than the internal hardware. A processor write may be made to either byte of the output compare register without affecting the other byte. The output level (OLVL) bit is clocked to the output level register regardless of whether the output compare flag (OCF) is set or clear.

Because neither the output compare flag (OCF bit) nor the output compare register is affected by RESET, care must be exercised when initializing the output compare function with software. The following procedure is recommended:

(1) Write the high byte of the output compare register to inhibit further compares until the low byte is written.

(2) Read the timer status register to arm the OCF if it is already set.

(3) Write the output compare register low byte to enable the output compare function with the flag clear.

The advantage of this procedure is that it prevents the OCF bit from being set between the time it is read and the write to the output compare register. A software example is shown below.

```
B716  STA  OCMPHI;   INHIBIT OUTPUT COMPARE
B613  LDA  TSTAT;    ARM OCF BIT IF SET
BF17  STX  OCMPLO;   READY FOR NEXT COMPARE
```

INPUT CAPTURE REGISTER

The two 8-bit registers which make up the 16-bit input capture register are read-only and are used to latch the value of the free running counter after a defined transition is sensed by the corresponding input capture edge detector. The level transition which triggers the counter transfer is defined by the corresponding input edge bit (IEDG). Reset does not affect the contents of the input capture register.

The result obtained by an input capture will be one more than the value of the free running counter on the rising edge of the internal processor clock preceding the external transition (refer to timing diagram shown in Figure 16). This delay is required for internal synchronization. Resolution is affected by the prescaler allowing the timer to only increment every four internal processor clock cycles.

After a read of the most significant byte of the input capture register ($14), counter transfer is inhibited until the least significant byte ($15) of the input capture register is also read. This characteristic forces the minimum pulse period attainable to be determined by the time used in the capture software routine and its interaction with the main program. The free running counter increments every four internal processor clock cycles due to the prescaler.

A read of the least significant byte ($15) of the input capture register does not inhibit the free running counter transfer. Again, minimum pulse periods are ones which allow software to read the least significant byte ($15) and perform needed operations. There is no conflict between the read of the input capture register and the free running counter transfer since they occur on opposite edges of the internal processor clock.

TIMER CONTROL REGISTER (TCR)

The timer control register (TCR, location $12) is an 8-bit read/write register which contains five control bits. Three of these bits control interrupts associated with each of the three flag bits found in the timer status register (discussed below). The other two bits control: 1) which edge is significant to the capture edge detector (i.e., negative or positive), and 2) the next

value to be clocked to the output level register in response to a successful output compare. The timer control register and the free running counter are the only sections of the timer affected by RESET. The TCMP pin is forced low during external reset and stays low until a valid compare changes it to a high. The timer control register is illustrated below followed by a definition of each bit.

7	6	5	4	3	2	1	0
ICIE	OCIE	TOIE	0	0	0	IEDG	OLVL

TCR (LOCATION $12)

B7, ICIE — If the input capture interrupt enable (ICIE) bit is set, a timer interrupt is enabled when the ICF status flag (in the timer status register) is set. If the ICIE bit is clear, the interrupt is inhibited. The ICIE bit is cleared by RESET.

B6, OCIE — If the output compare interrupt enable (OCIE) bit is set, a timer interrupt is enabled whenever the OCF status flag is set. If the OCIE bit is clear, the interrupt is inhibited. The OCIE bit is cleared by RESET.

B5, TOIE — If the timer overflow interrupt enable (TOIE) bit is set, a timer interrupt is enabled whenever the TOF status flag (in the timer status register) is set. If the TOIE bit is clear, the interrupt is inhibited. The TOIE bit is cleared by RESET.

B1, IEDG — The value of the input edge (IEDG) bit determines which level transition on pin 1 will trigger a free running counter transfer to the input capture register. Reset does not affect the IEDG bit.

0 = negative edge

1 = positive edge

B0, OLVL — The value of the output level (OLVL) bit is clocked into the output level register by the next successful output compare and will appear at pin 2. This bit and the output level register are cleared by RESET.

0 = low output

1 = high output

TIMER STATUS REGISTER (TSR)

The timer status register (TSR) is an 8-bit register of which the three most significant bits contain read-only status information. These three bits indicate the following:

1. A proper transition has taken place at the TCAP pin with an accompanying transfer of the free running counter contents to the input capture register,
2. A match has been found between the free running counter and the output compare register, and
3. A free running counter transition from $FFFF to $0000 has been sensed (timer overflow).

The timer status register is illustrated below followed by a definition of each bit. Refer to timing diagrams shown in Figures 16, 17, and 18 for timing relationship to the timer status register bits.

7	6	5	4	3	2	1	0
ICF	OCF	TOF	0	0	0	0	0

TSR (LOCATION $13)

B7, ICF — The input capture flag (ICF) is set when a proper edge has been sensed by the input capture edge detector. It is cleared by a processor access of the timer status register (with ICF set) followed by accessing the low byte ($15) of the input capture register. Reset does not affect the input compare flag.

B6, OCF — The output compare flag (OCF) is set when the output compare register contents match the contents of the free running counter. The OCF is cleared by accessing the timer status register (with OCF set) and then accessing the low byte ($17) of the output compare register. Reset does not affect the output compare flag.

B5, TOF — The timer overflow flag (TOF) bit is set by a transition of the free running counter from $FFFF to $0000. It is cleared by accessing the timer status register (with TOF set) followed by an access of the free running counter least significant byte ($19). Reset does not affect the TOF bit.

Accessing the timer status register satisfies the first condition required to clear any status bits which happen to be set during the access. The only remaining step is to provide an access of the register which is associated with the status bit. Typically, this presents no problem for the input capture and output compare functions.

A problem can occur when using the timer overflow function and reading the free running counter at random times to measure an elapsed time. Without incorporating the proper precautions into software, the timer overflow flag could unintentionally be cleared if: 1) the timer status register is read or written when TOF is set, and 2) the least significant byte of the free running counter is read but not for the purpose of servicing the flag. The counter alternate register at address $1A and $1B contains the same value as the free running counter (at address $18 and $19); therefore, this alternate register can be read at any time without affecting the timer overflow flag in the timer status register.

During STOP and WAIT instructions, the programmable timer functions as follows: during the wait mode, the timer continues to operate normally and may generate an interrupt to trigger the CPU out of the wait state; during the stop mode, the timer holds at its current state, retaining all data, and resumes operation from this point when an external interrupt is received.

OSCILLATOR CONTROL REGISTER (OCR)

The Oscillator Control Register (OCR, location $11) is an 8-bit register which contains three functional bits. The bits control the source of the Timer input and the main CPU oscillator start-up delay following a STOP instruction. The operation of each bit is as described below:

7	6	5	4	3	2	1	0
0	0	0	EOE	ECC	NDEL	0	0

OCR (LOCATION $11)

B4, EOE — Setting the EOE bit high configures the TCAP/TOSC1 and TCMP/TOSC2 as an oscillator amplifier. A crystal or ceramic resonator network can be connected across the two pins to form an oscillator. For accurate counting, after the EOE bit is set to configure the TCAP/TOSC1 and TCMP/TOSC2 as an oscillator amplifier and a crystal or resonator is connected across the two pins, the user should delay setting the ECC bit until the oscillator has stabilized (typically 2-5ms). RESET and power-up clear the EOE bit.

B3, ECC — Setting the ECC bit high connects the input of the Timer to the TCAP/TOSC1 pad. The signal at the TCAP/TOSC1 pin is divided by four and then applied to the Timer. This allows counting external events with a resolution of four, or use of a frequency different than the main CPU time base. An external clock source can be used, or the EOE bit can be set to allow use of a crystal or resonator. If the EOE bit is set to configure the TCAP/TOSC1 and TCMP/TOSC2 as an oscillator amplifier and a crystal or resonator is connected across the two pins, the user should delay setting the ECC bit until the oscillator has stabilized (typically 2-5ms). RESET and power-up clear the ECC bit.

B2, NDEL — Setting the NDEL bit high overrides the normal 4064 t_{CYC} delay which is introduced when exiting from STOP mode via an interrupt (RESET will clear the NDEL bit). Instead a 2 t_{CYC} delay will be introduced. When the RC oscillator mask option has been chosen, the delay is always 2 t_{CYC} and the NDEL bit has no effect. NDEL is cleared by RESET and power-up.

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 727-9207
FAX: (407) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
Taiwan Limited
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029