EMIF09-02726Sx

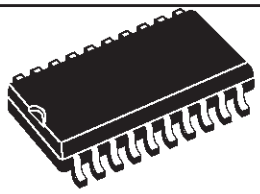
Application Specific Discretes
A.S.D.™

EMI FILTER
INCLUDING ESD PROTECTION

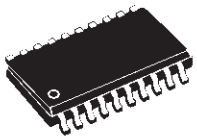
MAIN APPLICATIONS

Where EMI filtering in ESD sensitive equipment is required :

- Computers and printers
- Communication systems
- Mobile phones
- MCU Boards



SO-20



SSOP20

DESCRIPTION

The EMIF09-02726sx is a highly integrated array designed to suppress EMI / RFI noise in all systems subjected to electromagnetic interferences.

Additionally, this filter includes an ESD protection circuitry which prevents the protected device from destruction when subjected to ESD surges up to 15 kV.

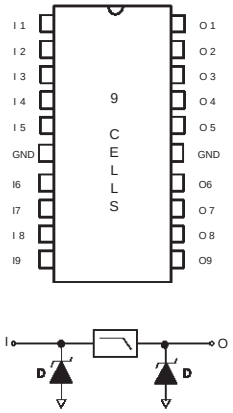
BENEFITS

- Cost-effectiveness compared to discrete solution
- EMI bi-directional low-pass filter
- High efficiency in ESD suppression.
- High reliability offered by monolithic integration

COMPLIES WITH THE FOLLOWING STANDARD:

IEC 1000-4-2 15kV (air discharge)
8 kV (contact discharge)

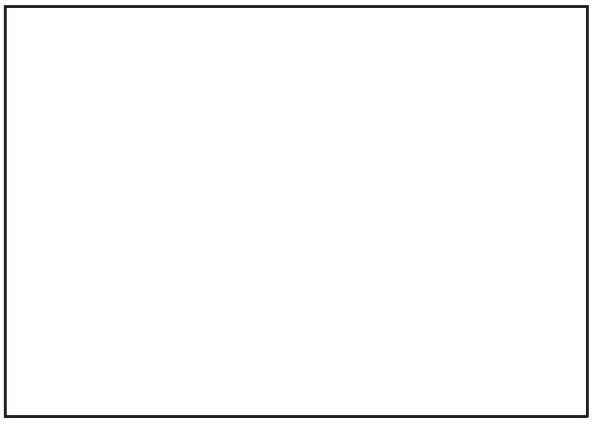
PIN-OUT CONFIGURATION



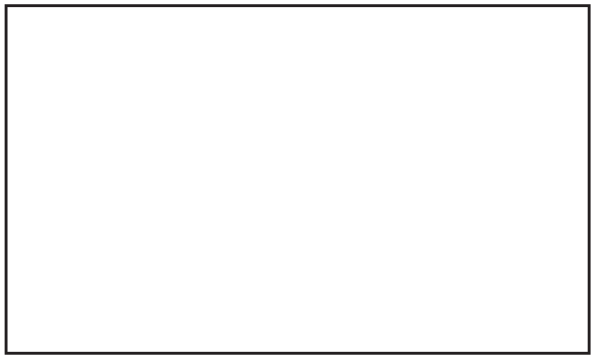
$R_{I/O}$ = 27 Ω, tolerance +/-20%

C_{IN} = 130pF

EMIF09-02726Sx filtering response curves



Typical response to IEC1000-4-2 (16 kV air discharge)

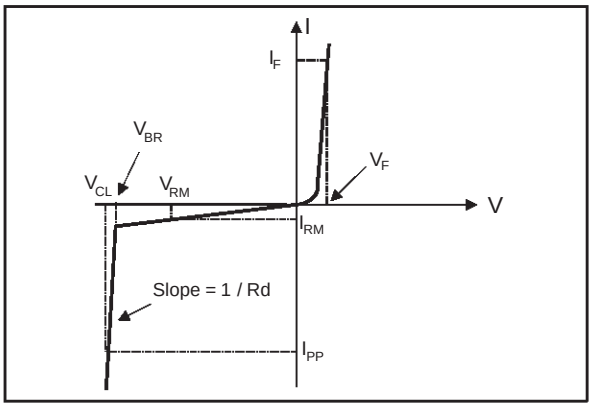


ASD is a trademark of STMicroelectronics

ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25°C)

Symbol	Parameter	Value	Unit
V_{PP}	Maximum electrostatic discharge in following measurement conditions: MIL STD 883C - METHOD 3015-6 IEC1000-4-2 - air discharge IEC1000-4-2 - contact discharge	 25 16 9	 kV
P_{PP}	Peak pulse power (8/20µs)	200	W
T_{stg} T_j	Storage temperature range Junction temperature	- 55 to + 150 150	°C °C
T_{OP}	Operating temperature range	- 40 to + 85	°C

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{CL}	Clamping voltage
V_F	Forward voltage drop
C_{IN}	Input capacitance per line
Rd	Dynamic impedance
I_{RM}	Leakage current
I_{PP}	Peak pulse current



Symbol	Test conditions	Min.	Typ.	Max.	Unit
I_{RM}	V_{RM} = 5.25 V, between any I/O pin and GND			20	µA
V_{BR}	I_R = 1 mA, between any I/O pin and GND	6.1		7.2	V
V_F	IF = 200 mA, between any I/O pin and GND			1.25	V
Rd	I_{PP} = 15 A, t_p = 2.5µs (note 2)		0.3		Ω
C	0V bias V_{RMS} = 30mV F = 1MHz (note 3)		130		pF

Note 1: V_{CL} corresponds to the voltage level seen at the output pin
Note 2: Rd is given per diode
Note 3: C is given per diode

Fig. 1: Peak power dissipation versus initial junction temperature.

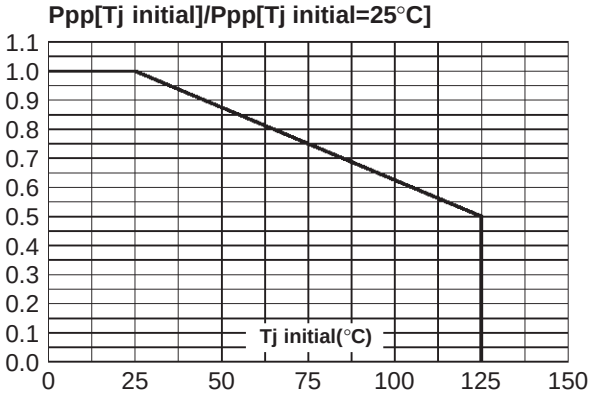


Fig. 2: Peak pulse power versus exponential pulse duration (Tj initial=25°C).

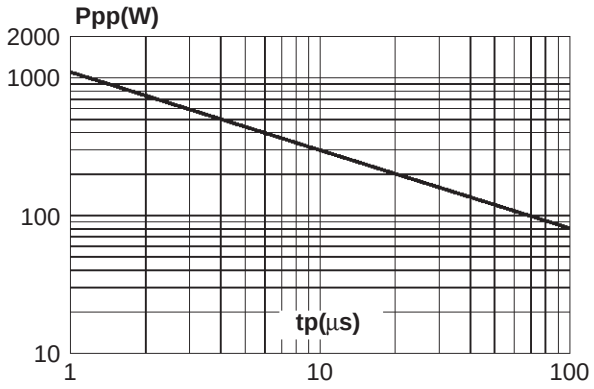


Fig. 3: Clamping voltage versus peak pulse current (Tj initial=25°C).
Rectangular waveform: tp = 2.5µs

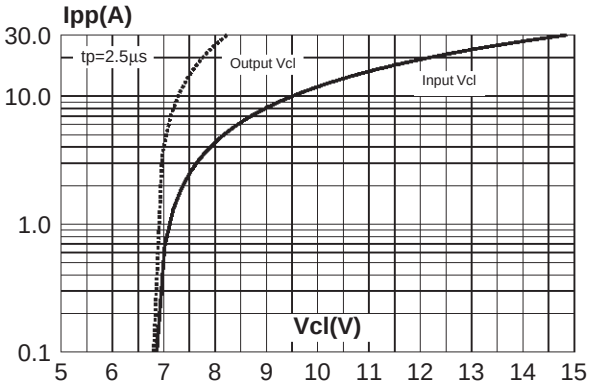


Fig. 4: Input capacitance versus reverse applied voltage (typical values).

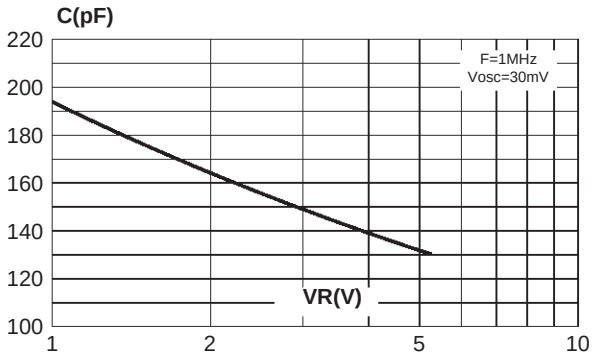


Fig. 5: Relative variation of leakage current versus junction temperature (typical values).

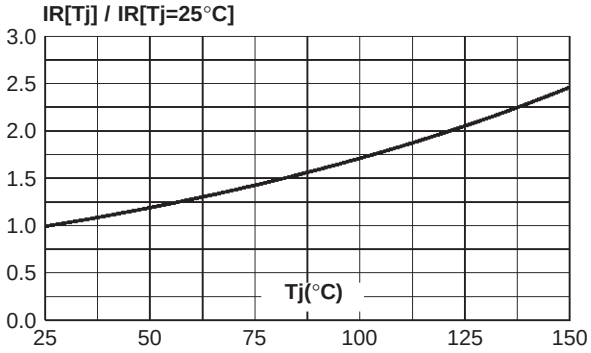
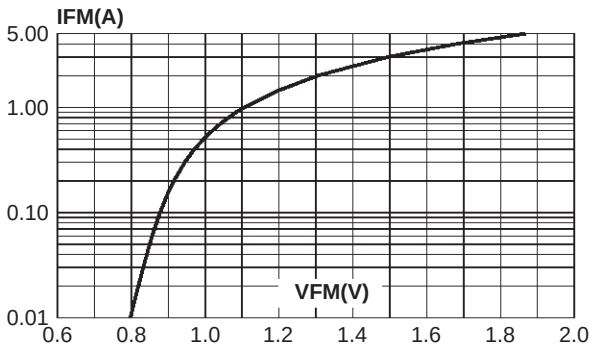


Fig. 6: Peak forward voltage drop versus peak forward current (typical values).
Rectangular waveform: tp = 2.5µs



ESD protection by the EMIF09-02726Sx

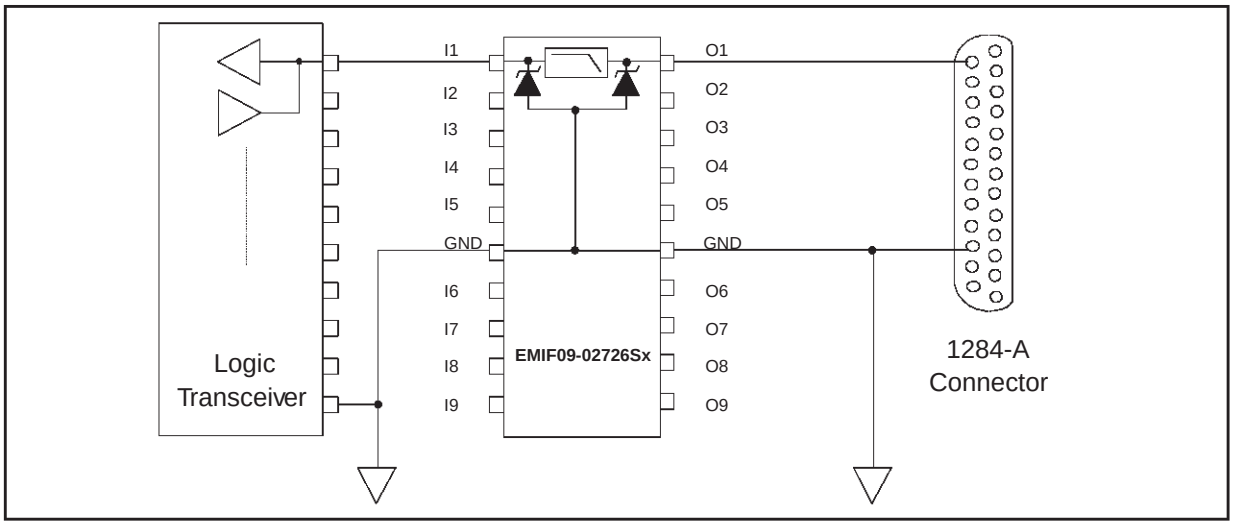
Electrostatic discharge (ESD) is a major cause of failure in electronic systems.

Transient Voltage Suppressors are an ideal choice for ESD protection. They are capable of clamping the incoming transient to a low enough level such that damage to the protected semiconductor is prevented.

Surface mount TVS arrays offer the best choice for minimal lead inductance.

They serve as parallel protection elements, connected between the signal line to ground. As the transient rises above the operating voltage of the device, the TVS array becomes a low impedance path diverting the transient current to ground.

Fig. 7: Example of connection for one cell of the EMIF09-02726Sx



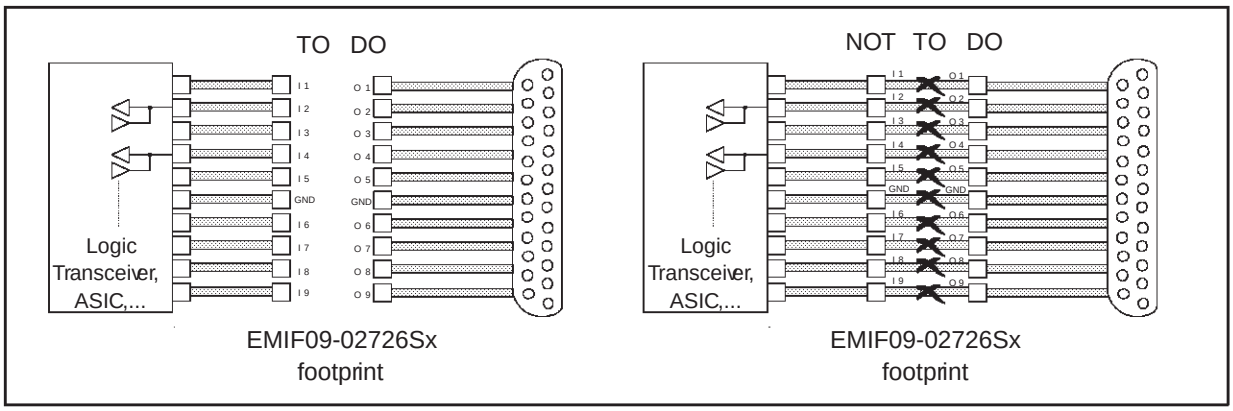
The EMIF09-02726Sx array is the ideal board level protection of ESD sensitive semiconductor components. It provides best efficiency when using separated inputs and outputs, in the so called 4-points structure.

Circuit Board Layout

Circuit board layout is a critical design step in the suppression of ESD induced transients. The following guidelines are recommended :

- The EMIF09-02726Sx should be placed as near as possible to the input terminals or connectors.
- The path length between the ESD suppressor and the protected line should be minimized.
- All conductive loops, including power and ground loops should be minimized.
- The ESD transient return path to ground should be kept as short as possible.
- Ground planes should be used whenever possible.

Fig. 8: Recommended PCB layout to benefit from 4-point structure



TECHNICAL INFORMATION

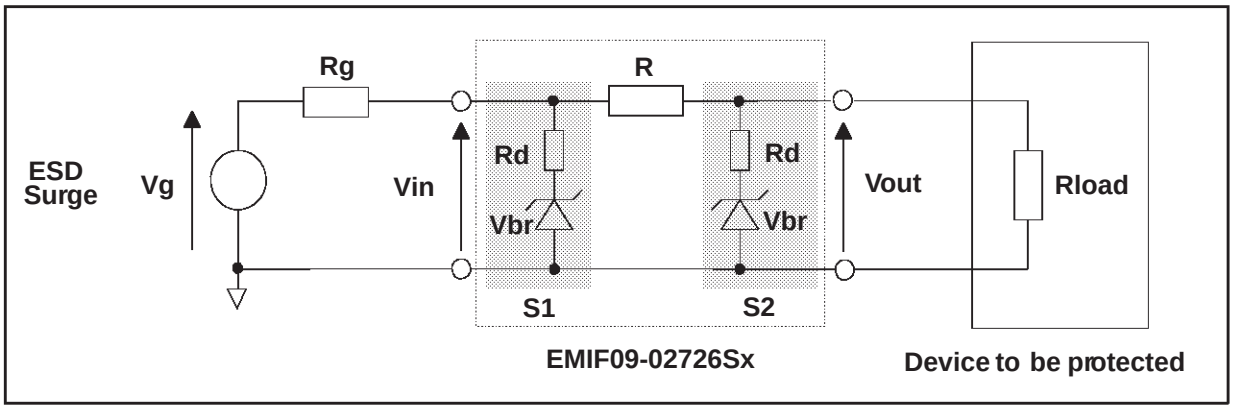
ESD PROTECTION

The EMIF09-02726Sx is particularly optimized to perform high level ESD protection. The clamping voltage is given by the formula:

$$V_{CL} = V_{br} + R_d.I_{PP}$$

The protection function is splitted in 2 stages. As shown in figure A1, the ESD strike is clamped by the first stage S1 and then its remaining overvoltage is applied to the second stage through the resistor R. Such a configuration makes the output voltage very low at the Vout level.

Fig. A1: ESD clamping behavior



To determine the remaining voltages at both Vin and Vout stages, we give the typical dynamic resistance value Rd. Considering that : R>>Rd, Rg>>Rd and Rload>>Rd, the voltages are given by the following formulas:

$$Vin = \frac{R_g.V_{br} + R_d.V_g}{R_g}$$

$$Vout = \frac{R.V_{br} + R_d.Vin}{R}$$

The result of the calculation made for V_G= 8kV, Rg= 330 Ω (IEC1000-4-2 standard), V_{br}=6.6V, Rd=0.3 Ω and R=27 Ω is:

Vin = 13.87V

Vout = 6.75 V

This confirms the very low remaining voltage across the device to be protected. It is also important to note that in this approximation the parasitic inductance effect was not taken into account. This could be few tenths of volts during few ns at the Vin side. This parasitic effect is not present at the Vout side because the current involved after the resistance R is low.

LATCH-UP PHENOMENA

The early aging and destruction of IC's is often due to latch-up phenomena which is principally induced by dV/dt. Thanks to its RC structure, the EMIF09-02726Sx provides a high immunity to latch-up by integration of fast edges. (See the response of EMIF09-02726Sx to a 1ns edge on Fig. A3)

The measurements performed as described below show very clearly the high efficiency of the ESD protection:

- no influence of the parasitic inductances on Vout stage
- Vout clamping voltage very close to Vbr

Fig. A2: Measurement conditions

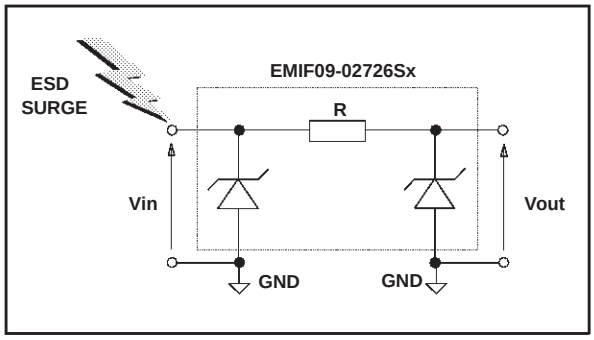


Fig. A3: Remaining voltage at both stages S1 (Vin) and S2 (Vout) during ESD surge

a) Positive surge

b) Negative surge

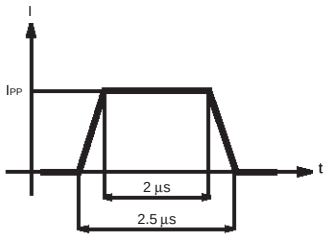
It should be noted that the EMIF09-02726Sx is not only active for positive ESD surges but also for negative ones. For this kind of disturbance, it clamps close to ground voltage as shown in Fig. A3b.

NOTE: DYNAMIC RESISTANCE MEASUREMENT

Generally the PCB designers need to calculate easily the clamping voltage VCL. This is why we give the dynamic resistance in addition to the classical parameters. Figure A4 illustrates the current waveform used to measure the Rd.

As the value of the dynamic resistance remains stable for a surge duration lower than 20µs, the 2.5µs rectangular surge is well adapted. In addition both rise and fall times are optimized to avoid any parasitic phenomenon during the measurement of Rd.

Fig. A4: Rd measurement current wave



2.5µs duration measurement wave

FREQUENCY BEHAVIOR

In addition to the ESD protection, the EMIF09-02726Sx offers an EMI / RFI filtering function thanks to its Pi-filter structure. This low-pass filter is characterized by the following parameters:

- Cut-off frequency 20MHz
- Insertion loss -3dBm
- High frequency rejection >-18dBm

Fig. A5: EMIF09-02726Sx filtering response curves

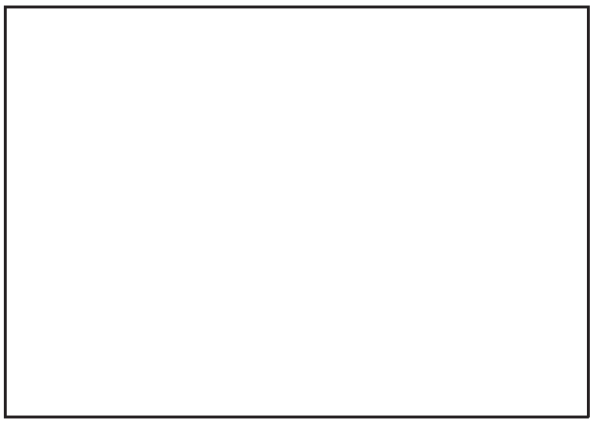
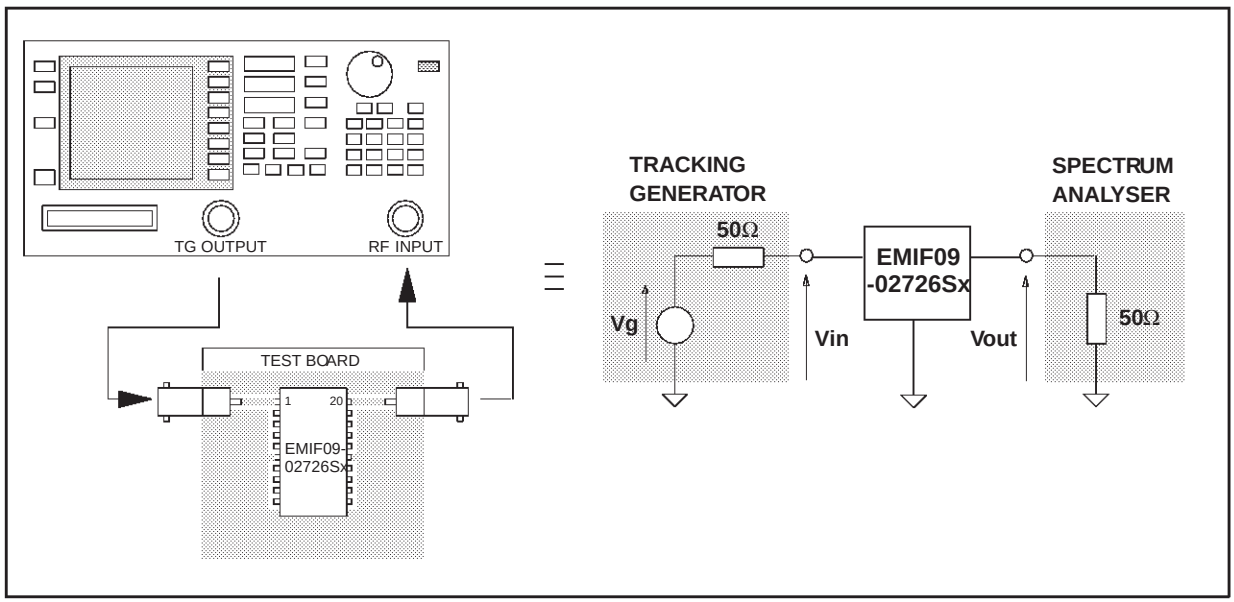


Figure A5 gives these parameters, in particular the signal rejection at the 900MHz GSM frequency is measured at about -21dBm (SO-20) and -26dBm (SSOP20), while the attenuation for FM broadcast range (around 100MHz) is better than -17dBm for both SO-20 and SSOP20.

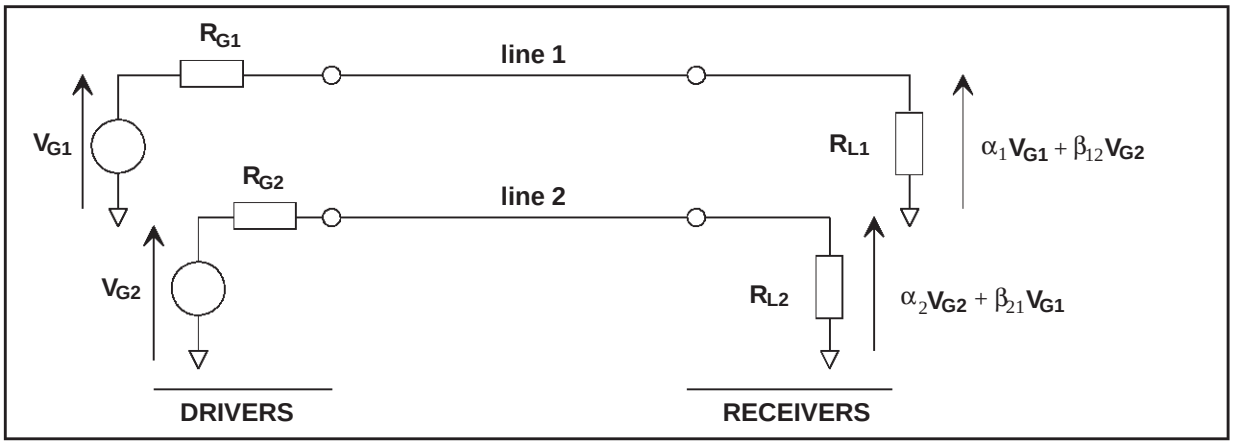
Fig. A6: Measurement conditions



CROSSTALK BEHAVIOR

1- Crosstalk phenomena

Fig. A7: Crosstalk phenomena



The crosstalk phenomena are due to the coupling between 2 lines. The coupling factor (β12 or β21) increases when the gap across lines decreases, particularly in silicon dice. In the example above the expected signal on load RL2 is α2VG2, in fact the real voltage at this point has got an extra value β21VG1. This part of the VG1 signal represents the effect of the crosstalk phenomenon of the line 1 on the line 2. This phenomenon has to be taken into account when the drivers impose fast digital data or high frequency analog signals in the disturbing line. The perturbed line will be more affected if it works with low voltage signal or high load impedance (few kΩ). The following chapters give the value of both digital and analog crosstalk.

2- Digital Crosstalk

Fig. A8: Digital crosstalk measurements

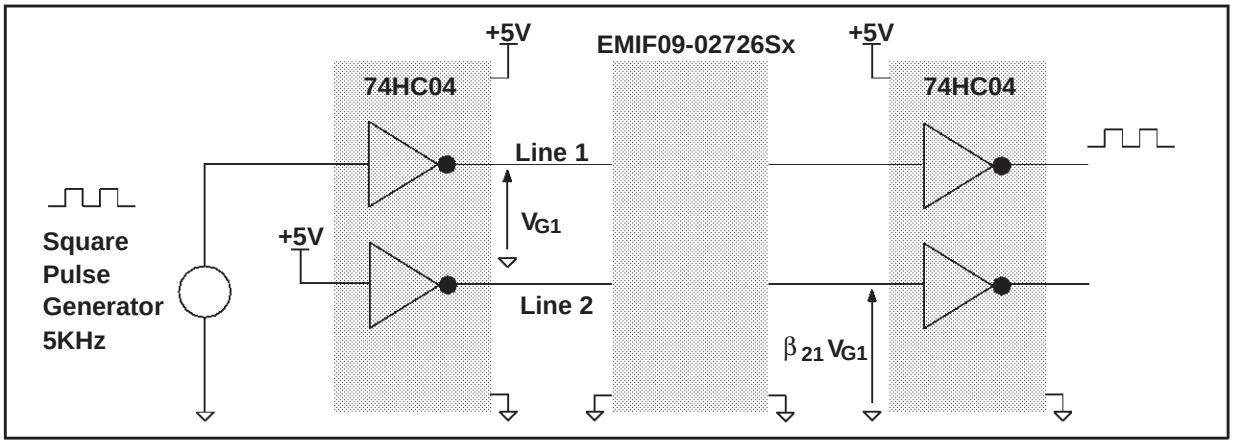
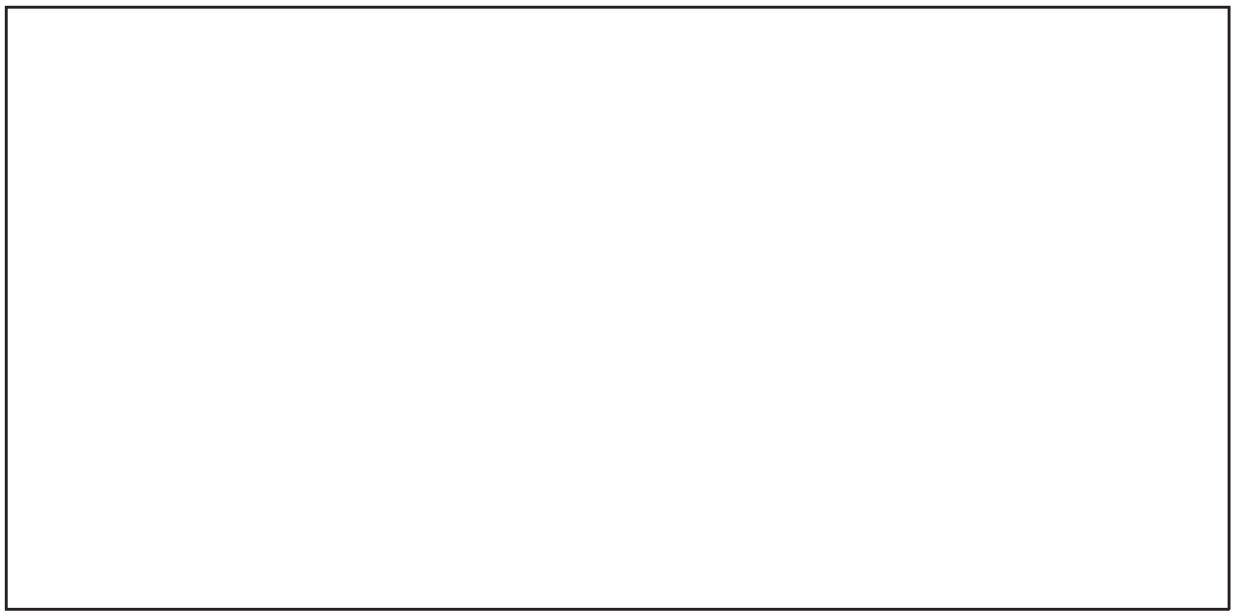


Figure A8 shows the measurement circuit used to quantify the crosstalk effect in a classical digital application.

Figure A9 shows that in the case of a signal from 0 to 5V with a rise time of a few tenths of ns, the impact on the disturbed line is less than 100mV peak to peak. No data disturbance is noted on the concerned line. The same results are obtained with falling edges.

Note: The measurements have been performed in the worst case i.e. on two adjacent cells (1/20 & 2/19).

Fig. A9: Digital crosstalk results



3- Analog Crosstalk

Fig. A10: Analog crosstalk measurements

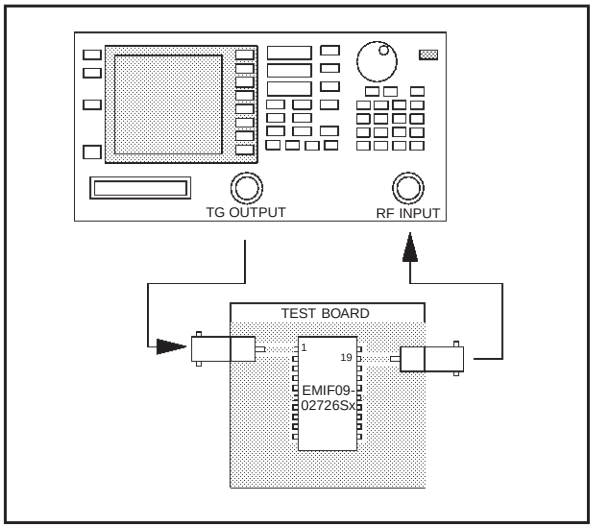


Fig. A11: Typical analog crosstalk results

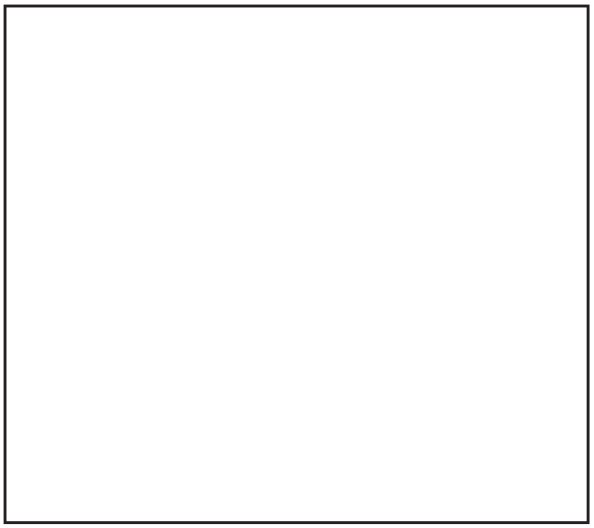


Figure A10 gives the measurement circuit for the analog application. In figure A11, the curves show the effect of cell 1/20 on cell 2/19, no difference is found with other couples of adjacent cells. In usual frequency range of analog signals (up to 100MHz) the effect on disturbed line is less than -32 dBm for SO-20 package and -37dBm for SSOP20 package.

4- PSpice model

Fig. A12: PSpice model of one EMIF09-02726Sx cell

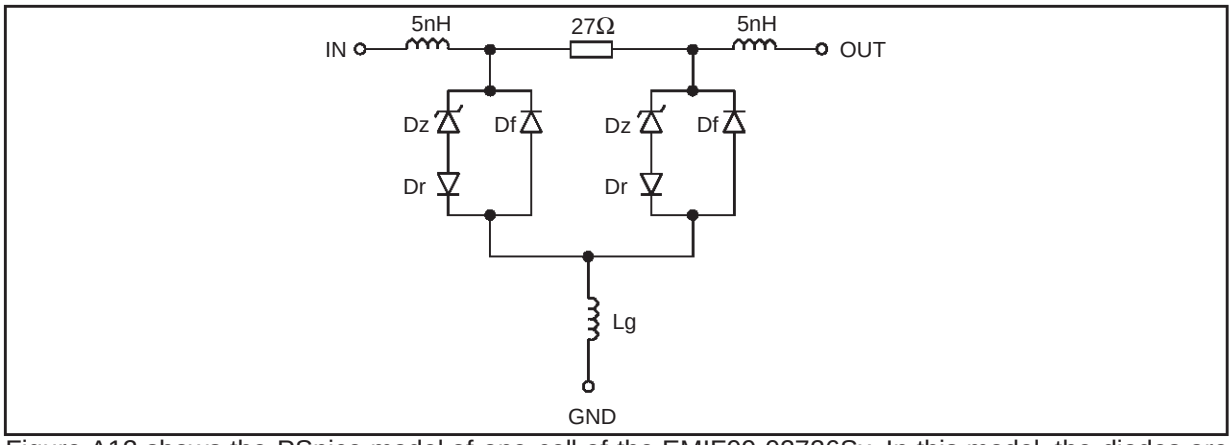


Figure A12 shows the PSpice model of one cell of the EMIF09-02726Sx. In this model, the diodes are defined by the following PSpice parameters :

	Dz	Df	Dr
BV	5.6	1000	1000
Cjo	130p	130p	1p
IBV	1m	100u	100u
IKF	1000	0	1000
IS	10E-21	2.0861E-21	10E-15
ISR	1p	1n	100p
N	1	1	0.6
M	0.3333	0.3333	0.3333
RS	0.3	0.3	1m
VJ	0.6	0.6	0.6
TT	1u	1u	1n

Note: This simulation model is given for an ambient temperature of 27°C.

The value of Lg is depending on the package:

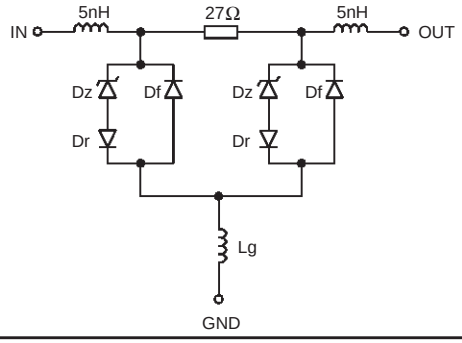
- SSOP20 --> Lg=0.7nH
- SO-20 --> Lg=1.4nH

The comparison between the PSpice simulation and the measured frequency response is given in fig A13a & A13b. This shows that the PSpice model is very close to the product behavior.

Fig. A13: Comparison between PSpice simulation and measured frequency response

a) SSOP20 Package

b) SO-20 Package



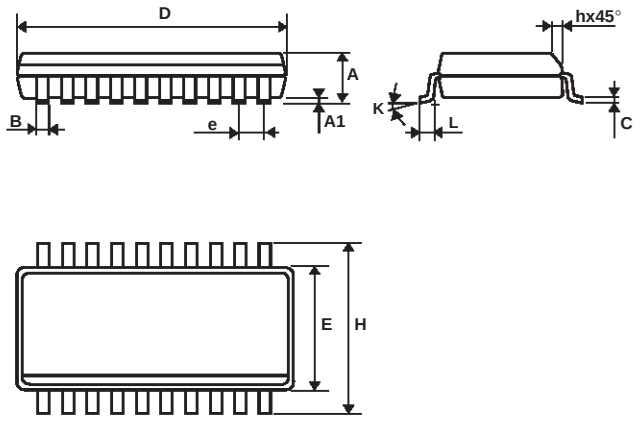
PART NUMBERING AND ORDERING INFORMATION

EMIF 09 - 027 26 S 3

- EMIF: EMI FILTERING
- 09: 9 Bits Wide
- 027: R value (Ω)
- 26: C/10, 2 x 130pF = 260pF
- S: Surface mount
- 3: Package: 3: SO-20, 6: SSOP20

PACKAGE MECHANICAL DATA

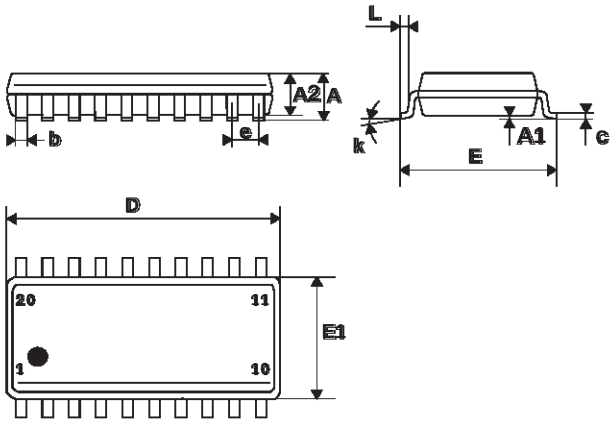
SO-20 (Plastic)



REF.	DIMENSIONS					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.35		2.65	0.092		0.104
A1	0.10		0.20	0.004		0.008
B	0.33		0.51	0.013		0.020
C	0.23		0.32	0.009		0.013
D	12.6		13.0	0.484		0.512
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.0		10.65	0.394		0.419
h	0.25		0.75	0.010		0.029
L	0.50		1.27	0.020		0.050
K	8° (max)					

PACKAGE MECHANICAL DATA

SSOP20 (Plastic)



REF.	DIMENSIONS					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			2.00			0.079
A1			0.25			0.010
A2	1.51		2.00	0.059		0.079
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.10		0.35	0.004		0.014
D	7.05		8.05	0.278		0.317
E	7.60		8.70	0.299		0.343
E1	5.02	6.10	6.22	0.198	0.240	0.245
e		0.65			0.026	
k	0°		10°	0°		10°
L	0.25	0.50	0.80	0.010	0.020	0.031

ORDERING CODE

Order code	Marking	Package	Weight	Delivery mode	Base qty (pcs)
EMIF09-02726S3	ESDR6V1-27	SO-20	0.52 g.	Tube	50
EMIF09-02726S6	ESDR6V1-27	SSOP20	0.18 g.	Tube	50