Data Sheet August 2000 File Number 3040.3

Radiation Hardened 8-Bit Bus Transceiver

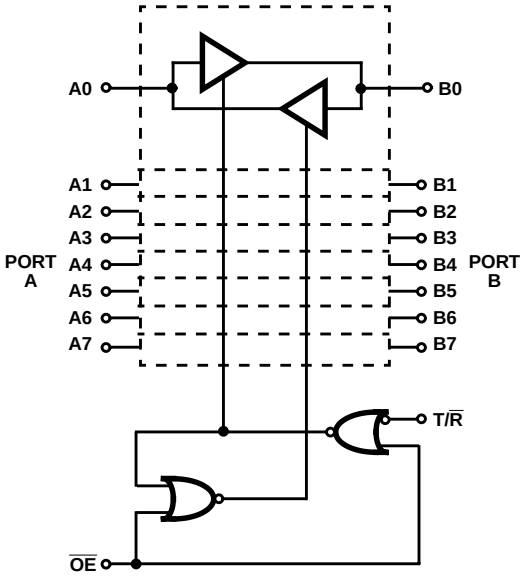
The Intersil HS-82C08RH is a radiation-hardened octal bus transceiver with three-state outputs. It is manufactured using a self-aligned, junction isolated CMOS process and is designed for use with the HS-80C08RH radiation-hardened microprocessor. The HS-82C08RH allows asynchronous two-way communication between data buses. The direction of data flow is determined by the logic level on the transmit/receive (T/$\overline{R}$) input. A logic high on the T/$\overline{R}$ input specifies data flow from Port A to Port B of the device. Conversely, a logic low on the T/$\overline{R}$ input specifies data flow from Port B to Port A. The Output Enable input disables both ports by placing them in the high impedance state.

The HS-82C08RH is ideally suited for a wide variety of buffering applications in radiation-hardened microcomputer systems.

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed here must be used when ordering.

Detailed Electrical Specifications for these devices are contained in SMD 5962-95714. A "hot-link" is provided on our homepage for downloading.
www.intersil.com/spacedefense/space.asp

Functional Diagram



Features

- Electrically Screened to SMD # 5962-95714
- QML Qualified per MIL-PRF-38535 Requirements
- Radiation Performance
  - Total Dose . . . . . 100 krad(Si) (Max)
  - Latch-Up Immune EPI-CMOS . . . . . >1 x 10^{12} rad(Si)/s
- Bidirectional Three-State Input/Outputs
- Low Propagation Delay Time
- Low Power Consumption
- Single Power Supply . . . . . +5V
- Electrically Equivalent to Sandia SA2997
- Military Temperature Range . . . . . -55^{o}C to 125^{o}C

Ordering Information

ORDERING NUMBER	INTERNAL MKT. NUMBER	TEMP. RANGE (^{o}C)
5962R9571401QRC	HS1-82C08RH-8	-55 to 125
5962R9571401QXC	HS9-82C08RH-8	-55 to 125
5962R9571401VRC	HS1-82C08RH-Q	-55 to 125
5962R9571401VXC	HS9-82C08RH-Q	-55 to 125

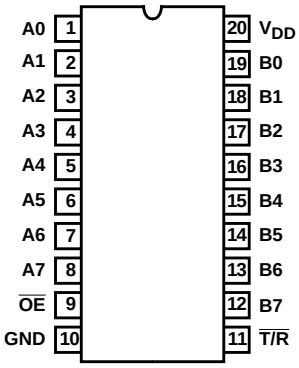
TRUTH TABLE

INPUTS		OPERATION	
OUTPUT ENABLE	TRANSMIT /RECEIVE	PORT A	PORT B
0	0	Out	In
0	1	In	Out
1	X	High Z	High Z

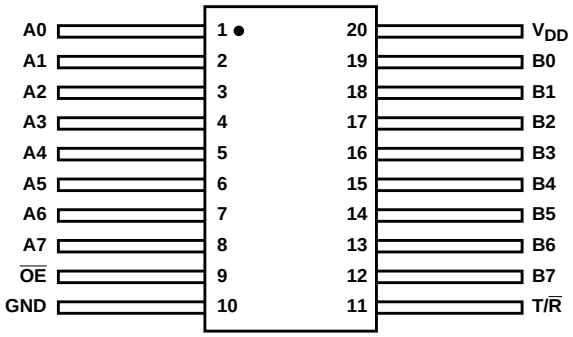
X = Don't Care

Pinouts

20 LEAD CERAMIC DUAL-IN-LINEMETAL-SEAL PACKAGE (SBDIP) MIL-STD-1835, CDIP2-T20
TOP VIEW

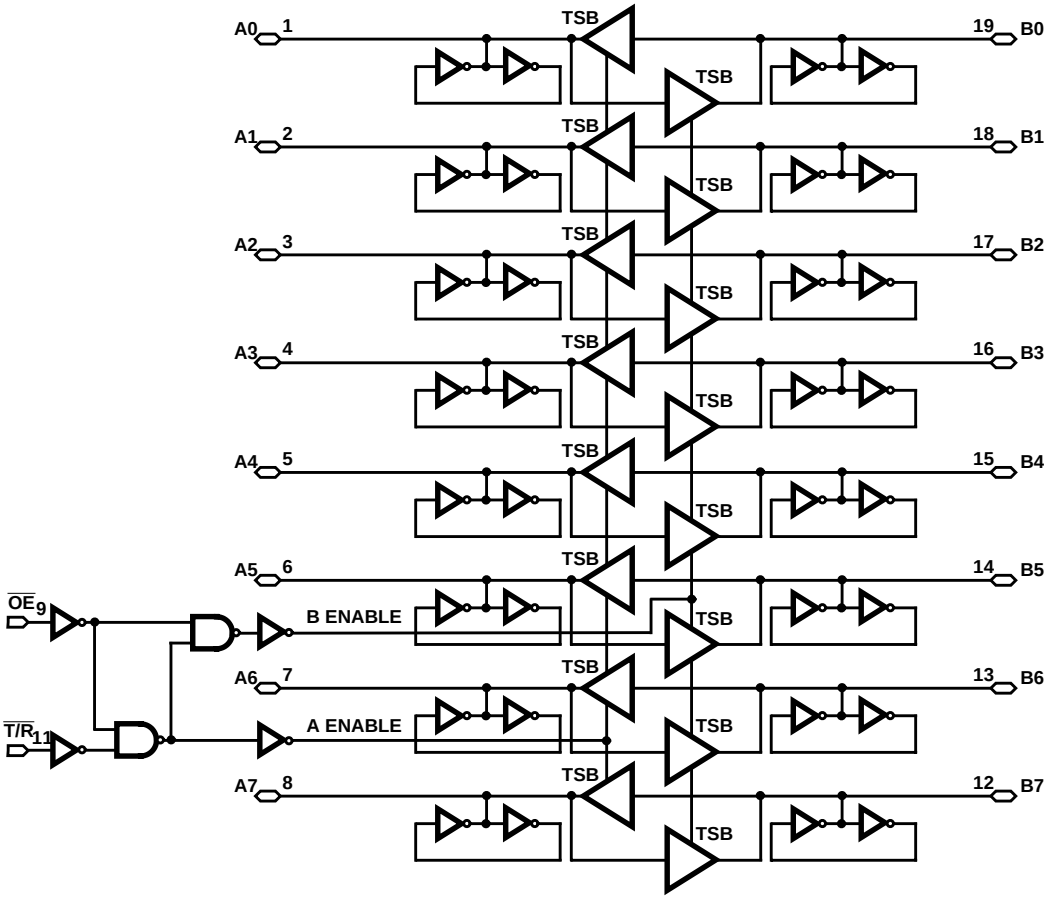


20 LEAD CERAMIC METAL SEALFLATPACK PACKAGE (FLATPACK) MIL-STD-1835, CDFP4-F20
TOP VIEW



PIN	DESCRIPTION	PIN	DESCRIPTION
A0-A7	Local Bus Data I/O Pins	T/$\overline{R}$	Transmit/Receive Input
B0-B7	System Bus Data I/O Pins	$\overline{OE}$	Active Low Output Enable

Logic Diagram



NOTE: An Important caveat that is applicable to CMOS devices in general is that unused inputs should never be left floating. This rule applies to inputs connected to a three-state bus. The need for external pull-up resistors during three-state bus conditions is eliminated by the presence of regenerative latches on the following HS-82C08RH pins. A0-7 and B0-7 The functional block diagram depicts one of these pins with the regenerative latch. When the CMOS driver assumes the high impedance state, the latch holds the bus in whatever logic state (high or low) it was before the three-state condition. A transient drive current of ±1.5mA at $V_{DD}/2$ ±0.5V for 10ns is required to switch the latch. Thus, CMOS device inputs connected to the bus are not allowed to float during three-state conditions.

Switching Time Waveforms

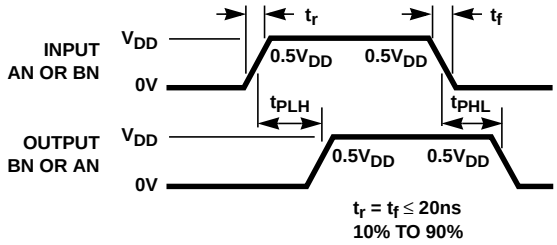
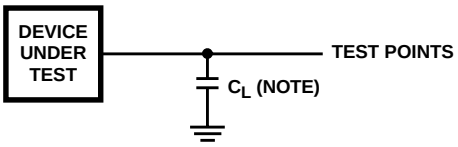


FIGURE 1. PORT TO PORT



NOTE: C_L includes stray and jig capacitance.

FIGURE 2. AC TESTING LOAD CIRCUIT

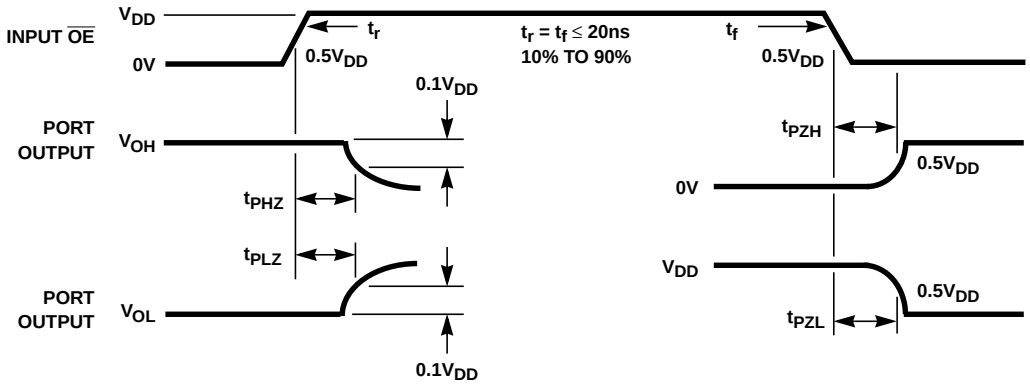


FIGURE 3. $\overline{OE}$ TO HIGH-IMPEDANCE, $\overline{OE}$ TO PORT OUTPUT

Die Characteristics

DIE DIMENSIONS:

76.0 mils x 89.4 mils x 14 mils ±1 mil

INTERFACE MATERIALS:

Glassivation:

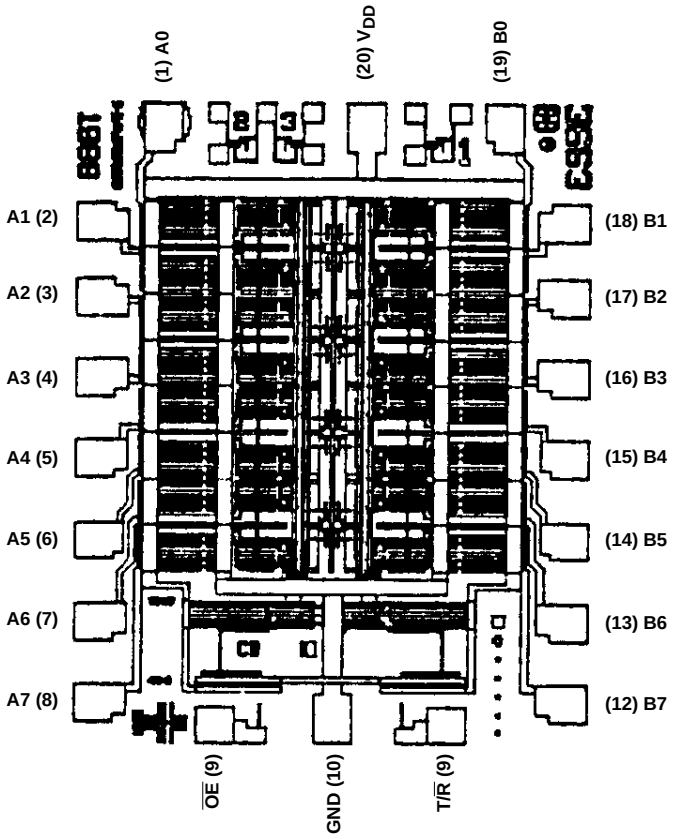
Type: SiO_2
Thickness: 8kÅ ±1kÅ

Top Metallization:

Type: Si - Al
Thickness: 11kÅ ±2kÅ

Metallization Mask Layout

HS-82C08RH



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