

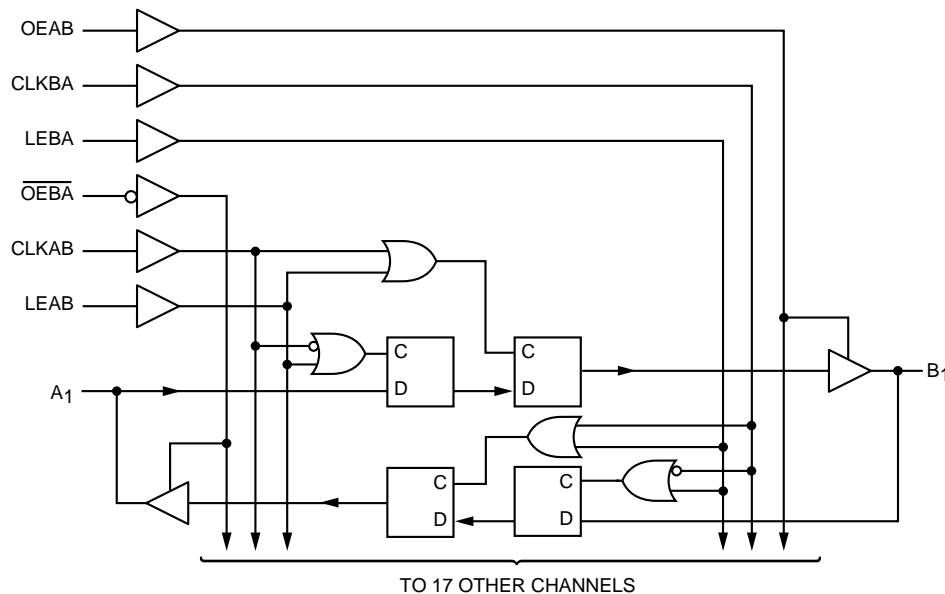
## FEATURES/BENEFITS

- 5V tolerant inputs and outputs
- Bus Hold feature holds last active state during 3-state operation
- 10 $\mu$ A I<sub>CCQ</sub> quiescent power supply current
- Hot insertable
- 2.0V–3.6V V<sub>CC</sub> supply operation
- $\pm$ 24mA balanced output drive
- Power down high impedance inputs and outputs
- t<sub>PD</sub> = 4.6ns max.
- Input hysteresis for noise immunity
- Meets or exceeds JEDEC Standard 36 specifications
- Multiple power and ground pins for low noise
- Operating temperature range:  
 –40°C to 85°C
- Latch-up performance exceeds 500mA
- ESD performance:  
 Human body model > 2000V  
 Machine model > 200V
- Packages available:  
 56-pin TSSOP  
 56-pin SSOP

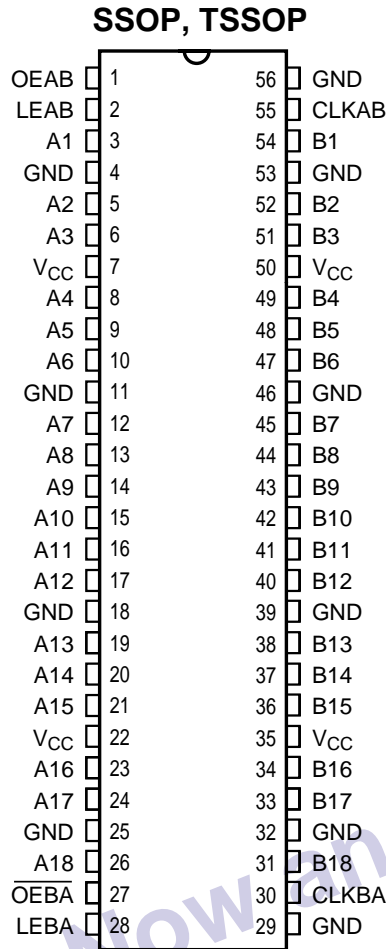
## DESCRIPTION

The LVCH16501A is an 18-bit registered bus transceiver with three-state outputs that are ideal for driving address and data buses. These high-speed, low-power registered transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched and clocked modes. The QS74LVCH16501A provides Bus Hold circuitry on the data inputs to retain the last active state during 3-state operation, eliminating the need for external pull-up resistors. The 3.3V LVC family features low power, low switching noise, and fast switching speeds for low power portable applications as well as high-end advanced workstation applications. 5V tolerant inputs and outputs allow this LVC product to be used in mixed 5V and 3.3V applications. Easy board layout is facilitated by the use of flow-through pinouts and byte enable controls provide architectural flexibility for systems designers. To accommodate hot-plug or live insertion applications, of this product is designed not to load an active bus when V<sub>CC</sub> is removed. However, during power up or power down sequence,  $\overline{OE}$  should be tied to V<sub>CC</sub> to ensure high-impedance state on the outputs.

**Figure 1. Functional Block Diagram**



**Figure 2. Pin Configuration**  
(All Pins Top View)



**Table 1. Pin Description**

Name	Description
OEAB	A-to-B Output Enable Input
$\overline{OEBA}$	B-to-A Output Enable Input (Active Low)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
Ax	A-to-B Data Inputs or B-to-A 3-State Outputs
Bx	B-to-A Data Inputs or A-to-B 3-State Outputs

**Table 2. Function Table <sup>(1)</sup>**

Inputs				Outputs
OEAB	LEAB	CLKAB	Ax	Bx
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	H	X	B <sup>(2)</sup>
H	L	L	X	B <sup>(3)</sup>

**Notes:**

1. A-to-B data flow is shown. B-to-A data flow is similar but uses  $\overline{OEBA}$ , LEBA, and CLKBA.
2. Output level before the indicated steady-state input conditions were established.
3. Output level before the indicated steady-state input conditions were established, provided that CLKAB was LOW before LEAB went LOW.

**Table 3. Absolute Maximum Ratings**

Supply Voltage to Ground .....	-0.5V to 7.0V
DC Output Voltage $V_{OUT}$	
Outputs HIGH-Z .....	-0.5V to 7.0V
Outputs Active .....	-0.5V to $V_{CC} + 0.5V$
DC Input Voltage $V_{IN}$ .....	-0.5V to 7.0V
DC Input Diode Current with $V_{IN} < 0$ .....	-50mA
DC Output Diode Current	
$V_O < 0$ .....	-50mA
$V_O > V_{CC}$ .....	50mA
DC Output Source/Sink Current ( $I_{OH}/I_{OL}$ ) .....	$\pm 50mA$
DC Supply Current per Supply Pin .....	$\pm 100mA$
DC Ground Current per Ground Pin .....	$\pm 100mA$
$T_{STG}$ Storage Temperature .....	-65°C to 150°C

**Note:** Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

**Table 4. Recommended Operating Conditions**

Symbol	Parameter	Min	Max	Unit	
$V_{CC}$	Supply Voltage, Operating	2.0	3.6	V	
	Supply Voltage, Data Retention Only	1.5	3.6		
$V_{IH}$	Input HIGH Voltage	$V_{OL} = 2.7$ to 3.6V	2.0	V	
$V_{IL}$	Input LOW Voltage	$V_{CC} = 2.7$ to 3.6V	—	0.8	V
$V_{IN}$	Input Voltage	0	5.5	V	
$V_{OUT}$	Output Voltage in Active State	0	$V_{CC}$	V	
	Output Voltage in "OFF" State	0	5.5		
$I_{OH}$	Output Current HIGH	$V_{CC} = 3.0$ –3.6V	—	-24	mA
		$V_{CC} = 2.7V$		-12	
$I_{OL}$	Output Current LOW	$V_{CC} = 3.0$ –3.6V	—	24	mA
		$V_{CC} = 2.7V$	—	12	
$\Delta t/\Delta v$	Input Transition Slew Rate	—	10	ns/V	
$T_A$	Operating Free Air Temperature	-40	85	°C	

## QS74LVCH16501A ADVANCE INFORMATION

**Table 5. DC Electrical Characteristics Over Operating Range**

Industrial Temperature Range,  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions	Min	Typ <sup>(1)</sup>	Max	Unit
$V_{OH}$	Output HIGH Voltage	$V_{CC} = 2.7\text{V}$ , $I_{OH} = -100\mu\text{A}$ $V_{CC} = 2.7\text{V}$ , $I_{OH} = -12\text{mA}$ $V_{CC} = 3.0\text{V}$ , $I_{OH} = -12\text{mA}$ $V_{CC} = 3.0\text{V}$ , $I_{OH} = -24\text{mA}$	$V_{CC} - 0.2$ 2.2 2.4 2.2	— — — —	— — — —	V
$V_{OL}$	Output LOW Voltage	$V_{CC} = 2.7\text{V}$ , $I_{OL} = 100\mu\text{A}$ $V_{CC} = 2.7\text{V}$ , $I_{OL} = 12\text{mA}$ $V_{CC} = 3.0\text{V}$ , $I_{OL} = 24\text{mA}$	— — —	— — —	0.2 0.4 0.55	V
$V_{IK}$	Input Clamp Voltage	$V_{CC} = 2.7\text{V}$ , $I_{IN} = -18\text{mA}$	—	-0.7	-1.2	V
$I_I$	Input Leakage Current	$V_I = 0\text{V}$ , $V_I = 5.5\text{V}$ , $V_{CC} = 3.6\text{V}$	—	—	$\pm 1.0$	$\mu\text{A}$
$ I_{BH} $	Bus Hold Inputs Overdrive Current <sup>(2,3)</sup>	$V_{CC} = 3.6\text{V}$ , $V_{IN} = 0\text{V}$ or $V_{IN} = V_{CC}$ $V_{CC} = 3.6\text{V}$ , $0.8\text{V} < V_{IN} < 2.0\text{V}$	— —	— —	50 500 <sup>(4)</sup>	$\mu\text{A}$
$I_{BHH}$ $I_{BHL}$	Bus Hold Input Sustaining Current	$V_{CC} = 3\text{V}$	$V_{IN} = 2.0\text{V}$ $V_{IN} = 0.8\text{V}$	-75 75	— —	$\mu\text{A}$
$I_{OZ}$	High-Z I/O Leakage	$V_O = 0\text{V}$ , $V_O = 5.5\text{V}$ , $V_I = V_{IH}$ or $V_{IL}$ , $V_{CC} = 3.6\text{V}$	—	—	$\pm 1.0$	$\mu\text{A}$
$I_{OFF}$	Power Off Leakage	$V_{CC} = 0\text{V}$ , $V_I$ or $V_O = 5.5\text{V}$	—	—	10	$\mu\text{A}$
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = 3.6\text{V}$ , $V_{IN} = V_{CC}$ or GND	—	0.1	10	$\mu\text{A}$
$\Delta I_{CC}$	Quiescent Power Supply Current per Control Inputs at TTL HIGH	$V_{CC} = 3.6\text{V}$ , $V_{IN} = V_{CC} - 0.6\text{V}^{(5)}$	—	2.0	3.0	$\mu\text{A}$
	Quiescent Power Supply Current per Bus Hold Inputs at TTL HIGH	$V_{CC} = 3.6\text{V}$ , $V_{IN} = V_{CC} - 0.6\text{V}^{(5)}$	—	75	500	$\mu\text{A}$

**Notes:**

- Typical values are at  $V_{CC} = 3.3\text{V}$  and  $T_A = 25^{\circ}\text{C}$ .
- These parameters are guaranteed by characterization, but not production tested.
- Pins with Bus Hold are identified in the pin description.
- An external driver must provide at least  $|I_{BH}|$  during transition to guarantee that the Bus Hold input will change state.
- Per TTL driven input. All other inputs at  $V_{CC}$  or GND.

**Table 6. Dynamic Switching Characteristics**

Symbol	Parameter	Test Conditions	Typ <sup>(1)</sup>	Unit
$V_{OLP}$	Quiet Output Dynamic Peak $V_{OL}$	$C_L = 50\text{pF}$ , $V_{CC} = 3.3\text{V}$ $V_{IH} = 3.3\text{V}$ , $V_{IL} = 0\text{V}$	0.8	V
$V_{OLV}$	Quiet Output Dynamic Valley $V_{OL}$	$C_L = 50\text{pF}$ , $V_{CC} = 3.3\text{V}$ $V_{IH} = 3.3\text{V}$ , $V_{IL} = 0\text{V}$	0.8	V
$C_{PD}$	Power Dissipation	$C_L = 50\text{pF}$ , $f = 10\text{MHz}$ , $V_{CC} = 3.3 \pm 0.3\text{V}$	Output Enable Output Disable	35 6
				$\text{pF}$

**Note:**

- Typical values are at  $V_{CC} = 3.3\text{V}$ ,  $25^{\circ}\text{C}$  ambient.

**Table 7. Capacitance<sup>(1)</sup>**

Symbol	Pins	Conditions	Typ	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V, V <sub>OUT</sub> = 0V, f = 1MHz	7.0	pF
C <sub>I/O</sub>	I/O Capacitance	V <sub>IN</sub> = 0V, V <sub>OUT</sub> = 0V, f = 1MHz	8.0	pF

**Note:**

1. Capacitance is characterized but not production tested.

**Table 8. Switching Characteristics Over Operating Range**

Industrial Temperature Range, T<sub>A</sub> = -40°C to 85°C

C<sub>LOAD</sub> = 50pF, R<sub>LOAD</sub> = 500Ω unless otherwise noted.

Symbol	Description <sup>(1)</sup>	V <sub>CC</sub> = 3.3 ±0.3V		V <sub>CC</sub> = 2.7V <sup>(2)</sup>		Unit
		Min	Max	Min	Max	
f <sub>MAX</sub>	CLKAB or CLKBA Frequency <sup>(2)</sup>	150	—	—	—	MHz
t <sub>PD</sub>	Propagation Delay Ax to Bx or Bx to Ax	1.5	4.6	1.5	5.2	ns
	Propagation Delay LEBA to Ax, LEAB to Bx	1.5	5.3	1.5	6.0	
	Propagation Delay CLKBA to Ax, CLKAB to Bx	1.5	5.3	1.5	6.0	
t <sub>EN</sub>	Output Enable Time OEBA to Ax, OEAB to Bx	1.5	5.6	1.5	6.0	ns
t <sub>DIS</sub>	Output Disable Time <sup>(2)</sup> OEBA to Ax, OEAB to Bx	1.5	5.8	1.5	6.5	ns
t <sub>SU</sub>	Setup Time HIGH or LOW Ax to CLKAB, Bx to CLKBA	3.0	—	3.0	—	ns
t <sub>H</sub>	Hold Time HIGH or LOW Ax to CLKAB, Bx to CLKBA	0	—	0	—	ns
	Setup Time HIGH or Low	3.0	—	3.0	—	
t <sub>SU</sub>	Ax to LEAB Bx to LEBA					Clock LOW
	t <sub>H</sub>	Hold Time HIGH or LOW Ax to LEAB, Bx to LEBA	1.5	—	1.5	—
t <sub>W</sub>		Pulse Width <sup>(2)</sup>	3.0	—	3.0	—
t <sub>SK(O)</sub>	Output Skew <sup>(3)</sup>	—	0.5	—	0.5	ns

**Notes:**

1. See test circuit and waveforms. Minimum Limits are guaranteed but not tested on Propagation Delays.
2. Guaranteed by characterization.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by characterization but not production tested.

TEST CIRCUIT AND WAVEFORMS

Figure 3. Test Circuit

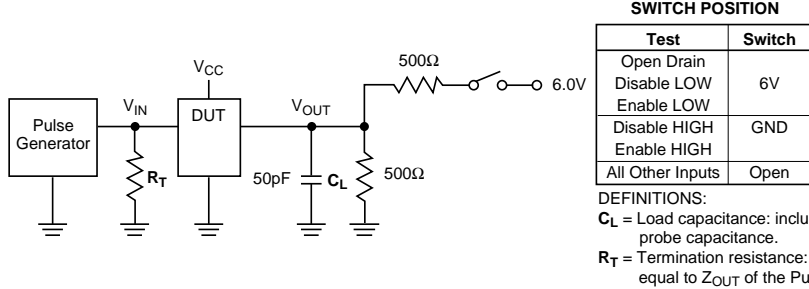


Figure 4. Setup, Hold, and Release Timing

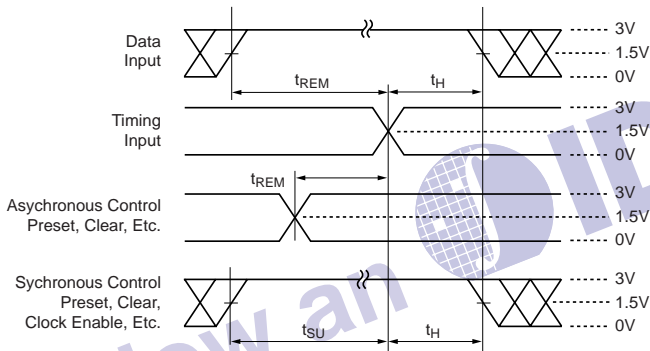


Figure 6. Pulse Width

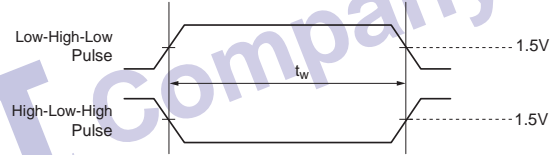


Figure 5. Enable and Disable Timing

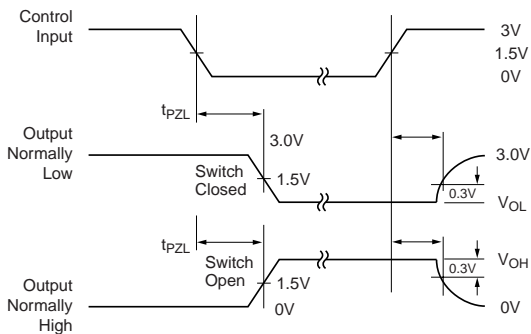
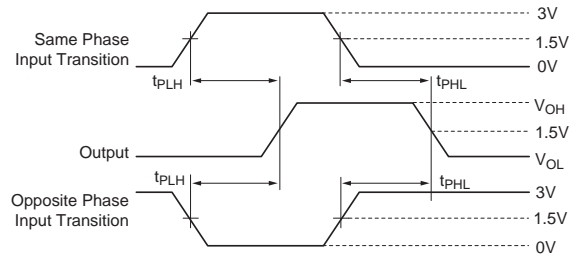


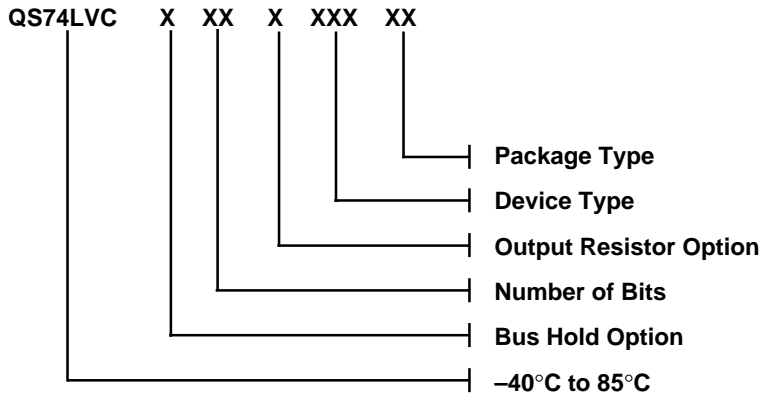
Figure 7. Propagation Delay



Notes:

1. Input Control Enable = LOW and Input Control Disable = HIGH.
2. Pulse Generator for All Pulses: Rate  $\leq$  1.0MHz;  $Z_{OUT} \leq 50\Omega$ ;  $t_F, t_R \leq 2.5ns$ .

**ORDERING INFORMATION**



**Bus Hold Option:**  
H – with Bus Hold

**Number of Bits:**  
16 – 18-Bit

**Output Resistor Option:**  
Blank – No Output Resistor

**Device Type:**  
501

**Package Type:**  
PV – SSOP, 300 mil  
PA – TSSOP, 240 mil

Now an  IDT™ company