QUALITY SEMICONDUCTOR, INC.

# High-Speed CMOS 3.3V 8-Bit Transceiver with Bus Hold

**QS74LVCH245A**

## FEATURES/BENEFITS

- 5V tolerant inputs and outputs
- Bus Hold feature holds last active state during 3-state operation
- 10µA $I_{CCQ}$ quiescent power supply current
- Hot insertable
- 2.0V–3.6V $V_{CC}$ supply operation
- ±24mA balanced output drive
- Power down high impedance inputs and outputs
- Input hysteresis for noise immunity
- Meets or exceeds JEDEC Standard 36 specifications
- Multiple power and ground pins for low noise
- Operating temperature range:
  –40°C to 85°C
- Latch-up performance exceeds 500mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V
- Packages available:
  20-pin QSOP
  20-pin SOIC
  20-pin TSSOP

## DESCRIPTION

The LVCH245A is an 8-bit non-inverting transceiver that has three-state outputs which are useful for bus-oriented applications. The Transmit/Receive (T/R) input determines the direction of data flow, either from A to B or B to A, and the Output Enable ($\overline{OE}$) inputs enables the selected port for output. The 3.3V LVC family features low power, low switching noise, and fast switching speeds for low power portable applications as well as high-end, advanced workstation applications. 5V tolerant inputs and outputs allow this LVC product to be used in mixed-voltage applications. Active Bus Hold feature on LVCH245A retains last valid logic state at unused or floating data inputs, thus eliminating the need for external pull-up resistors. To accomodate hot-plug or live insertion applications, this product is designed not to load an active bus when $V_{CC}$ is removed. However, during power up or power down sequence, $\overline{OE}$ should be tied to $V_{CC}$ to ensure high-impedance state on the outputs.

**Figure 1. Functional Block Diagram**

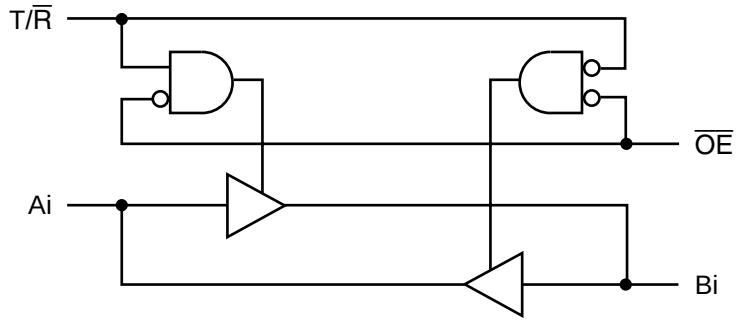
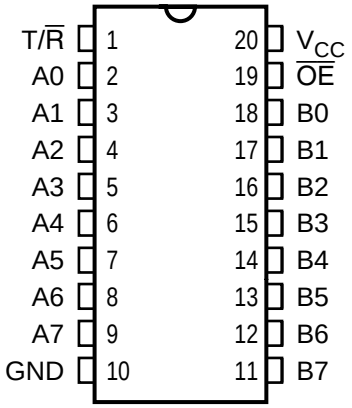


**Figure 2. Pin Configuration**
(All Pins Top View)

**SOIC, QSOP, TSSOP**




## Table 1. Pin Description

| Name | I/O | Description |
|---|---|---|
| Ai | I/O | Data Bus A |
| Bi | I/O | Data Bus B |
| $T/\overline{R}$ | I | Direction |
| $\overline{OE}$ | I | Three-State Output Enable |

## Table 2. Function Table

| $\overline{OE}$ | $T/\overline{R}$ | A | B | Function |
|---|---|---|---|---|
| H | X | Hi-Z | Hi-Z | Disable |
| L | L | Output | Input | Bus B to Bus A |
| L | H | Input | Output | Bus A to Bus B |

## Table 3. Absolute Maximum Ratings

Supply Voltage to Ground ..... –0.5V to 7.0V
DC Output Voltage $V_{OUT}$
  Outputs HIGH-Z ..... –0.5V to 7.0V
  Outputs Active ..... –0.5V to $V_{CC}$ + 0.5V
DC Input Voltage $V_{IN}$ ..... –0.5V to 7.0V
DC Input Diode Current with $V_{IN} < 0$ ..... –50mA
DC Output Diode Current
  $V_O < 0$ ..... –50mA
  $V_O > V_{CC}$ ..... 50mA
DC Output Source/Sink Current ($I_{OH}/I_{OL}$) ..... ±50mA
DC Supply Current per Supply Pin ..... ±100mA
DC Ground Current per Ground Pin ..... ±100mA
$T_{STG}$ Storage Temperature ..... –65°C to 150°C

**Note:** Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

## Table 4. Recommended Operating Conditions

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage, Operating | | 2.0 | 3.6 | V |
| | Supply Voltage, Data Retention Only | | 1.5 | 3.6 | |
| $V_{IH}$ | Input HIGH Voltage | $V_{OL}$ = 2.7 to 3.6V | 2.0 | — | V |
| $V_{IL}$ | Input LOW Voltage | $V_{CC}$ = 2.7 to 3.6V | — | 0.8 | V |
| $V_{IN}$ | Input Voltage | | 0 | 5.5 | V |
| $V_{OUT}$ | Output Voltage in Active State | | 0 | $V_{CC}$ | V |
| | Output Voltage in “OFF” State | | 0 | 5.5 | |
| $I_{OH}$ | Output Current HIGH | $V_{CC}$ = 3.0–3.6V | — | –24 | mA |
| | | $V_{CC}$ = 2.7V | | –12 | |
| $I_{OL}$ | Output Current LOW | $V_{CC}$ = 3.0–3.6V | — | 24 | mA |
| | | $V_{CC}$ = 2.7V | — | 12 | |
| $\Delta t/\Delta v$ | Input Transition Slew Rate | | — | 10 | ns/V |
| $T_A$ | Operating Free Air Temperature | | –40 | 85 | °C |

## Table 5. DC Electrical Characteristics Over Operating Range

Industrial Temperature Range, $T_A$ = –40°C to 85°C

| Symbol | Parameter | Test Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = 2.7V, $I_{OH}$ = –100µA<br>$V_{CC}$ = 2.7V, $I_{OH}$ = –12mA<br>$V_{CC}$ = 3.0V, $I_{OH}$ = –12mA<br>$V_{CC}$ = 3.0V, $I_{OH}$ = –24mA | $V_{CC}$ –0.2<br>2.2<br>2.4<br>2.2 | —<br>—<br>—<br>— | —<br>—<br>—<br>— | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = 2.7V, $I_{OL}$ = 100µA<br>$V_{CC}$ = 2.7V, $I_{OL}$ =12mA<br>$V_{CC}$ = 3.0V, $I_{OL}$ = 24mA | —<br>—<br>— | —<br>—<br>— | 0.2<br>0.4<br>0.55 | V |
| $V_{IK}$ | Input Clamp Voltage | $V_{CC}$ = 2.7V, $I_{IN}$ = –18mA | — | –0.7 | –1.2 | V |
| $I_I$ | Input Leakage Current | $V_I$ = 0V, $V_I$ = 5.5V, $V_{CC}$ = 3.6V | — | — | ±1.0 | µA |
| $\|I_{BH}\|$ | Bus Hold Inputs Overdrive Current[2,3] | $V_{CC}$ = 3.6V, $V_{IN}$ =0V or $V_{IN}$ = $V_{CC}$ | — | — | 50 | µA |
| | | $V_{CC}$ = 3.6V, 0.8V < $V_{IN}$ < 2.0V | — | — | 500[4] | |
| $I_{BHH}$<br>$I_{BHL}$ | Bus Hold Input Sustaining Current | $V_{CC}$ = 3V, $V_{IN}$ = 2.0V | –75 | — | — | µA |
| | | $V_{CC}$ = 3V, $V_{IN}$ = 0.8V | 75 | — | — | |
| $I_{OZ}$ | High-Z I/O Leakage | $V_O$ = 0V, $V_O$ = 5.5V,<br>$V_I$ = $V_{IH}$ or $V_{IL}$, $V_{CC}$ = 3.6V | — | — | ±1.0 | µA |
| $I_{OFF}$ | Power Off Leakage | $V_{CC}$ = 0V, $V_I$ or $V_O$ = 5.5V | — | — | 10 | µA |
| $I_{CC}$ | Quiescent Power Supply Current | $V_{CC}$ = 3.6V, $V_{IN}$ = $V_{CC}$ or GND | — | 0.1 | 10 | µA |
| $\Delta I_{CC}$ | Quiescent Power Supply Current per Control Inputs at TTL HIGH | $V_{CC}$ = 3.6V, $V_{IN}$ = $V_{CC}$ – 0.6V[5] | — | 2.0 | 3.0 | µA |
| | Quiescent Power Supply Current per Bus Hold Inputs at TTL HIGH | $V_{CC}$ = 3.6V, $V_{IN}$ = $V_{CC}$ – 0.6V[5] | — | 75 | 500 | µA |

**Notes**:
1. Typical values are at $V_{CC}$ = 3.3V and $T_A$ = 25°C.
2. These parameters are guaranteed by characterization, but not production tested.
3. Pins with Bus Hold are identified in the pin description.
4. An external driver must provide at least $|I_{BH}|$ during transition to guarantee that the Bus Hold input will change state.
5. Per TTL driven input. All other inputs at $V_{CC}$ or GND.

## Table 6. Dynamic Switching Characteristics

| Symbol | Parameter | Test Conditions | | Typ(1) | Unit |
|---|---|---|---|---|---|
| $V_{OLP}$ | Quiet Output Dynamic Peak $V_{OL}$ | $C_L$ = 50pF, $V_{CC}$ = 3.3V | $V_{IH}$ = 3.3V, $V_{IL}$ = 0V | 0.8 | V |
| $V_{OLV}$ | Quiet Output Dynamic Valley $V_{OL}$ | $C_L$ = 50pF, $V_{CC}$ = 3.3V | $V_{IH}$ = 3.3V, $V_{IL}$ = 0V | 0.8 | V |
| $C_{PD}$ | Power Dissipation | $C_L$ = 50pF, f = 10MHz, $V_{CC}$ = 3.3 ±0.3V | Output Enable | 20 | pF |
| | | | Output Disable | 4 | |

**Note:**
1. Typical values are at $V_{CC}$ = 3.3V, 25°C ambient.

## Table 7. Capacitance(1)

| Symbol | Pins | Conditions | Typ | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V, $V_{OUT}$ = 0V, f = 1MHz | 7.0 | pF |
| $C_{I/O}$ | I/O Capacitance | $V_{IN}$ = 0V, $V_{OUT}$ = 0V, f = 1MHz | 8.0 | pF |

**Note:**
1. Capacitance is characterized but not production tested.

## Table 8. Switching Characteristics Over Operating Range

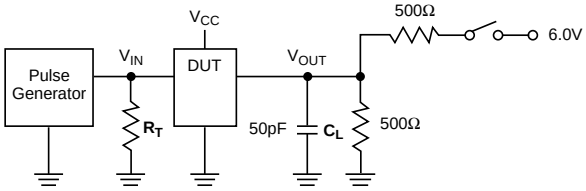
Industrial Temperature Range, $T_A$ = –40°C to 85°C.
$C_{LOAD}$ = 50pF, $R_{LOAD}$ = 500Ω unless otherwise noted.

| Symbol | Description(1) | $V_{CC}$ = 3.3 ±0.3V | | $V_{CC}$ = 2.7V(2) | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $t_{PD}$ | Propagation Delay xAi to xYi | 1.5 | 6.3 | 1.5 | 7.3 | ns |
| $t_{EN}$ | Output Enable Time x$\overline{G}$ to xYi | 1.5 | 8.5 | 1.5 | 9.5 | ns |
| $t_{DIS}$ | Output Disable Time(2) x$\overline{G}$ to xYi | 1.5 | 7.8 | 1.5 | 8.5 | ns |
| $t_{SK(O)}$ | Output Skew(3) | — | 0.5 | — | — | ns |

**Notes:**
1. Minimums guaranteed but not tested. See Test Circuit and Waveforms.
2. Guaranteed by characterization.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by characterization but not production tested.

## TEST CIRCUIT AND WAVEFORMS

### Figure 3. Test Circuit

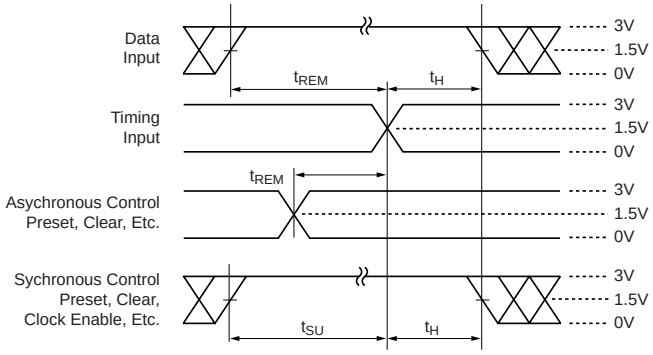



**SWITCH POSITION**

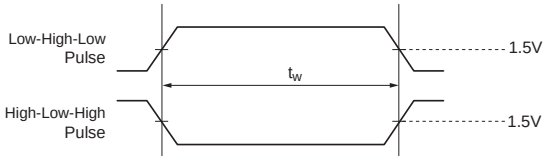
| Test | Switch |
|---|---|
| Open Drain<br>Disable LOW<br>Enable LOW | 6V |
| Disable HIGH<br>Enable HIGH | GND |
| All Other Inputs | Open |

DEFINITIONS:
$C_L$ = Load capacitance: includes jig and probe capacitance.
$R_T$ = Termination resistance: should be equal to $Z_{OUT}$ of the Pulse Generator.

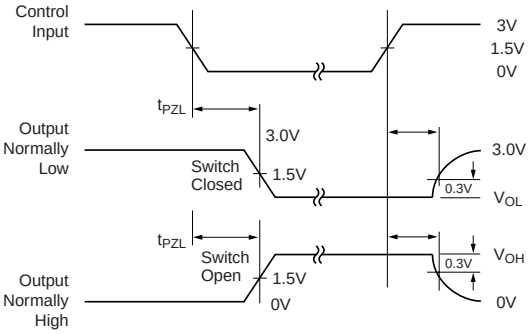
### Figure 4. Setup, Hold, and Release Timing



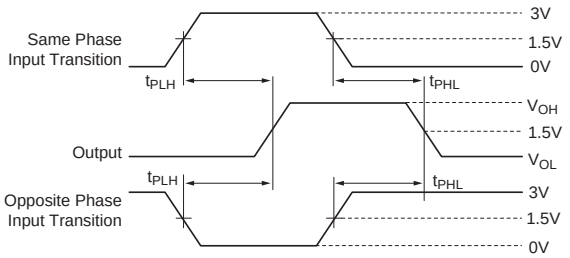

### Figure 6. Pulse Width




### Figure 5. Enable and Disable Timing

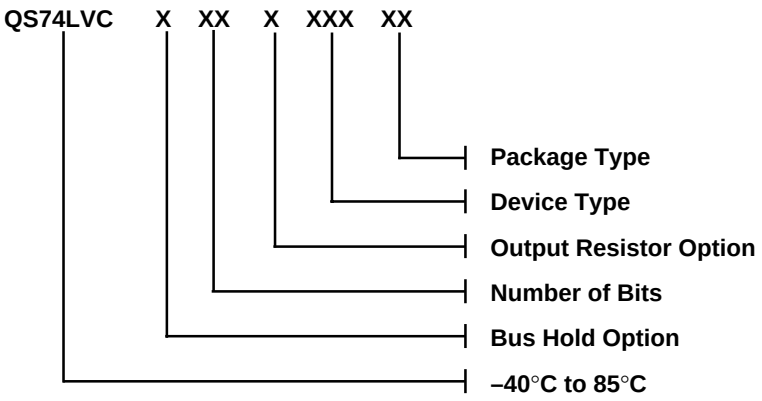



### Figure 7. Propagation Delay




Notes:
1. Input Control Enable = LOW and Input Control Disable = HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_{OUT} \leq 50\Omega$; $t_F$, $t_R \leq 2.5$ns.

## ORDERING INFORMATION




**Bus Hold Option:**
H – with Bus Hold

**Number of Bits:**
Blank – 8-Bit

**Output Resistor Option:**
Blank – No Output Resistor

**Device Type:**
245

**Package Type:**
Q – QSOP, 150 mil
SO – SOIC, 300 mil
PA – TSSOP, 170 mil