PIC16C65A → PIC16C65B Migration

DEVICE MIGRATIONS

This document is intended to describe the functional differences and the electrical specification differences that are present when migrating from one device to the next.

Note:	Even though compatible devices are specified to be tested to the same electrical specification, the characteristics of the devices may be different from each other (due to process difference). For systems that were designed to the device specifications, these process differences should not cause any issues in the application. For systems that did not tightly meet the electrical specifications, the process differences may cause the device to behave differently in the application.

Note:	While there are no functional or electrical changes to the device oscillator specifications, the user should verify that the device oscillator starts and performs as expected. Adjusting the loading capacitor values and/or the oscillator mode may be required.

Table 1 shows the considerations that must be taken into account when migrating from the PIC16C65A to the PIC16C65B.

TABLE 1: PIC16C65A → PIC16C65B DIFFERENCES

Functional Differences due to Errata or Module Update					
No.	**Module**	**Difference**	**H/W**	**S/W**	**Prog.**
1	CCP	CCP Special Event Trigger clears Timer1.	—	✔	—
2		Compare mode drives pin correctly.	—	✔	—
3	Timers	Reading or writing TMR1H or TMR1L may affect TMR1H or TMR1L unexpectedly.	—	✔	—
4		WDT/TMR0 prescaler assignment changes do not affect TMR0 count.	—	✔	—
5	SSP	TMR2 SPI™ clock synchronized to start of SPI Transmission.	—	✔	—
6		Can now transmit multiple words in SPI mode.	—	✔	—
7		Supports all four SPI modes. (Now uses SSP vs BSSP module.) See SSP module in the PICmicro™ Mid-Range MCU Family Reference Manual (DS33023A).	—	✔	—
8		I^2C™ no longer generates ACK pulses when module is enabled.	—	✔	—
9	USART	Async receive errors due to BRGH setting corrected.	—	✔	—
10	Oscillator	TOST delay may be skipped when waking from SLEEP.	—	✔	—
11	RESET	Short $\overline{\text{MCLR}}$ pulses may cause improper operation on the PIC16C65B.	✔	—	—
12		Operating voltage and frequency ranges have been redefined.	✔	—	—

H/W - Issues may exist with regard to the application circuits.
S/W - Issues may exist with regard to the user program.
Prog. - Issues may exist when writing the program to the controller.

TABLE 2: ELECTRICAL SPECIFICATION DIFFERENCES

Param No.	Symbol	Characteristic		PIC16C65A			PIC16C65B			Unit
				Min	Typ†	Max	Min	Typ†	Max	
Core										
	VDD	Supply Voltage								
D001		XT, LP and RC mode		4.0	—	6.0	4.0	—	**5.5**	V
D001A		HS mode		4.5	—	5.5	**4.0**	—	5.5	V
		BOR enabled **(Note 1)**		—	—	—	**VBOR**	—	**5.5**	V
D005	VBOR	Brown-out Reset Voltage		3.7	4.0	4.3	**3.65**	—	**4.35**	V
D150	VOD	Open-Drain High Voltage on RA4		—	—	14.0	—	—	**8.5**	V
SSP in SPI mode										
71	TscH	SCK input high time (slave mode)	Continuous	TCY+20	—	—	**1.25TCY + 30**	—	—	ns
71A			Single Byte				**40**	—	—	ns
72	TscL	SCK input low time (slave mode)	Continuous	TCY+20	—	—	**1.25TCY + 30**	—	—	ns
72A			Single Byte				**40**	—	—	ns
73	TdiV2scH TdiV2scL	Setup time of SDI data input to SCK edge		50	—	—	**100**	—	—	ns
73A **(Note 2)**	TB2B	Last clock edge of Byte1 to the 1st clock edge of Byte2		—	—	—	**1.5TCY + 40**	—	—	ns
74	TscH2diL TscL2diL	Hold time of SDI data input to SCK edge		50	—	—	**100**	—	—	ns
75	TdoR	SDO data output rise time	PIC16CXX	—	10	25	—	10	25	ns
			PIC16LCXX				—	**20**	**45**	ns
78	TscR	SCK output rise time (master mode)	PIC16CXX	—	10	25	—	10	25	ns
			PIC16LCXX				—	**20**	**45**	ns
80	TscH2doV TscL2doV	SDO data output valid after SCK edge	PIC16CXX	—	—	50	—	—	50	ns
			PIC16LCXX				—	—	**100**	ns
83	TscH2ssH TscL2ssH	$\overline{SS}$ ↑ after SCK edge		—	—	—	**1.5TCY + 40**	—	—	ns

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When BOR is enabled, the device will operate until VDD drops below VBOR.

2: Specification 73A is only required if specifications 71A and 72A are used.

NOTES:

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