PIC16C717/770/771

Programming Specifications for PIC16C717/770/771 OTP MCUs

This document includes the programming specifications for the following devices:

- PIC16C717
- PIC16C770
- PIC16C771

1.0 PROGRAMMING THE PIC16C717/770/771

The PIC16C717/770/771 can be programmed using a serial method. In serial mode, the PIC16C717/770/771 can be programmed while in the users system. This allows for increased design flexibility. This programming specification applies to PIC16C717/770/771 devices in all packages.

1.1 Hardware Requirements

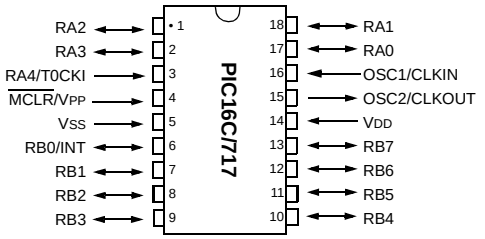
The PIC16C717/770/771 requires two programmable power supplies, one for VDD (2.5V to 6.5V recommended) and one for VPP (12V to 14V). Both supplies should have a minimum resolution of 0.25V.

1.2 Programming Mode

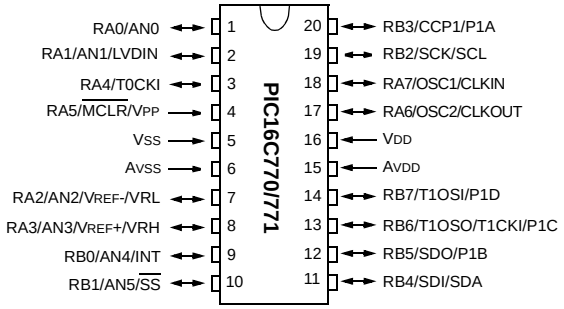
The programming mode for the PIC16C717/770/771 allows programming of user program memory, special locations used for ID, and the configuration word for the PIC16C717/770/771.

Pin Diagrams

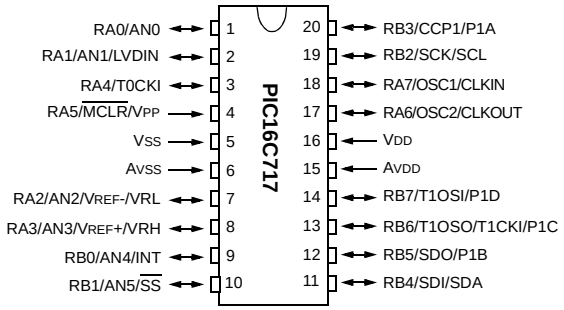
18-Pin PDIP, SOIC, Windowed CERDIP



20-Pin PDIP, SOIC, SSOP, Windowed CERDIP



20-Pin SSOP



2.0 PROGRAM MODE ENTRY

2.1 User Program Memory Map

The user memory space extends from 0x0000 to 0x1FFF (8K). Table 2-1 shows actual implementation of program memory in the PIC16C717/770/771 family.

TABLE 2-1: IMPLEMENTATION OF PROGRAM MEMORY IN THE PIC16C717/770/771

Device	Program Memory Size
PIC16C717	0x000 – 0x7FF (2K)
PIC16C770	0x000 – 0x7FF (2K)
PIC16C771	0x000 – 0xFFF (4K)

When the PC reaches the last location of the implemented program memory, it will wrap around and address a location within the physically implemented memory (see Figure 2-1).

In programming mode, the program memory space extends from 0x0000 to 0x3FFF, with the first half (0x0000-0x1FFF) being user program memory and the second half (0x2000-0x3FFF) being configuration memory. The PC will increment from 0x0000 to 0x1FFF and wrap to 0x000, or 0x2000 to 0x3FFF and wrap around to 0x2000 (not to 0x0000). Once in configuration memory, the highest bit of the PC stays a '1', thus always pointing to the configuration memory. The only way to point to user program memory is to reset the part and reenter program/verify mode, as described in Section 2.2.

In the configuration memory space, 0x2000-0x207F or 0x2000-0x20FF are utilized. When in a configuration memory, as in the user memory, the 0x2000-0x2XFF segment is repeatedly accessed as PC exceeds 0x2XFF (Figure 2-1).

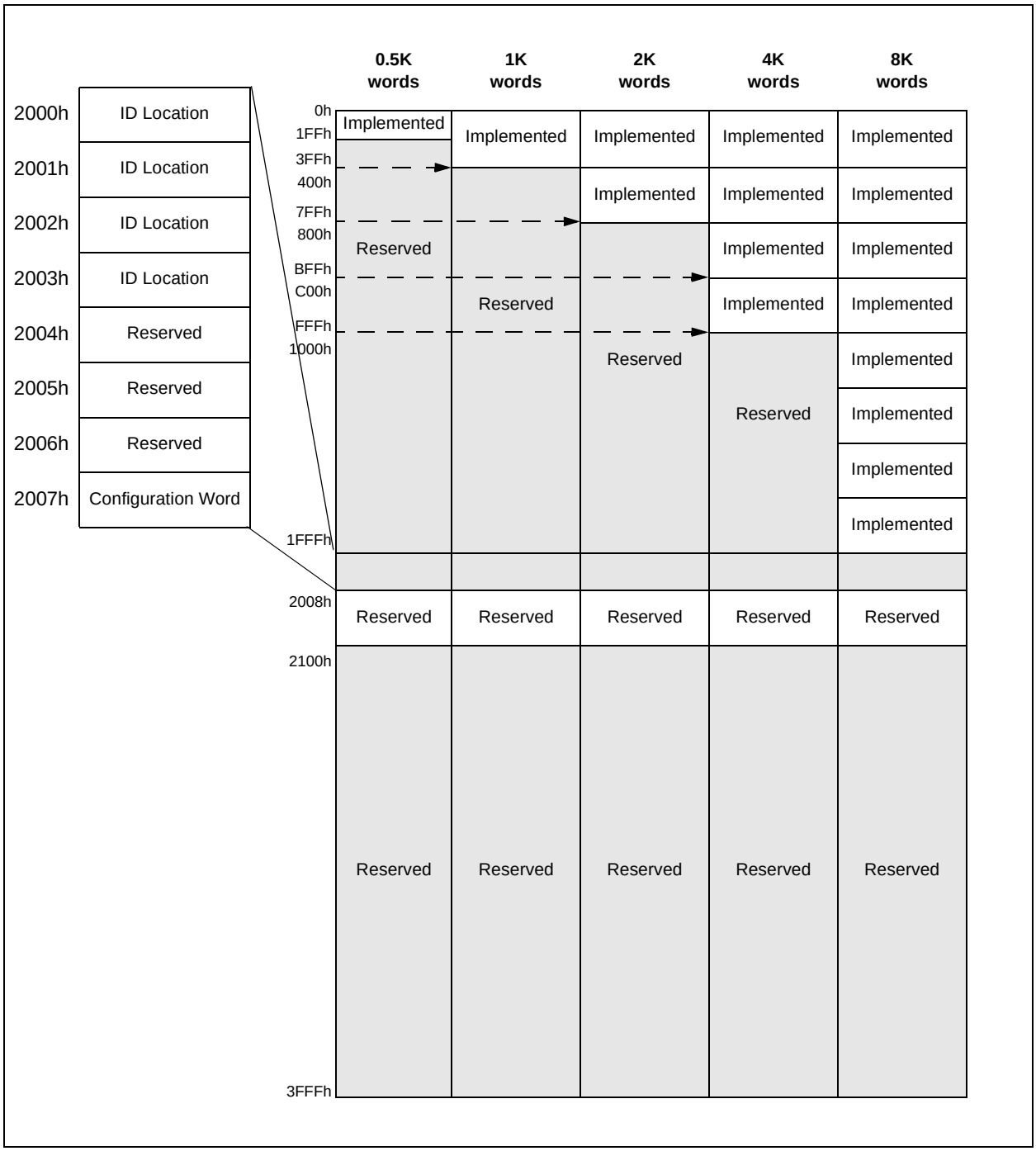
A user may store identification information (ID) in four ID locations. The ID locations are mapped in [0x2000: 0x2003]. It is recommended that the user use only the four least significant bits of each ID location. In some devices, the ID locations read out in a scrambled fashion after code protection is enabled. For these devices, it is recommended that ID location is written as "`11 1111 1bbb bbbb`" where '`bbbb`' is ID information.

Note: All other locations are reserved and should not be programmed.

In other devices, the ID locations read out normally, even after code protection. To understand how the devices behave, refer to Table 4-1.

To understand the scrambling mechanism after code protection, refer to Section 3.1.

FIGURE 2-1: PROGRAM MEMORY MAPPING



2.2 Program/Verify Mode

The program/verify mode is entered by holding pins RB6 and RB7 low while raising MCLR pin from VSS to the appropriate VIHH (high voltage). VDD is then raised from VSS to the appropriate VDD level. Once in this mode, the user program memory and the configuration memory can be accessed and programmed in serial fashion. The mode of operation is serial, and the memory that is accessed is the user program memory. RB6 is a Schmitt Trigger input in this mode.

The sequence that enters the device into the programming/verify mode, places all other logic into the RESET state (the MCLR pin was initially at VSS). This means that all I/O are in the RESET state (high impedance inputs).

Note 1: The MCLR pin should be raised as quickly as possible from VIL to VIHH. This is to ensure that the device does not have the PC incremented while in valid operation range.

2: The MCLR pin must be raised from VIL to VIHH before VDD is applied. This is to ensure that the device does not have the PC incremented while in valid operation range

3: Do not power any pin before VDD is applied.

2.2.1 PROGRAM/VERIFY OPERATION

The RB6 pin is used as a clock input pin, and the RB7 pin is used for entering command bits and data input/output during serial operation. To input a command, the clock pin (RB6) is cycled six times. Each command bit is latched on the falling edge of the clock with the least significant bit (LSb) of the command being input first. The data on pin RB7 is required to have a minimum setup and hold time (see AC/DC specs), with respect to the falling edge of the clock. Commands that have data associated with them (read and load) are specified to have a minimum delay of 1 µs between the command and the data. After this delay, the clock pin is cycled 16 times with the first cycle being a Start bit and the last cycle being a Stop bit. Data is also input and output LSb first. Therefore, during a read operation the LSb will be transmitted onto pin RB7 on the rising edge of the second cycle, and during a load operation the LSb will be latched on the falling edge of the second cycle. A minimum 1 µs delay is also specified between consecutive commands.

All commands are transmitted LSb first. Data words are also transmitted LSb first. The data is transmitted on the rising edge and latched on the falling edge of the clock. To allow for decoding of commands and reversal of data pin configuration, a time separation of at least 1 µs is required between a command and a data word (or another command).

The commands that are available are listed in Table 2-2.

2.2.1.1 Load Configuration

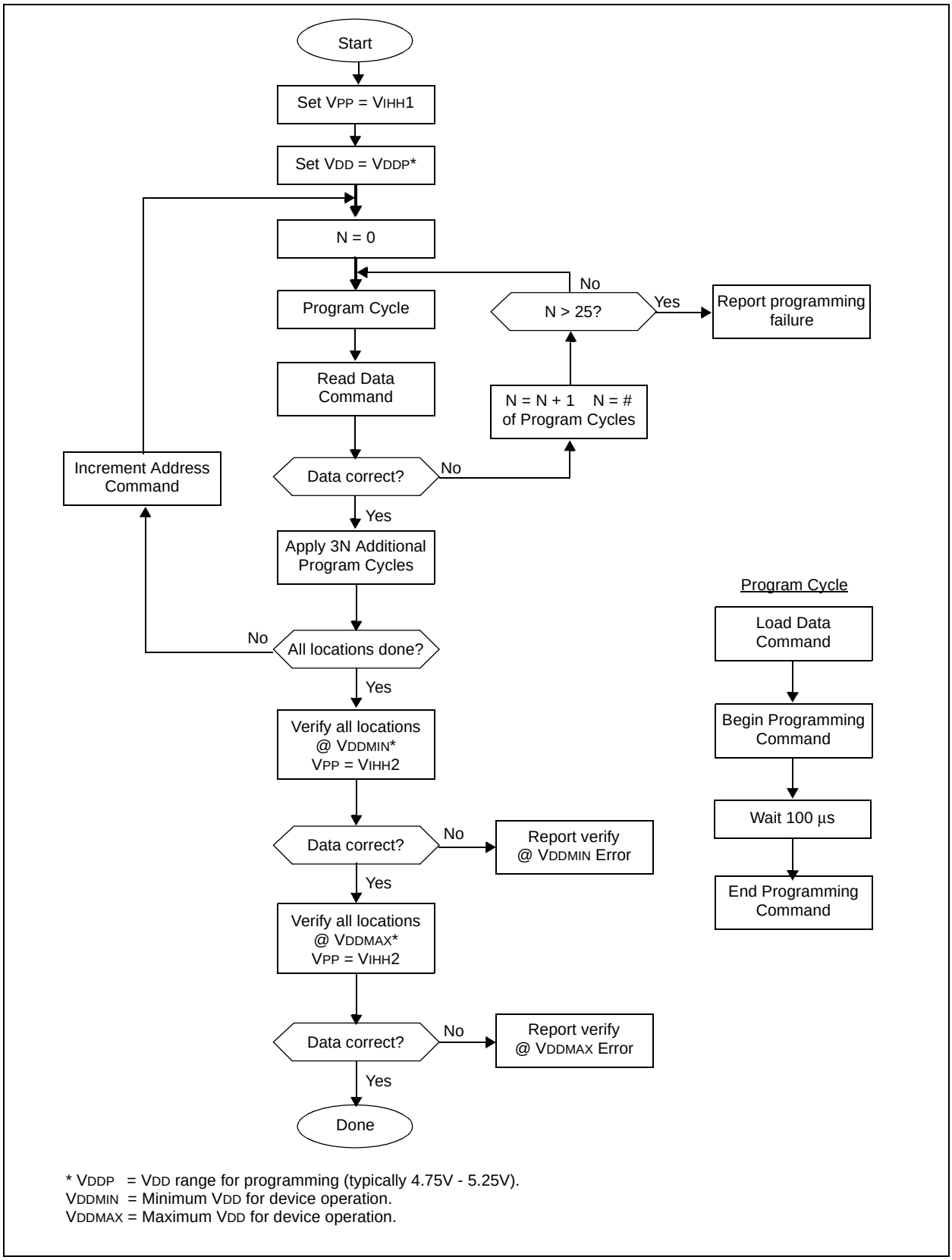
After receiving this command, the program counter (PC) will be set to 0x2000. By then applying 16 cycles to the clock pin, the chip will load 14-bits in a “data word” as described above, to be programmed into the configuration memory. A description of the memory mapping schemes for normal operation and configuration mode operation is shown in Figure 2-1. After the configuration memory is entered, the only way to get back to the user program memory is to exit the program/verify test mode by taking MCLR low (VIL).

TABLE 2-2: COMMAND MAPPING

Command	Mapping (MSb... LSb)						Data
Load Configuration	0	0	0	0	0	0	0, data(14), 0
Load Data	0	0	0	0	1	0	0, data(14), 0
Read Data	0	0	0	1	0	0	0, data(14), 0
Increment Address	0	0	0	1	1	0	
Begin programming	0	0	1	0	0	0	
End Programming	0	0	1	1	1	0	

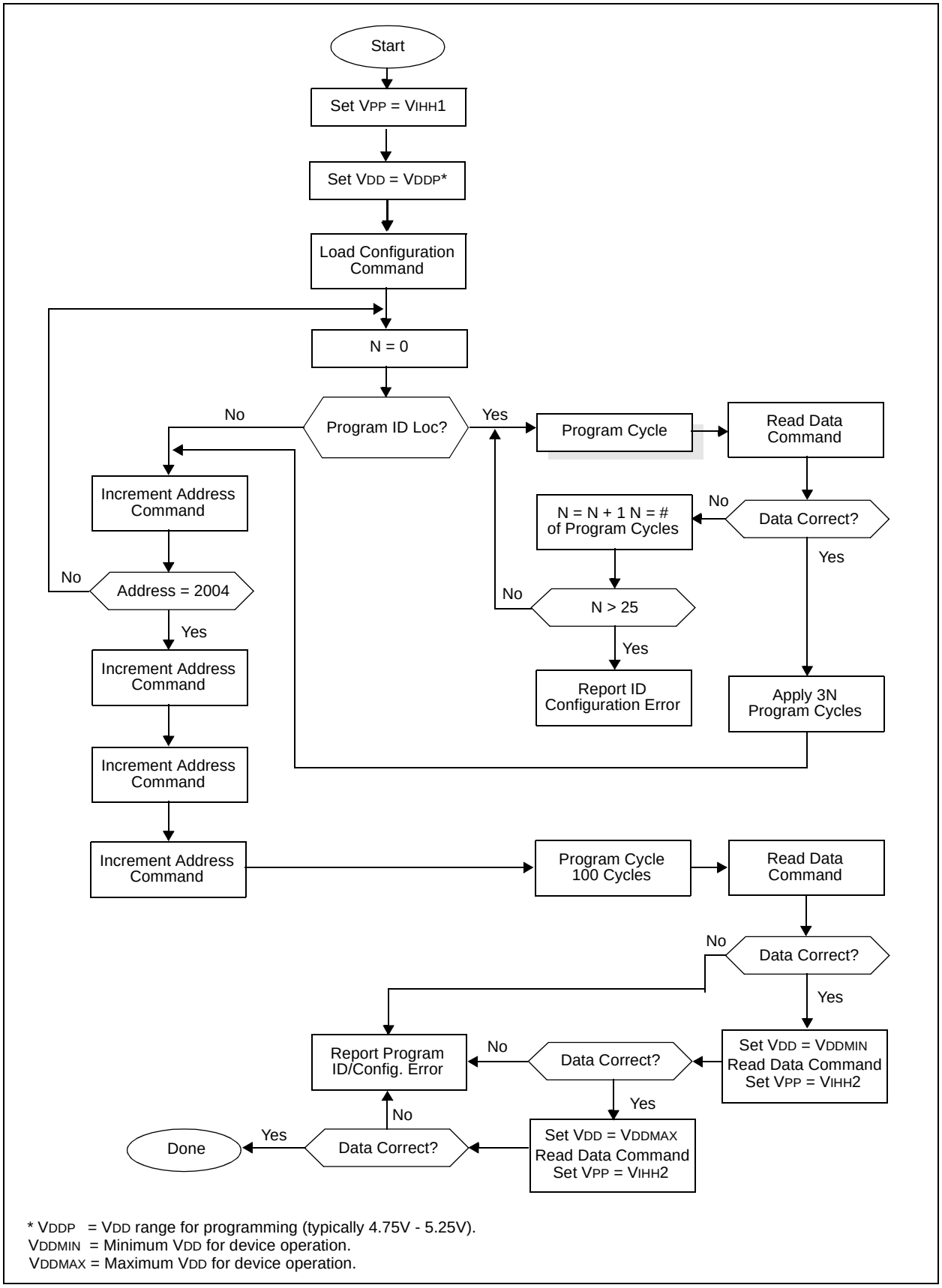
Note: The clock must be disabled during In-Circuit Serial Programming™.

FIGURE 2-2: PROGRAM FLOW CHART - PIC16C717/770/771 PROGRAM MEMORY



* VDDP = VDD range for programming (typically 4.75V - 5.25V).
VDDMIN = Minimum VDD for device operation.
VDDMAX = Maximum VDD for device operation.

FIGURE 2-3: PROGRAM FLOW CHART - PIC16C717/770/771 CONFIGURATION WORD & ID LOCATIONS



* VDDP = VDD range for programming (typically 4.75V - 5.25V).
VDDMIN = Minimum VDD for device operation.
VDDMAX = Maximum VDD for device operation.

2.2.1.2 Load Data

After receiving this command, the chip will load in a 14-bit “data word” when 16 cycles are applied, as described previously. A timing diagram for the load data command is shown in Figure 4-1.

2.2.1.3 Read Data

After receiving this command, the chip will transmit data bits out of the memory currently accessed starting with the second rising edge of the clock input. The RB7 pin will go into output mode on the second rising clock edge, and it will revert back to input mode (hi-impedance) after the 16th rising edge. A timing diagram of this command is shown in Figure 4-2.

2.2.1.4 Increment Address

The PC is incremented when this command is received. A timing diagram of this command is shown in Figure 4-3.

2.2.1.5 Begin Programming

A load command (load configuration or load data) must be given before every begin programming command. Programming of the appropriate memory (test program memory or user program memory) will begin after this command is received and decoded. Programming should be performed with a series of 100µs programming pulses. A programming pulse is defined as the time between the begin programming command and the end programming command.

2.2.1.6 End Programming

After receiving this command, the chip stops programming the memory (configuration program memory or user program memory) that it was programming at the time.

2.3 Programming Algorithm Requires Variable VDD

The PIC16C717/770/771 uses an intelligent algorithm. The algorithm calls for program verification at VDDMIN as well as VDDMAX. Verification at VDDMIN guarantees good “erase margin”. Verification at VDDMAX guarantees good “program margin.”

The actual programming must be done with VDD in the VDDP range (4.75 - 5.25V).

VDDP = VDD range required during programming.

VDDMIN = minimum operating VDD spec for the part.

VDDMAX = maximum operating VDD spec for the part.

Programmers must verify the PIC16C717/770/771 at its specified VDDMAX and VDDMIN levels. Since Microchip may introduce future versions of the PIC16C717/770/771 with a broader VDD range, it is best that these levels are user selectable (defaults are ok).

Note:	Any programmer not meeting these requirements may only be classified as “prototype” or “development” programmer, but not a “production” quality programmer.

3.0 CONFIGURATION WORD

The PIC16C717/770/771 family members have several configuration bits. These bits can be programmed (reads '0'), or left unprogrammed (reads '1'), to select various device configurations. Figure 3-1 provides an overview of configuration bits.

FIGURE 3-1: CONFIGURATION WORD FOR PIC16C717/770/771 DEVICE

$\overline{CP}$	$\overline{CP}$	BORV1	BORV0	$\overline{CP}$	$\overline{CP}$	-	BODEN	MCLRE	$\overline{PWRTE}$	WDTE	FOSC2	FOSC1	FOSC0
bit13	12	11	10	9	8	7	6	5	4	3	2	1	bit0

Register: CONFIG
Address 2007h

bit 13,12: **$\overline{CP}$:** Program Memory Code Protection
bit 9,8: 1 = Code protection off
0 = All program memory is protected(2)

bit 11-10: **BORV<1:0>**: Brown-out Reset Voltage bits
00 = VBOR set to 4.5V
01 = VBOR set to 4.2V
10 = VBOR set to 2.7V
11 = VBOR set to 2.5V

bit 7: **Unimplemented:** Read as '1'

bit 6: **BODEN**: Brown-out Detect Reset Enable bit(1)
1 = Brown-out Detect Reset enabled
0 = Brown-out Detect Reset disabled

bit 5: **MCLRE**: RA5/$\overline{MCLR}$ Pin Function Select
1 = RA5/$\overline{MCLR}$ pin function is $\overline{MCLR}$
0 = RA5/$\overline{MCLR}$ pin function is digital input, $\overline{MCLR}$ internally tied to VDD

bit 4: **$\overline{PWRTE}$**: Power-up Timer Enable bit(1)
1 = PWRT disabled
0 = PWRT enabled

bit 3: **WDTE**: Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 2-0: **FOSC<2:0>**: Oscillator Selection bits(3)
000 = LP oscillator: Ceramic resonator on RA6/OSC2/CLKOUT and RA7/OSC1/CLKIN
001 = XT oscillator: Crystal on RA6/OSC2/CLKOUT and RA7/OSC1/CLKIN
010 = HS oscillator: High frequency crystal on RA6/OSC2/CLKOUT and RA7/OSC1/CLKIN
011 = EC: I/O function on RA6/OSC2/CLKOUT pin, CLKIN function on RA7/OSC1/CLKIN
100 = INTRC oscillator: I/O function on RA6/OSC2/CLKOUT pin, I/O function on RA7/OSC1/CLKIN
101 = INTRC oscillator: CLKOUT function on RA6/OSC2/CLKOUT pin, I/O function on RA7/OSC1/CLKIN
110 = ER oscillator: I/O function on RA6/OSC2/CLKOUT pin, Resistor on RA7/OSC1/CLKIN
111 = ER oscillator: CLKOUT function on RA6/OSC2/CLKOUT pin, Resistor on RA7/OSC1/CLKIN

Note 1: Enabling Brown-out Reset automatically enables the Power-up Timer (PWRT) regardless of the value of bit $\overline{PWRTE}$. Ensure the Power-up Timer is enabled any time Brown-out Reset is enabled.
2: All of the CP bits must be given the same value to enable code protection.
3: When the internal oscillator is selected (INTRC or ER), and the part is in RESET, the oscillator is disabled and CLKOUT is held low.

3.1 Embedding Configuration Word and ID Information in the Hex File.

To allow portability of code, the programmer is required to read the configuration word and ID locations from the hex file when loading the hex file. If configuration word information was not present in the hex file, then a simple warning message may be issued. Similarly, while saving a hex file, configuration word and ID information must be included. An option to not include this information may be provided.

Microchip Technology Inc. feels strongly that this feature is beneficial to the end customer.

3.2 Checksum

3.2.1 CHECKSUM CALCULATIONS

Checksum is calculated by reading the contents of the PIC16C717/770/771 memory locations and adding up the opcodes up to the maximum user addressable location, e.g., 0-0xFFF for the PIC16C771. Any carry bits exceeding 16-bits are neglected. Finally, the configuration word (appropriately masked) is added to the checksum. Checksum computation for each member of the PIC16C717/770/771 devices is shown in Table 3-1.

The checksum is calculated by summing the following:

- The contents of all program memory locations
- The configuration word, appropriately masked
- Masked ID locations (when applicable)

The least significant 16 bits of this sum is the checksum.

The following table describes how to calculate the checksum for each device. Note that the checksum calculation differs depending on the code protect setting. Since the program memory locations read out differently depending on the code protect setting, the table describes how to manipulate the actual program memory values to simulate the values that would be read from a protected device. When calculating a checksum by reading a device, the entire program memory can simply be read and summed. The configuration word and ID locations can always be read.

Note that some older devices have an additional value added in the checksum. This is to maintain compatibility with older device programmer checksums.

TABLE 3-1: CHECKSUM COMPUTATION

Device	Code Protect	Checksum*	Blank Value	0x25E6 at 0 and max address
PIC16C717	OFF ALL	SUM[0x000:0x07FF] + CFGW & 0x3F7F CFGW & 0x3F7F + SUM_ID	0x377F 0x43FE	0x034D 0x0FCC
PIC16C770	OFF ALL	SUM[0x000:0x07FF] + CFGW & 0x3F7F CFGW & 0x3F7F + SUM_ID	0x377F 0x43FE	0x034D 0x0FCC
PIC16C771	OFF ALL	SUM[0x000:0x0FFF] + CFGW & 0x3F7F CFGW & 0x3F7F + SUM_ID	0x2F7F 0x3BFE	0xFB4D 0x07CC

Legend: CFGW = Configuration Word
SUM[a:b] = [Sum of locations a through b inclusive]
SUM_XNOR7[a:b] = XNOR of the seven high order bits of memory location with the seven low order bits summed over locations a through b inclusive. For example, XNOR(0x3C31)=0x78 XNOR 0c31 = 0x0036.
SUM_ID = ID locations masked by 0xF then made into a 16-bit value with ID0 as the most significant nibble. For example, ID0 = 0x12, ID1 = 0x37, ID2 = 0x4, ID3 = 0x26, then SUM_ID = 0x2746.
*Checksum = [Sum of all the individual expressions] **MODULO** [0xFFFF]
+ = Addition
& = Bitwise AND
| = Bitwise OR

4.0 PROGRAM/VERIFY MODE

TABLE 4-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY TEST MODE

Standard Operating Conditions Operating Temperature: +10°C ≤ TA ≤ +40°C, unless otherwise stated, (20°C recommended) Operating Voltage: 4.5V ≤ VDD ≤ 5.5V, unless otherwise stated.							
Parameter No.	**Sym.**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
		General					
PD1	VDDP	Supply voltage during programming	4.75	5.0	5.25	V	
PD2	IDDP	Supply current (from VDD) during programming	–	–	20	mA	
PD3	VDDV	Supply voltage during verify	VDDMIN	–	VDDMAX	V	Note 1
PD4	VIHH1	Voltage on $\overline{MCLR}$/VPP during programming	12.75	–	13.25	V	Note 2
PD5	VIHH2	Voltage on $\overline{MCLR}$/VPP during verify	VDD + 4.0	–	13.25	–	
PD6	IPP	Programming supply current (from VPP)	–	–	50	mA	
PD9	VIH	(RB6, RB7) input high level	0.8 VDD	–	–	V	Schmitt Trigger input
PD8	VIL	(RB6, RB7) input low level	0.2 VDD	–	–	V	Schmitt Trigger input
		Serial Program Verify					
P1	TR	$\overline{MCLR}$/VPP rise time (VSS to VHH) for test mode entry	–	–	8.0	µs	
P2	Tf	$\overline{MCLR}$ fall time	–	–	8.0	µs	
P3	Tset1	Data in setup time before clock ↓	100	–	–	ns	
P4	Thld1	Data in hold time after clock ↓	100	–	–	ns	
P5	Tdly1	Data input not driven to next clock input (delay required between command/data or command/command)	1.0	–	–	µs	
P6	Tdly2	Delay between clock ↓ to clock ↑ of next command or data	1.0	–	–	µs	
P7	Tdly3	Clock ↑ to date out valid (during read data)	200	–	–	ns	
P8	Thld0	Hold time after $\overline{MCLR}$ ↑	2	–	–	µs	
P9	TPPDP	Hold time after VPP↑	5			µs	

Note 1: Program must be verified at the minimum and maximum VDD limits for the part.

2: VIHH must be greater than VDD + 4.5V to stay in programming/verify mode.

FIGURE 4-1: LOAD DATA COMMAND (PROGRAM/VERIFY)

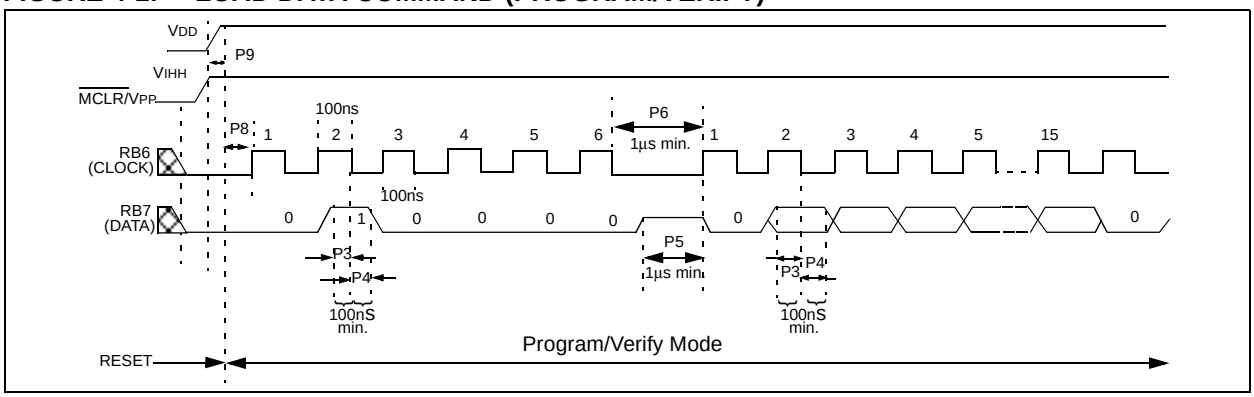


FIGURE 4-2: READ DATA COMMAND (PROGRAM/VERIFY)

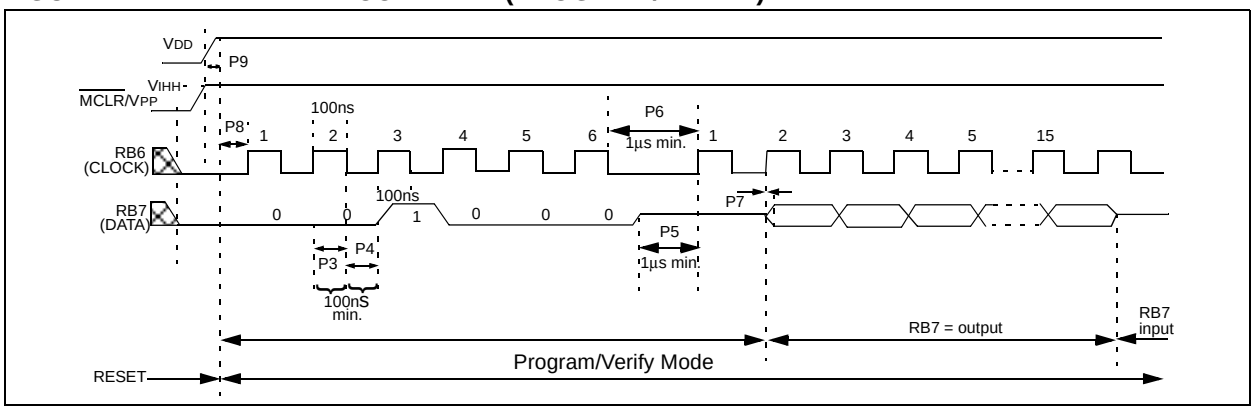
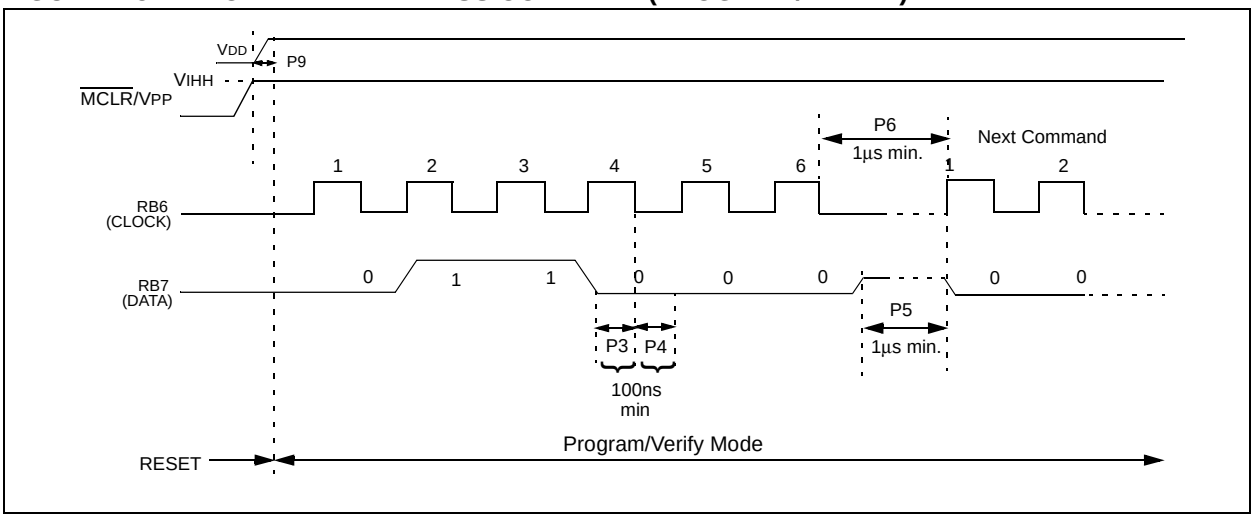


FIGURE 4-3: INCREMENT ADDRESS COMMAND (PROGRAM/VERIFY)



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