32/64-Channel Infinite Sample-and-Hold

Preliminary Technical Data

AD5532/64

FEATURES

- **Infinite Hold Capability with No Droop**
- **Single Input, 32/64 Output Channels**
- **Input/Output Transfer Function Nonlinearity of ±0.012% max**
- **Per-Channel Acquisition time of 16 µs max**
- **Input Voltage: 0 to +3V**
- **Output Voltage Span: +10V**
  - **e.g. -3V to +7V**
  - **-2.5V to +7.5V**

APPLICATIONS

- **Level Setting**
- **Instrumentation**
- **Automatic Test Equipment**
- **Control Systems**
- **Data Acquisition**
- **Low Cost I/O**

GENERAL DESCRIPTION

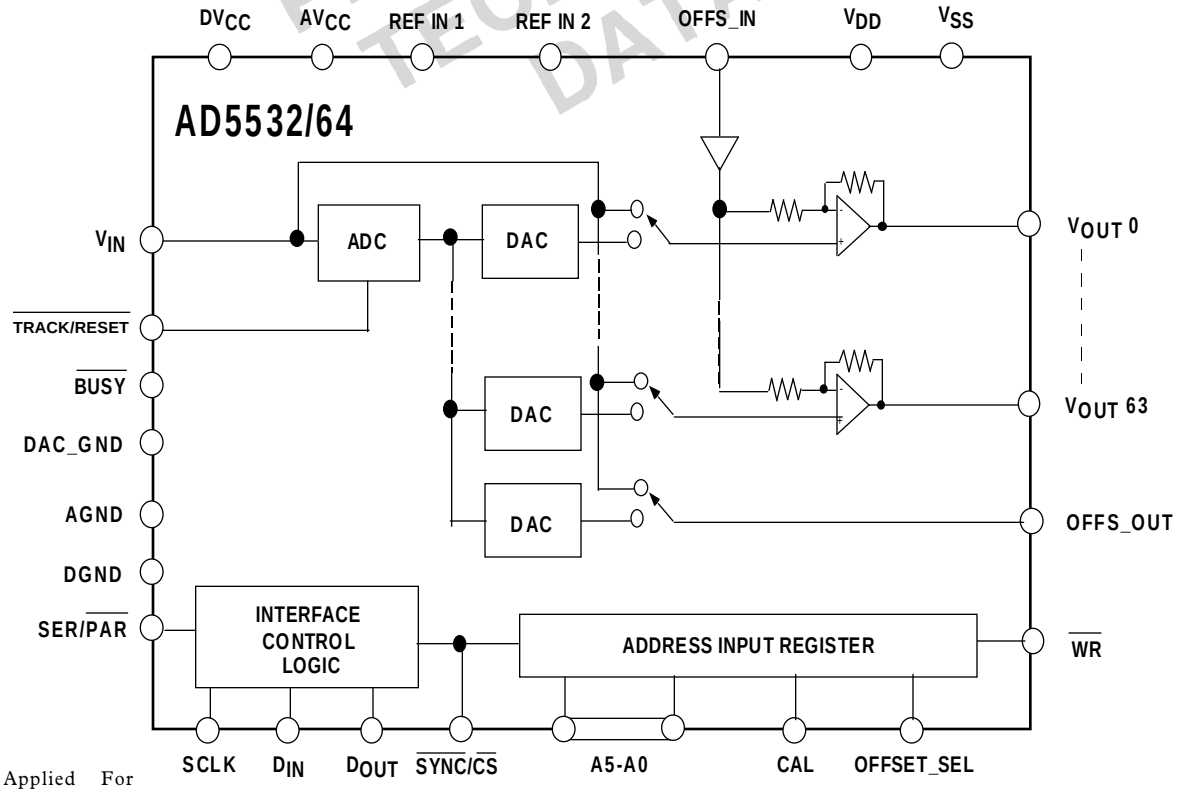
The AD5532/64 combines a 32/64 channel voltage translation function with an infinite output hold capability. An analog input voltage on the common input pin, V_{IN}, is sampled and its digital representation transferred to a chosen DAC register. The output of this DAC is updated to reflect the new contents of the DAC register. Channel selection is accomplished via the parallel address inputs A0-A5 or via the serial input port.

The device is operated with AVcc = +5V±5%, DVcc= 2.7V to 5.5V, Vss = -4.75V to -16.5V and V_{DD}= 8V to 16.5V and requires a stable +3V reference on REF IN pins as well as an offset voltage on OFFS_IN. The output voltage range is determined by the headroom of the output amplifier and is restricted to a range from Vss+2.2V to V_{DD}-2V. The AD5564 is available in a 119-lead BGA package.

PRODUCT HIGHLIGHTS

1. No Droop; Infinite Hold Capability
2. Typically ±0.006% transfer function nonlinearity between Input and Output.
3. 32/64 14-bit DACs in one package, guaranteed monotonic with 9-bit linearity.
4. The AD5564 is available in a 119-lead BGA package with a bump pitch of 1.27mm and a body size of 14mm by 22mm.

FUNCTIONAL BLOCK DIAGRAM



Patents Applied For

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REV. PrE

AD5532/64-SPECIFICATIONS

V_{DD} = +8V to +16.5V, V_{SS} = -4.75V to -16.5V; AV_{CC} = +4.75V to +5.25V; DV_{CC} = +2.7V to +5.25V; AGND = DGND = DAC_GND = 0V; Output Range from Vss+2.2V to V_{DD} -2V. All specifications T_{MIN} to T_{MAX} unless otherwise noted.

Mode 1 - SHA Mode

Parameter[1]	B Version[2]	Units	Conditions/Comments
ANALOG CHANNEL			
V_{IN} to V_{OUT} Nonlinearity	± 0.012	% max	Typically ±0.006% (after gain and offset adjustment)
Offset Error	± 60	mV max	See Figure 1 (page 8)
Gain Error	± 100	mV max	See Figure 1 (page 8)
Channel-to-Channel Matching	TBD	% typ	
ANALOG INPUT (V_{IN})			
Input Voltage Range	0 to +3	V	Nominal Input Range
Input Current	100	nA max	V_{IN} being acquired on one channel
	6.4	µA max	V_{IN} being acquired on all 64 channels simultaneously - Cal Mode
Input Capacitance	50	pF typ	
ANALOG INPUT (OFFS_IN)			
Input Current	100	nA max	
REFERENCE INPUTS			
Nominal Input Voltage	+3.0	V	
Input Voltage Range	+2.85/+3.15	V min/max	
Input Current	50	nA max	
ANALOG OUTPUTS (V_{OUT} 0-63)			
Output Temp Coeff	10	ppm/°C typ	AD780 as reference for the AD5532/64
Output Impedance	1	kΩ typ	
Output Range	V_{SS} +2.2 /V_{DD} - 2	V min/max	100µA load on the output
Maximum Output Current	500	µA typ	
Maximum Capacitive Load	15	nF max	
Output Noise	250	µV rms	1MHz Bandwidth
Short-Circuit Current	10	mA typ	
Output PSRR	-70	dB	V_{DD} varied ±5%.
	-70	dB	V_{SS} varied ±5%
DC Crosstalk	250	µV max	
ANALOG OUTPUT (OFFS_OUT)			
Output Temp Coeff	10	ppm/°C typ	AD780 as reference for the AD5532/64
Output Impedance	1.0	kΩ typ	
Output Range	0 / +REF IN	V min/max	
Output Noise	100	µV rms	1MHz Bandwidth
Maximum Output Current	10	µA typ	Source Current
Maximum Capacitive Load	100	pF typ	
Short-Circuit Current	10	mA typ	Sink Current
Output PSRR	-70	dB typ	AV_{CC} varied ±5%
DIGITAL INPUTS			
Input Current	±10	µA max	
Input Low Voltage	0.8	V max	DV_{CC} = 5V±5%
	0.4	V max	DV_{CC} = 3V±10%
Input High Voltage	2.0	V min	
Input Hysteresis (SCLK only)	200	mV typ	
Input Capacitance	10	pF max	

NOTES:
[1]See Terminology
[2]B Version: Industrial temperature range -40°C. to +85°C.
[3]Guaranteed by design and characterisation, not production tested

AD5532/64-SPECIFICATIONS

V_{DD} = +8V to +16.5V, V_{SS} = -4.75V to -16.5V; AV_{CC} = +4.75V to +5.25V; DV_{CC} = +2.7V to +5.25V; AGND = DGND = DAC_GND = 0V; Output Range from Vss+2.2V to V_{DD} -2V. All specifications T_{MIN} to T_{MAX} unless otherwise noted.

Mode 1 - SHA Mode (cont.)

Parameter[1]	B Version[2]	Units	Conditions/Comments
DIGITAL OUTPUTS ($\overline{BUSY}$, D_{OUT})			
Output Low Voltage	0.4	V max	DV_{CC} = 5V. Sinking TBD mA
Output High Voltage	4.0	V min	DV_{CC} = 5V. Sourcing TBD µA
Output Low Voltage	0.4	V max	DV_{CC} = 3V. Sinking TBD mA
Output High Voltage	2.4	V min	DV_{CC} = 3V. Sourcing TBD µA
Floating-State Leakage Current[4]	TBD	µA max	
Floating-State Input Capacitance[4]	TBD	pF max	
POWER REQUIREMENTS			
Power-Supply Voltages			
V_{DD}	+8/+16.5	V min/max	
V_{SS}	-4.75/-16.5	V min/max	
AV_{CC}	+4.75/+5.25	V min/max	
DV_{CC}	+2.7/+5.25	V min/max	
Power-Supply Currents[5]			
I_{DD}	22	mA typ	
I_{SS}	22	mA typ	
AI_{CC}	54	mA typ	
DI_{CC}	< 1	mA max	
Power Dissipation[5]	600	mW typ	V_{DD}=10V, V_{SS}=-5V
AC CHARACTERISTICS			
AC Crosstalk	2.5	nV-s max	
Output Settling Time	3	µs max	100pF Capacitive load
Acquisition Time	16	µs max	Acquire V_{IN} to ± 0.012% accuracy
Slew Rate	1	V/µs typ	
Digital Feedthrough	2.5	nV-s typ	
Digital Crosstalk	2.5	nV-s typ	
$\overline{TRACK}$ MODE			
Output PSRR	TBD	dB	V_{DD} varied ±5%.
	TBD	dB	V_{SS} varied ±5%
Bandwidth	TBD	kHz typ	

NOTES:
[1]See Terminology
[2]B Version: Industrial temperature range -40°C. to +85°C.
[3]Guaranteed by design and characterisation, not production tested
[4]D_{OUT} only
[5]Outputs Unloaded. All figures are for the AD5564. The numbers for AD5532 are approx 50% of these.
Specifications subject to change without notice

AD5532/64-SPECIFICATIONS

V_{DD} = +8V to +16.5V, V_{SS} = -4.75V to -16.5V; AV_{CC} = +4.75V to +5.25V; DV_{CC} = +2.7V to +5.25V; AGND = DGND = DAC_GND = 0V; Output Range from Vss+2.2V to V_{DD} -2V. All specifications T_{MIN} to T_{MAX} unless otherwise noted.

Mode 2 - DAC Mode

Parameter[1]	B Version[2]	Units	Conditions/Comments
DC PERFORMANCE			
Resolution	14	Bits	
Integral Nonlinearity (INL)	TBD	% of FSR typ	
Differential Nonlinearity (DNL)	±1	LSB max	Guaranteed Monotonic
Offset Error	TBD	mV max	
Gain Error	TBD	% max	
Full-Scale Error	TBD	mV max	
Offset Error Temp Coeff	TBD	µV/°C typ	
Gain Error Temp Coeff	TBD	µV/°C typ	
Channel-to-Channel Matching	TBD	% max	
AC CHARACTERISTICS			
Output Settling Time	TBD	µs typ	
OFFS_IN Settling Time	TBD	µs typ	
Digital-to-Analog Glitch Impulse	TBD	nV-s typ	
Digital Crosstalk	TBD	nV-s typ	
Analog Crosstalk	TBD	nV-s typ	
Total Harmonic Distortion (THD)	TBD	dB typ	
Output Noise Spectral Density	TBD	nV/(Hz)$^{1/2}$ typ	

NOTES:
[1]See Terminology
[2]B version: Industrial temperature range -40°C. to +85°C.
[3]Guaranteed by design and characterisation, not production tested
Specifications subject to change without notice

Timing Characteristics
Serial Interface

Parameter[1]	Limit at T_{MIN}, T_{MAX} (B Version)	Units	Conditions/Comments
t_1	25	ns min	SCLK High Pulse Width
t_2	25	ns min	SCLK Low Pulse Width
t_3	5	ns min	$\overline{SYNC}$ Falling Edge to SCLK Falling Edge Setup Time
t_4	TBD	ns min	$\overline{SYNC}$ Low Time
t_5	10	ns min	D_{IN} Setup Time
t_6	5	ns min	D_{IN} Hold Time
t_7	5	ns min	$\overline{SYNC}$ Falling Edge to SCLK Rising Edge Setup Time
t_8[2]	10	ns max	SCLK Rising Edge to D_{OUT} Valid
t_9[2]	20	ns max	SCLK Falling Edge to D_{OUT} High Impedance

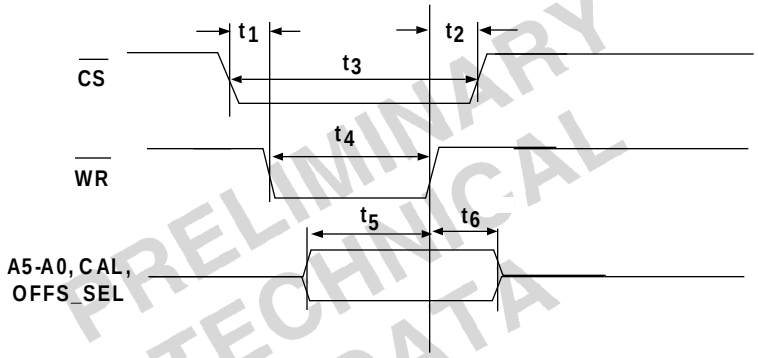
NOTES:
[1]See Interface Timing Diagrams on following pages
[2]These numbers are measured with the load circuit of Figure x

Parallel Interface

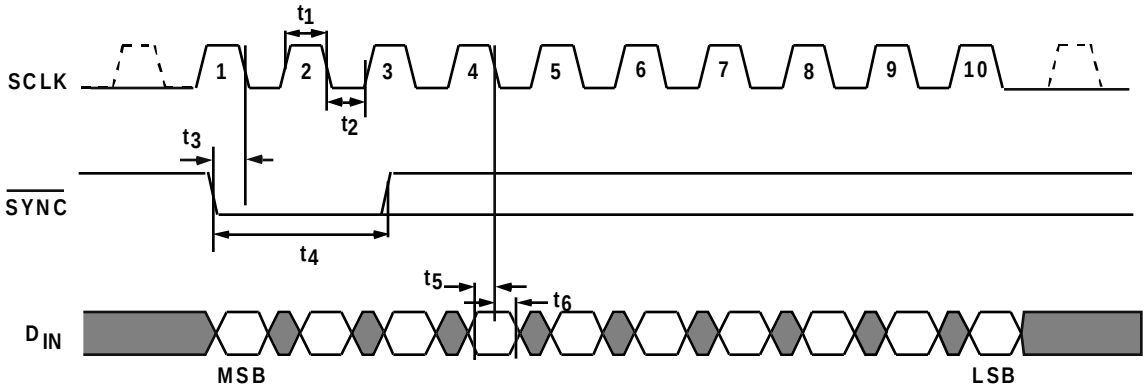
Parameter[1]	Limit at T_{MIN}, T_{MAX} (B Version)	Units	Conditions/Comments
t_1	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_2	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time
t_3	50	ns min	$\overline{CS}$ Pulse Width Low
t_4	50	ns min	$\overline{WR}$ Pulse Width Low
t_5	20	ns min	A5-A0, CAL, OFFS_SEL to $\overline{WR}$ Setup Time
t_6	0	ns min	A5-A0, CAL, OFFS_SEL to $\overline{WR}$ Hold Time

NOTES:
[1]See Interface Timing Diagrams below

Parallel Interface Timing Diagram

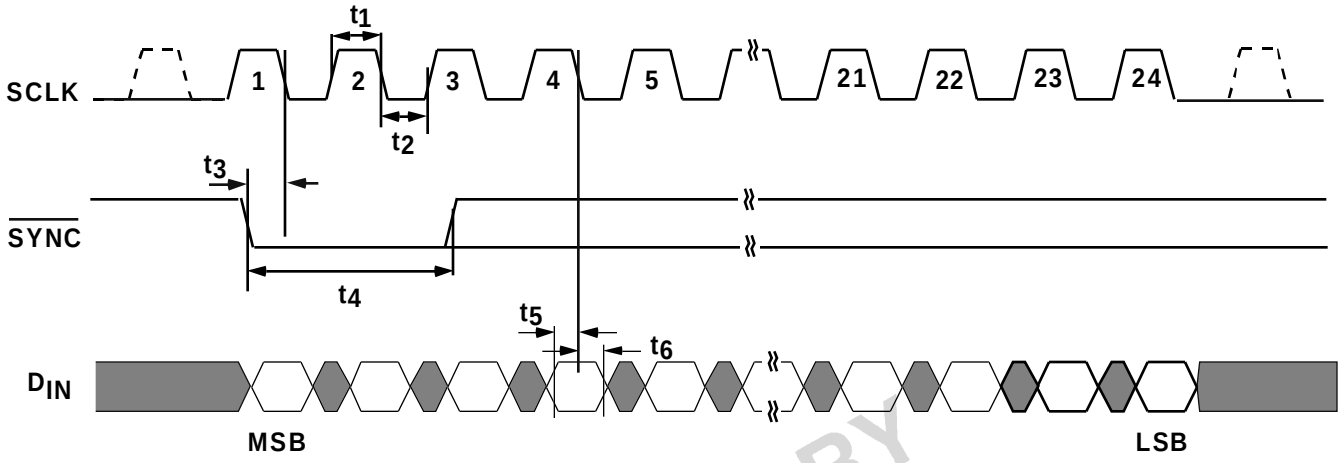


Serial Interface Timing Diagrams

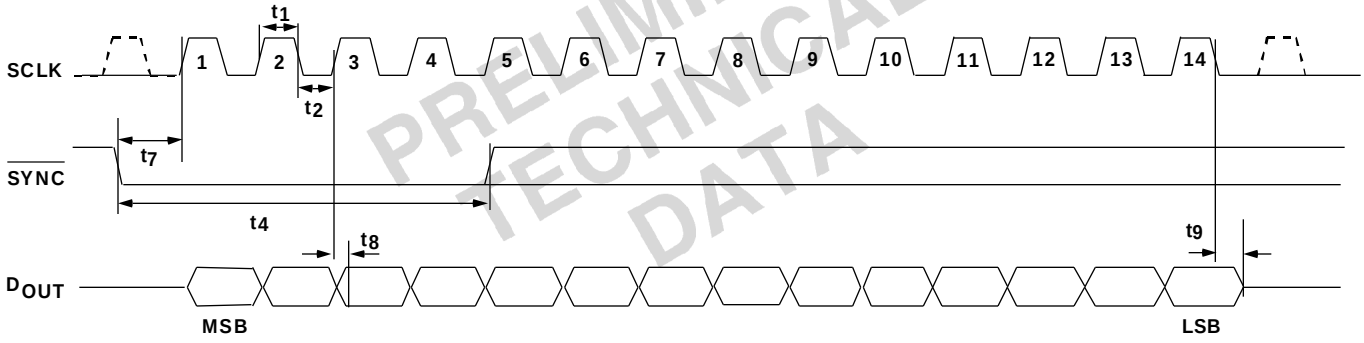


10-Bit Write (SHA Mode and Both Readback Modes)

Serial Interface Timing Diagrams



24-Bit Write (DAC Mode)



14-Bit Read(Both Readback Modes)

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND.....-0.3V to +17V
V_{SS} to AGND.....+0.3V to -17V
AV_{CC} to AGND, DAC_GND.....-0.3V to +7V
DV_{CC} to DGND.....-0.3V to +7V
Digital Inputs to DGND.....-0.3V to DV_{CC}+0.3V
Digital Outputs to DGND.....-0.3V to DV_{CC}+0.3V
REF IN to AGND, DAC_GND.....-0.3V to +7V
V_{IN} to AGND, DAC_GND.....-0.3V to +7V
V_{OUT}0-63 to AGND.....V_{SS}-0.3V to V_{DD}+0.3V
OFFS_OUT to AGND.....V_{SS}-0.3V to V_{DD}+0.3V
AGND to DGND.....TBD
Short-Circuit Current.....TBD mA
Operating Temperature Range
Industrial (B Version).....-40°C to +85°C
Storage Temperature Range.....-65°C to +150°C
Junction Temperature (T_J max).....+150°C
BGA Package,
Power Dissipation.....(T_J max - T_A)/θ_{JA} mW
θ_{JA} Thermal Impedance.....28°C /W
Solder Ball Temperature, Soldering.....TBD °C.

NOTES:

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Transient currents of up to 100mA will not cause SCR latch-up

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5532/64 devices feature proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Terminology

SHA Mode

V_{IN} to V_{OUT} Nonlinearity
This is a measure of the maximum deviation from a straight line passing through the endpoints of the V_{IN} vs. V_{OUT} transfer function. It is expressed as a percentage of the full-scale span.

Offset Error
This is a measure of the output error when V_{IN} = 100mV. Ideally, with V_{IN}=100mV:

V_{OUT}= 350mV-2.5*V_{OFFSET}

Offset error is a measure of the difference between V_{OUT} (actual) and V_{OUT} (ideal). It is expressed in mV.

Full-Scale Error
This is a measure of the output error when V_{IN} = V_{REF}. Ideally, with V_{IN}=V_{REF}:

V_{OUT}= 3.5*V_{REF}-2.5*V_{OFFSET}

Full-scale error is a measure of the difference between V_{OUT} (actual) and V_{OUT} (ideal). It is expressed in mV.

Gain Error
This is a measure of the span error of the analog channel. It is the deviation in slope of the transfer function expressed in mV. It is calculated as:

Gain Error = Full-Scale error - Offset Error

Channel-to-Channel Matching
This is a measure of the difference between V_{OUT} on any two channels if they acquire the same V_{IN}. It is expressed as a percentage of the Full-Scale span.

Output Temp Coefficient
This is a measure of the change in analog output with changes in temperature. It is expressed in ppm/°C.

Output PSRR
Power-Supply Rejection Ratio (PSRR) is a measure of the change in analog output for a change in supply voltage (V_{DD} and V_{SS}). It is expressed in dBs. V_{DD} and V_{SS} are varied ± 5%. For the PSRR measurement of OFFS_OUT, the AV_{CC} supply is varied ± 5%.

DC Crosstalk
This the DC change in the output level of one channel in response to a full-scale change in the output of all other channels. It is expressed in µV.

AC Crosstalk
This is the area of the glitch that occurs on the output of one channel while another channel is acquiring. It is expressed in nV-secs.

Output Settling Time
This is the time taken from when $\overline{BUSY}$ goes high to when the output has settled to ± 0.012% (± 0.5 LSB at 12 bits).

Acquisition Time
This is the time taken for the V_{IN} input to be acquired. It is the length of time that $\overline{BUSY}$ stays low.

Digital Feeedthrough
This is a measure of the impulse injected into the analog outputs from the digital control inputs when the part is not being written to, i.e. $\overline{CS}/\overline{SYNC}$ is high. The digital inputs are toggled between all 0s and all 1s. The area of the glitch is expressed in nV-secs.

Digital Crosstalk
This is the area of the glitch transferred to the analog output while a digital word is being written to the part. The area of the glitch is expressed in nV-secs.

$\overline{TRACK}$ Mode Bandwidth
When $\overline{TRACK}$ input is brought low, the input voltage on V_{IN} is not acquired. It is connected directly to the output buffer stage and the output voltage is:

V_{OUT}= 3.5*V_{IN}-2.5*V_{OFFSET}

V_{IN} can, of course, be an AC waveform in which case the $\overline{TRACK}$ mode has a finite bandwidth. The bandwidth is the frequency at which the sine wave at the output falls to 3dB below the sine wave at the input (ignoring the gain factor).

DAC Mode

Integral Nonlinearity (INL)
This is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is expressed as a percentage of Full-Scale span.

Differential Nonlinearity (DNL)
Differential Nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified DNL of ±1 LSB maximum ensures monotonicity.

Offset Error
This is a measure of the output error with all zeroes loaded to the DAC. Ideally the output should be:

V_{OUT}= 350mV-2.5*V_{OFFSET}

Offset error is a measure of the difference between V_{OUT} (actual) and V_{OUT} (ideal). It is expressed in mV.

Full-Scale Error
This is a measure of the output error with all ones loaded to the DAC. Ideally, the output should be:

V_{OUT}= 3.5*V_{REF}-2.5*V_{OFFSET}

Full-scale error is a measure of the difference between V_{OUT} (actual) and V_{OUT} (ideal). It is expressed in mV.

Gain Error
This is a measure of the span error of the DAC. It is the deviation in slope of the transfer function expressed in mV. It is calculated as:

Gain Error = Full-Scale error - Offset Error

Channel-to-Channel Matching
This is a measure of the difference between V_{OUT} on any two DACs if they have the same digital code loaded to them. It is expressed as a percentage of the Full-scale span.

Output Settling Time
This is the time taken from when the last data bit is clocked into the DAC until the output has settled to within ± 0.012% (± 0.5 LSB at 12 bits).

OFFS_IN Settling Time
This is the time taken from a step change in input voltage on OFFS_IN until the output has settled to within ± 0.012% (± 0.5 LSB at 12 bits).

Digital-to-Analog Glitch Impulse
This is the area of the glitch injected into the analog output when the code in the DAC register changes state. It is specified as the area of the glitch in nV-secs when the digital code is changed by 1 LSB at the major carry transition (011...11 to 100...00).

Digital Crosstalk
This is the area of the glitch transferred to the analog output while a DAC code is being written to the part. The area of the glitch is expressed in nV-secs.

Analog Crosstalk
This the area of the glitch transferred to the output of one DAC due to a full-scale change in the output of another DAC. The area of the glitch is expressed in nV-secs.

Total Harmonic Distortion
This is the difference between an ideal sine-wave and a digitally constructed one using the DAC. The THD is a measure of the harmonics and noise present on the DAC output. It is measured in dBs.

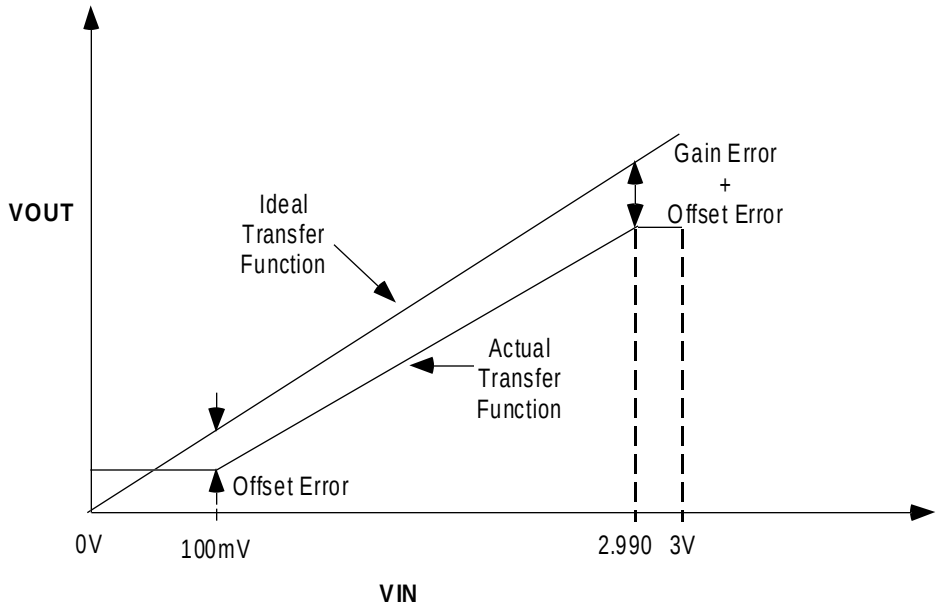


Figure 1. SHA Transfer Function

PIN FUNCTION DESCRIPTION

PIN NUMBERS

Pin No.	Mnemonic	Function
	AGND (1-4)	4 Analog GND pins.
	AV_{CC} (1-4)	4 Analog supply pins. Voltage range from +4.75V to +5.25V.
	V_{DD} (1-8)	8 V_{DD} supply pins. Voltage range from +8V to +16.5V.
	V_{SS} (1-8)	8 V_{SS} supply pins. Voltage range from -4.75V to -16.5V.
	DGND (1-2)	2 Digital GND pins
	DV_{CC} (1-2)	2 Digital supply pins. Voltage range from +2.7V to +5.25V.
	DAC_GND (1-4)	Reference GND supply for all the DACs.
	REF IN 1	Reference voltage for channels 0-31
	REF IN 2	Reference voltage for channels 32-63
	V_{OUT} (0-63)	Analog output voltages from the 64 channels.
	V_{IN}	Analog input voltage
	A5-A1[1], A0[2]	Parallel Interface: 6 address pins for the 64 channels. A5=MSB of channel address, A0=LSB.
	CAL[1]	Parallel Interface: Control input which allows all 64 channels to acquire V_{IN} simultaneously
	$\overline{CS}$ / $\overline{SYNC}$[2]	This pin is both the active low Chip Select pin for the parallel interface and the Frame Synchronisation pin for the serial interface.
	$\overline{WR}$[1]	Parallel Interface. Write pin. Active low. This is used in conjunction with the $\overline{CS}$ pin to address the device using the parallel interface.
	OFFSET_SEL[1]	Offset Select pin. This is activated when writing to the DAC which provides its output at the OFFS_OUT pin.
	SCLK[2]	Serial Clock input for serial interface. This can operate up at clock speeds up to 20MHz.
	D_{IN}[2]	Data input for serial interface. Data must be valid onthe falling edge of SCLK
	D_{OUT}	Output from the DAC registers for readback. Data is clocked out on the rising edge of SCLK and is valid on the falling edge of SCLK.
	SER/$\overline{PAR}$[1]	This pin allows the user to select whether the serial or parallel interface will be used. If the pin is tied low, the parallel interface will be used. If it is tied high, the serial interface will be used.
	OFFS_IN	Offset input. The user can supply a voltage here to offset the output span. OFFS_OUT can also be tied to this pin if the user wants to drive this pin with the Offset Channel.
	OFFS_OUT	Offset output. This is the acquired offset voltage which can be tied to OFFS_IN to offset the span.
	$\overline{BUSY}$	This output tells the user when the input voltage is being acquired. It goes low during acquisition and returns high when the acquisition operation is complete.
	$\overline{TRACK}$/$\overline{RESET}$[2]	If this input is held high, V_{IN} is acquired once the channel is addressed. While it is held low, the input to the gain/offset stage is switched directly to V_{IN}. The addressed channel begins to acquire V_{IN} on the rising edge of $\overline{TRACK}$. See $\overline{TRACK}$ Input section for further information. This input can also be used as a means of resetting the complete device to its power-on-reset conditions. This is achieved by applying a low going pulse of between 50ns and 150ns to this pin.See section on RESET Function for further details.

NOTES:
[1]Internal Pull-down devices on these logic inputs. Therfore, they can be left floating and will default to a logic low condition.
[2]Internal Pull-up devices on these logic inputs. Therfore, they can be left floating and will default to a logic high condition.

Circuit Description

The AD5532/64 can be thought of as consisting of an ADC and 32/64 DACs in a single package. The input voltage V_{IN} is sampled and converted into a digital word. The digital result is loaded into one of the DAC registers and is converted (after the gain and offset in the output buffer) into an analog output voltage ($V_{OUT}0$ - V_{OUT} 63). Since the channel output voltage is effectively the output of a DAC there is no droop associated with it. As long as power is maintained to the device the output voltage will remain constant until this channel is addressed again.

To update a single channel's output voltage the required new voltage level is set up on the common input pin, V_{IN}. The desired channel is then addressed via the parallel port or the serial port. When the channel address has been loaded, provided $\overline{TRACK}$ is high, the circuit begins to acquire the correct code to load to the DAC in order that the DAC output matches the voltage on V_{IN}. At this stage the $\overline{BUSY}$ pin goes low and remains so until the acquistion is complete. The non-inverting input to the output buffer (gain and offset stage) is tied to V_{IN} during the acquisition period to avoid spurious outputs while the DAC acquires the correct code. This is completed in 16 µs max. The $\overline{BUSY}$ pin goes high at this stage. Also at this time the updated DAC output assumes control of the output voltage. The output voltage of the DAC is connected to the non-inverting input of the output buffer. The held voltage will remain on the output pin indefinitely, without drooping, as long as power is maintained to the device.

On power-on, all the DACs, including the offset channel, are loaded with zeroes. The outputs of the DACs are at 100mV and the outputs of the output buffers are at negative full-scale. If the OFFS_IN pin is driven by the on-board offset channel, the outputs $V_{OUT}0$ to $V_{OUT}63$ are also at 100mV on power-on since OFFS_IN = 100mV (V_{OUT}=3.5*V_{DAC}-2.5*V_{OFFSET}=350mV-250mV=100mV).

$\overline{TRACK}$ Input

In normal mode of operation, $\overline{TRACK}$ is held high and the channel begins to acquire when it is addressed. However, if $\overline{TRACK}$ is low when the channel is addressed then V_{IN} is switched to the output buffer and an acquisition on the channel will not occur until a rising edge of $\overline{TRACK}$. At this stage the $\overline{BUSY}$ pin will go low until the acquisition is complete at which point the DAC assumes control of the voltage to the output buffer and V_{IN} is free to change again without affecting this output value.

This is useful in an application where the user wants to ramp up V_{IN} until V_{OUT} reaches a particular level (Figure 2). V_{IN} doesn't need to be acquired continuously while it is ramping up. $\overline{TRACK}$ can be kept low and only when V_{OUT} has reached its desired voltage is $\overline{TRACK}$ brought high. At this stage, the acquisition of V_{IN} begins.

In the example shown, a desired voltage is required on the output of the pin driver. This voltage is represented by one input to a comparator. The microcontroller/microprocessor ramps up the input voltage on V_{IN} through a DAC. $\overline{TRACK}$ is kept low while the voltage on V_{IN} ramps up so that V_{IN} is not continually acquired. When the desired voltage is reached on the output of the pin driver, the comparator output switches. The µC/µP then knows what code is required to be input in order to get the desired voltage at the DUT. The $\overline{TRACK}$ input is now brought high and the part begins to acquire V_{IN}. At this stage $\overline{BUSY}$ goes low until V_{IN} has been acquired. Then the output buffer is switched from V_{IN} to the output of the DAC.

Output Buffer Stage - Gain and Offset

The function of the output buffer stage is to translate the 0-3V output of the DAC to a useful range for ATE applications. This is done by gaining up the DAC output by 3.5 and offsetting the voltage by the voltage on OFFS_IN pin. The following table shows how the output range relates to the Offset voltage supplied by the user.

V_{OUT} = 3.5*V_{DAC} - 2.5*V_{OFFSET}

V_{DAC} is the output of the DAC and its range is 0-V_{REF}. V_{OFFSET} is the voltage at the OFFS_IN pin.

SAMPLE OUTPUT RANGES

V_{OFFSET} (V)	V_{DAC} (V)	V_{OUT} (V)
1	0 to 3	-2.5 to 8
0.5	0 to 3	-1.25 to 9.25

V_{OUT} is limited only by the headroom of the output amplifiers.

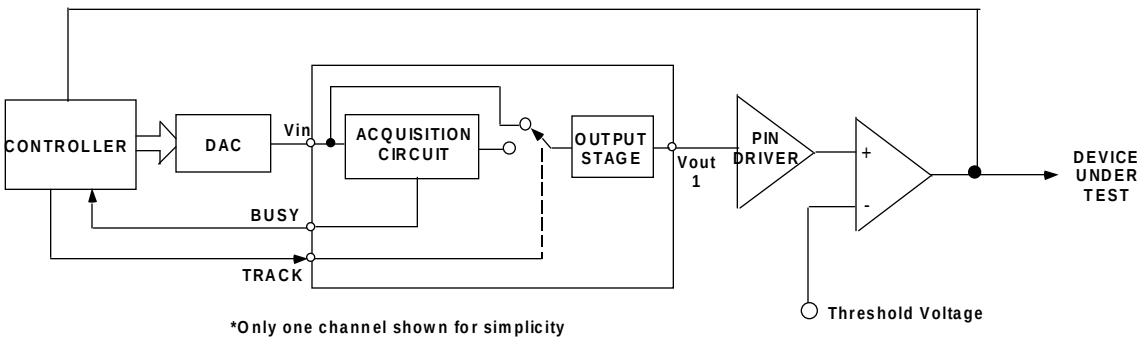


Figure 2. Typical ATE circuit using TRACK Input

Offset Voltage Channel
The offset voltage can be supplied externally by the user or it can be supplied by an additional DAC on the device itself. The offset voltage channel is used just like any other channel. The required offset voltage is set up on V_{IN} and it is acquired by the DAC. The DAC output is connected directly to OFFS_OUT. This offset voltage is used as the offset voltage for the 64 output amplifiers.

Reset Function
The reset function on the AD5532/64 can be used to reset all nodes on this device to their power-on-reset condition. This is implemented by applying a low going pulse of between 50ns and 150ns to the $\overline{TRACK}/\overline{RESET}$ pin on the device. If the applied pulse is less than 50ns it is taken as being a glitch and no operation takes place. If the applied pulse is wider than 150ns this pin adopts its track function on the selected channel, V_{IN} is switched to the output buffer and an acquisition on the channel will not occur until a rising edge of $\overline{TRACK}$.

INTERFACE
Serial Interface
The serial interface is controlled by 4 pins.
$\overline{SYNC}$, D_{IN}, SCLK: Standard 3-wire SPI interface pins. The $\overline{SYNC}$ pin is shared with the $\overline{CS}$ function of the parallel interface.
D_{OUT}: Data Out pin for reading back the contents of the DAC registers. The data is clocked out on the rising edge of SCLK and is valid on the falling edge of SCLK.

The SER/$\overline{PAR}$ pin must also be tied high to enable the serial interface and to disable the parallel interface.

Mode bits: There are 4 different modes of operation. See below for descriptions.

Cal bit: This is used as a calibration instruction. When this is active, all 64 channels acquire V_{IN} simultaneously.

Offset_Sel bit: Used to address the offset voltage control channel.

A5-A0: Used to address any one of the 64 channels (A5 = MSB of address, A0=LSB).

DB13-DB0: These are used to write a 14-bit word into the addressed DAC register. Clearly, this is only valid when in DAC mode.

The AD5532/64 can be used in 4 different modes of operation. These modes are set by two Mode bits, the first 2 bits in the serial word.

MODES OF OPERATION

Mode Bit 1	Mode Bit 2	Operating Mode
0	0	SHA Mode
0	1	DAC Mode
1	0	Acquire and Readback
1	1	Readback

1) SHA Mode:
Standard mode where a channel is addressed and that channel acquires the voltage on V_{IN}. This mode requires a 10-bit write (see figure below) to address the relevant channel ($V_{OUT}0$-$V_{OUT}63$, Offset Channel or all channels).

2) DAC Mode:
In this mode, a particular DAC register can be written to directly. This mode requires the 10-bit write from the SHA mode plus an extra 14 bits to write to the 14-bit register of the DAC. Any one of the 64 DAC registers may be written to individually or they can all be loaded simultaneously.

3)Acquire and Readback Mode:
This mode allows the user to read back the data in a particular DAC register. The relevant DAC is addressed (10-bit write as with SHA mode) and V_{IN} is acquired in typically 16us. Following the acquisition the next falling edge of $\overline{SYNC}$ clocks the data in the relevant DAC register out onto the D_{OUT} line in a 14-bit serial format.The full acquisition time must elapse before the DAC register data can be clocked out.

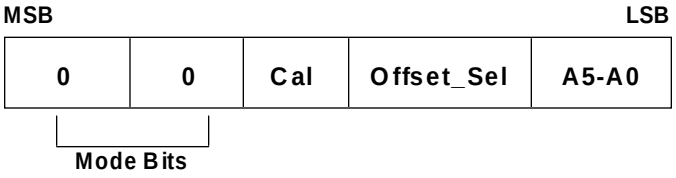
4) Readback
Again, this is a readback mode but no acquisition is performed. The relevant DAC is addressed (10-bit write) and on the next falling edge of $\overline{SYNC}$, the data in the relevant DAC register is clocked out onto the D_{OUT} line in a 14-bit serial format.

The serial write and read words can be seen in the figures below.

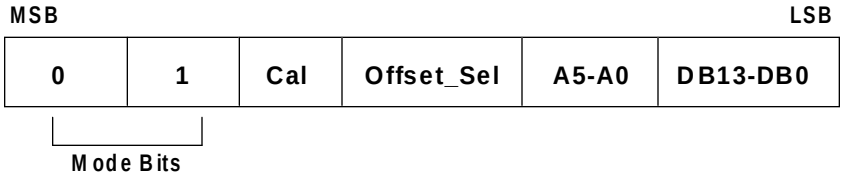
Digital Readback
This feature allows the user to readback the DAC register code of any of the DACs. This is useful if the system has been calibrated and the user wants to know what code in the DAC corresponds to a desired voltage on V_{OUT}. If the user requires this voltage again, all he needs to do is to input the code directly to the DAC register without going through the acquisition sequence. The user can readback the DAC register contents through the serial interface and can write directly to the DAC, again through the serial interface.

Parallel Interface
The parallel interface is controlled by 10 pins.
$\overline{CS}$: Active low package select pin. This pin is shared with the $\overline{SYNC}$ function for the serial interface.
$\overline{WR}$: Active low Write pin. The values on the address pins are latched on a rising edge of $\overline{WR}$.
A5-A0: 6 Address pins (A5=MSB of address, A0=LSB). These are used to address the relevant channel (out of a possible 64).
Offset_Sel: Offset select pin. This has the same function as the Offset_Sel bit in the serial interface. When it is activated, the offset voltage control channel is addressed. The address on A5-A0 is ignored in this case.
Cal:Same functionality as the Cal bit in the serial interface (calibration instruction). When this pin is active, all 64 channels acquire V_{IN} simultaneously.

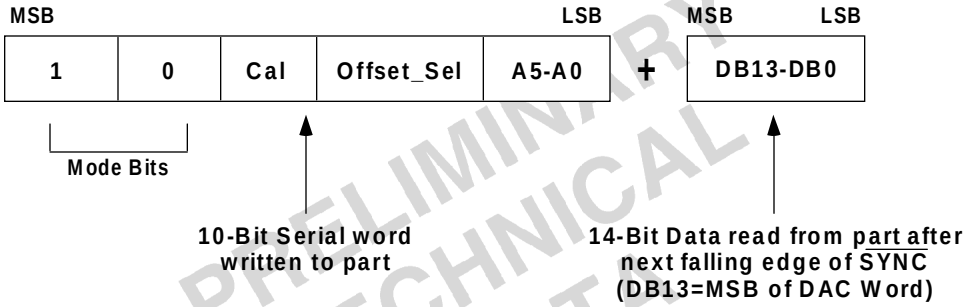
The SER/$\overline{PAR}$ bit must be tied low to enable the parallel interface and disable the serial interface.



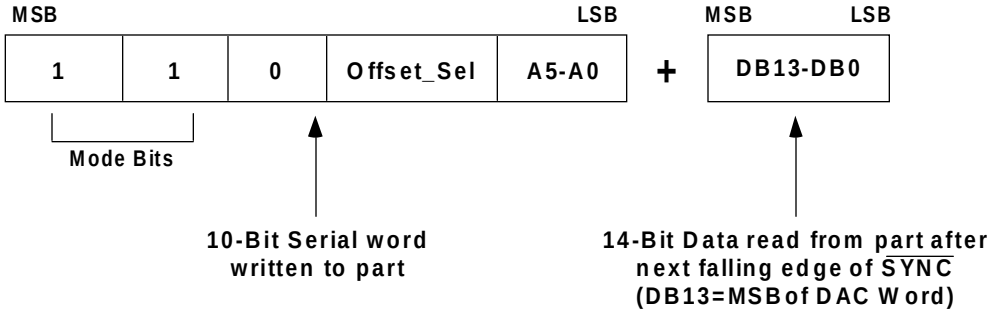
10-Bit Input Serial Write Word (SHA Mode)



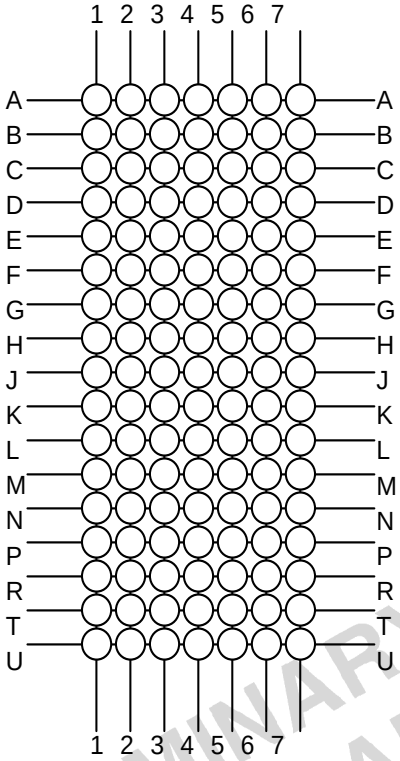
24-Bit Input Serial Write Word (DAC Mode)



Input Serial Interface (Acquire and Readback Mode)



Input Serial Interface (Readback Mode)



PBGA BALL CONFIGURATIONS

PBGA Number	Ball Name	PBGA Number	Ball Name	PBGA Number	Ball Name	PBGA Number	Ball Name
A1	VO26	E3	AVSS8	J5	AGND3	N7	VO59
A2	$\overline{CS}$/$\overline{SYNC}$	E4	AVSS7	J6	AGND4	P1	VO34
A3	A2	E5	N/C	J7	VO3	P2	VO41
A4	A1	E6	VO10	K1	VO31	P3	AVDD4
A5	A0	E7	VO5	K2	DACGND1	P4	AVDD7
A6	$\overline{BUSY}$	F1	VO14	K3	DACGND2	P5	REF_IN1
A7	VO9	F2	VO12	K4	DACGND3	P6	VO55
B1	VO25	F3	AVSS6	K5	DACGND4	P7	VO62
B2	$\overline{WR}$	F4	AVSS5	K6	AIN	R1	VO35
B3	SCLK	F5	DVCC1	K7	VO2	R2	VO40
B4	SDIN	F6	DVCC2	L1	VO32	R3	VO43
B5	SDOUT	F7	VO4	L2	AVCC1	R4	VO46
B6	OFFSEL	G1	VO16	L3	AVCC2	R5	VO63
B7	VO8	G2	OFFS_IN	L4	AVCC3	R6	VO54
C1	VO24	G3	OFFS_OUT	L5	AVCC4	R7	VO58
C2	VO22	G4	AVSS4	L6	VO0	T1	VO37
C3	A5	G5	SER/$\overline{PAR}$	L7	VO1	T2	VO39
C4	A4	G6	VO15	M1	VO27	T3	VO49
C5	A3	G7	VO17	M2	AVDD1	T4	VO48
C6	VO13	H1	VO18	M3	AVDD2	T5	VO45
C7	VO7	H2	AVSS1	M4	AVDD5	T6	VO53
D1	VO23	H3	AVSS2	M5	AVDD8	T7	VO57
D2	VO21	H4	AVSS3	M6	VO60	U1	VO36
D3	CAL	H5	$\overline{TRACK}$/$\overline{RESET}$	M7	VO61	U2	VO38
D4	DGND1	H6	VO19	N1	VO33	U3	VO50
D5	DGND2	H7	VO51	N2	VO42	U4	VO47
D6	VO11	J1	VO30	N3	AVDD3	U5	VO44
D7	VO6	J2	VO28	N4	AVDD6	U6	VO52
E1	VO29	J3	AGND1	N5	REF_OUT	U7	VO56
E2	VO20	J4	AGND2	N6	REF_IN2		