élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2166C

110 MHz Current Feedback Amplifier with Disable

Features

- 110 MHz 3 dB bandwidth ($A_V = +2$)
- 115 MHz 3 dB bandwidth ($A_V = +1$)
- 0.01% differential gain, $R_L = 500\Omega$
- 0.01° differential phase, $R_L = 500\Omega$
- Low supply current, 7.5 mA
- Fast disable < 75 ns
- Low cost
- 1500 V/μs slew rate

Applications

- Video amplifiers
- Cable drivers
- RGB amplifiers
- Test equipment amplifiers
- Current to voltage converters
- Broadcast equipment
- High speed communications
- Video multiplexing

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2166CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL2166CS	−40°C to +85°C	8-Pin SOIC	MDP0027

General Description

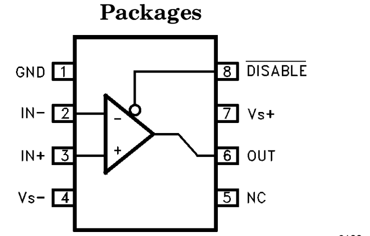
The EL2166C is a current feedback operational amplifier with −3 dB bandwidth of 110 MHz at a gain of +2. Built using the Elantec proprietary monolithic complementary bipolar process, this amplifer uses current mode feedback to achieve more bandwidth at a given gain than a conventional voltage feedback operational amplifier.

The EL2166C is designed to drive a double terminated 75Ω coax cable to video levels. Differential gain and phase are excellent when driving both loads of 500Ω (<0.01%/<0.01°) and double terminated 75Ω cables (0.025%/0.05° @ $V_S = \pm 15V$, 0.04%/0.02° @ $V_S = \pm 5V$).

The EL2166C has a superior output disable function. Time to enable or disable is < 75 ns. The $\overline{\text{DISABLE}}$ pin is TTL/CMOS compatible. In disable mode, the amplifier can withstand over 1500 V/μs signals at their outputs. The amplifier can operate on any supply voltage from 10V (±5V) to 33V (±16.5V), yet consume only 7.5 mA at any supply voltage. The EL2166C is available in 8-pin P-DIP and 8-pin SO packages.

Connection Diagram

EL2166C SO, P-DIP Packages



Top View

Manufactured under U.S. Patent No. 5,420,542, 4,893,091

Note: All information contained in this data sheet has been carefully checked and is believed to be accurate as of the date of publication; however, this data sheet cannot be a "controlled document". Current revisions, if any, to these specifications are maintained at the factory and are available upon your request. We recommend checking the revision level before finalization of your design documentation.

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Absolute Maximum Ratings ($T_A = 25°C$)

Voltage between V_S+ and V_S-	+33V
Voltage between +IN and −IN	±6V
Current into +IN or −IN	10 mA
Output Current	±50 mA
Current into $\overline{DISABLE}$ Pin	±5 mA
Voltage between $\overline{DISABLE}$ Pin and GND Pin	±7V
Voltage at IN+, IN−, V_{OUT}, $\overline{DISABLE}$, GND Pins	$(V_{S-}) - 0.5V$ to $(V_{S+}) + 0.5V$
Internal Power Dissipation	See Curves
Operating Ambient Temperature Range	−40°C to +85°C
Operating Junction Temperature Plastic Packages	150°C
Storage Temperature Range	−65°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at $T_A = 25°C$ and QA sample tested at $T_A = 25°C$, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at $T_A = 25°C$ for information purposes only.

Open Loop DC Electrical Characteristics

$V_S = \pm 15V$, $R_L = 150\Omega$, $T_A = 25°C$ unless otherwise specified

Parameter	Description	Conditions	Temp	Limits			Test Level	Units
				Min	Typ	Max	EL2166C	
V_{OS}	Input Offset Voltage	$V_S = \pm 5V, \pm 15V$	25°C		2	10	I	mV
TC V_{OS}	Average Offset Voltage Drift (Note 1)		Full		10		V	µV/°C
$+I_{IN}$	+Input Current	$V_S = \pm 5V, \pm 15V$	25°C		0.5	5	I	µA
$-I_{IN}$	−Input Current	$V_S = \pm 5V, \pm 15V$	25°C		5	20	I	µA
CMRR	Common Mode Rejection Ratio (Note 2)	$V_S = \pm 5V, \pm 15V$	25°C	55	62		II	dB
−ICMR	−Input Current Common Mode Rejection (Note 2)	$V_S = \pm 5V, \pm 15V$	25°C		0.1	2	I	µA/V
PSRR	Power Supply Rejection Ratio (Note 3)		25°C	65	72		II	dB
−IPSR	−Input Current Power Supply Rejection (Note 3)		25°C		0.1	2	I	µA/V

TD is 2.5in

Open Loop DC Electrical Characteristics — Contd.

$V_S = \pm 15V$, $R_L = 150\Omega$, $T_A = 25°C$ unless otherwise specified

Parameter	Description	Conditions	Temp	Limits			Test Level	Units
				Min	Typ	Max	EL2166C	
R_{OL}	Transimpedance (Note 4)	$V_S = \pm 15V$ $R_L = 400\Omega$	25°C	500	2000		I	kΩ
		$V_S = \pm 5V$ $R_L = 150\Omega$	25°C	500	1200		I	kΩ
$+R_{IN}$	+ Input Resistance		25°C	2.0	5.0		I	MΩ
$+C_{IN}$	+ Input Capacitance		25°C		2.5		V	pF
CMIR	Common Mode Input Range	$V_S = \pm 15V$	25°C	±12.6	±13.2		I	V
		$V_S = \pm 5V$	25°C	±2.6	±3.2		I	V
V_O	Output Voltage Swing	$R_L = 400\Omega$, $V_S = \pm 15V$	25°C	±12	±13.5		I	V
		$R_L = 150\Omega$, $V_S = \pm 15V$	25°C		±11.4		V	V
		$R_L = 150\Omega$, $V_S = \pm 5V$	25°C	±3.0	±3.7		I	V
I_{SC}	Output Short Circuit Current (Note 5)	$V_S = \pm 5V$, $V_S = \pm 15V$	25°C	50	80	130	I	mA
I_S	Supply Current	$V_S = \pm 15V$ $V_S = \pm 5V$	25°C		7.5	10.0	I	mA
I_S, OFF	Supply Current Disabled, Pin 8 = 0V		25°C		7.3	10.0	I	mA
I_{OUT}, OFF	Output Current Disabled, Pin 8 = 0V	$A_V = +1$	25°C		2.0	50.0	I	μA
V_{IH}	$\overline{\text{DISABLE}}$ Pin Voltage for Output Enabled (Note 9)		25°C	2.0			I	V
V_{IL}	$\overline{\text{DISABLE}}$ Pin Threshold for Output Disabled		25°C			0.8	I	V
I_{DIS}, ON	$\overline{\text{DISABLE}}$ Pin Input Current, Pin 8 = +5V		25°C		70	150	I	μA
I_{DIS}, OFF	$\overline{\text{DISABLE}}$ Pin Input Current, Pin 8 = 0V		25°C	−150	−60		I	μA

TD is 4.6in

Closed Loop AC Electrical Characteristics

$V_S = \pm 15V$, $A_V = +2$, $R_F = 560\Omega$, $R_L = 150\Omega$, $T_A = 25°C$ unless otherwise noted

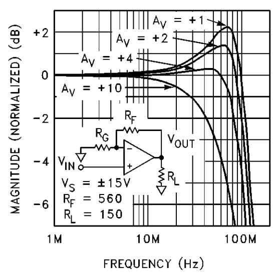
Parameter	Description	Conditions	Limits			Test Level	Units
			Min	Typ	Max	EL2166C	
BW	−3 dB Bandwidth (Note 8)	$V_S = \pm 15V$, $A_V = +2$		110		V	MHz
		$V_S = \pm 15V$, $A_V = +1$		115		V	MHz
		$V_S = \pm 5V$, $A_V = +2$		95		V	MHz
		$V_S = \pm 5V$, $A_V = +1$		100		V	MHz
SR	Slew Rate (Notes 6, 8)	$R_L = 400\Omega$	1000	1500		IV	V/µs
t_r, t_f	Rise Time, Fall Time, (Note 8)	$V_{OUT} = \pm 500mV$		3.2		V	ns
t_{pd}	Propagation Delay (Note 8)			4.3		V	ns
OS	Overshoot (Note 8)	$V_{OUT} = \pm 500$ mV		7		V	%
t_s	0.1% Settling Time (Note 8)	$V_{OUT} = \pm 10V$ $A_V = \pm 1$, $R_L = 1K$		35		V	ns
dG	Differential Gain (Notes 7, 8)	$R_L = 150\Omega$, $V_S = \pm 15V$		0.025		V	%
		$R_L = 150\Omega$, $V_S = \pm 5V$		0.05		V	%
		$R_L = 500\Omega$, $V_S = \pm 15V$		0.01		V	%
		$R_L = 500\Omega$, $V_S = 5V$		0.01		V	%
dP	Differential Phase (Notes 7, 8)	$R_L = 150\Omega$, $V_S = \pm 15V$		0.04		V	deg (°)
		$R_L = 150\Omega$, $V_S = \pm 5V$		0.02		V	deg (°)
		$R_L = 500\Omega$, $V_S = \pm 15V$		0.01		V	deg (°)
		$R_L = 500\Omega$, $V_S = 5V$		0.01		V	deg (°)
t_{DIS}	Disable/Enable Time (Note 10)			75		V	ns

Note 1: Measured from T_{MIN} to T_{MAX}.
Note 2: $V_{CM} = \pm 12.6V$ for $V_S = \pm 15V$ and $T_A = 25°C$
$V_{CM} = \pm 2.6V$ for $V_S = \pm 5V$ and $T_A = 25°C$
Note 3: The supplies are moved from ±5V to ±15V.
Note 4: $V_{OUT} = \pm 7V$ for $V_S = \pm 15V$, and $V_{OUT} = \pm 2V$ for $V_S = \pm 5V$.
Note 5: A heat sink is required to keep junction temperature below absolute maximum when an output is shorted.
Note 6: Slew Rate is with V_{OUT} from +10V to −10V and measured at the 25% and 75% points.
Note 7: DC offset from −0.714V through +0.714V, AC amplitude 286 mV_{p-p}, f = 3.58 MHz.
Note 8: All AC tests are performed on a "warmed up" part, except for Slew Rate, which is pulse tested.
Note 9: The EL2166C will remain ENABLED if pin 8 is either left unconnected or V_{IH} is applied to pin 8.
Note 10: Disable/Enable time is defined as the time from when the logic signal is applied to the $\overline{\text{DISABLE}}$ pin to when the output voltage has gone 50% of the way from its initial to its final value.

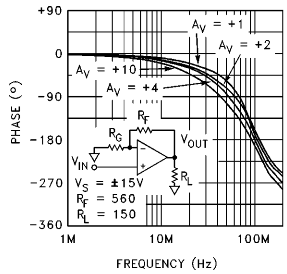
TD is 4.4in

Typical Performance Curves

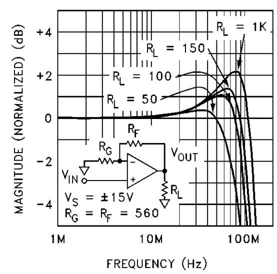
Non-Inverting Frequency Response (Gain)



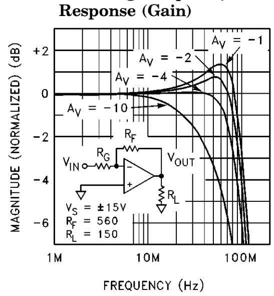
Non-Inverting Frequency Response (Phase)



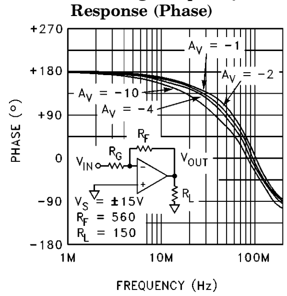
Frequency Response for Various R_L



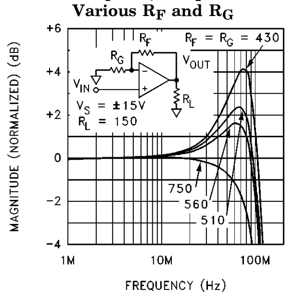
Inverting Frequency Response (Gain)



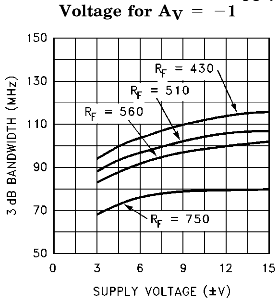
Inverting Frequency Response (Phase)



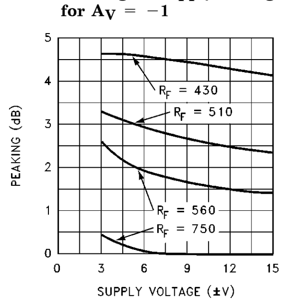
Frequency Response for Various R_F and R_G



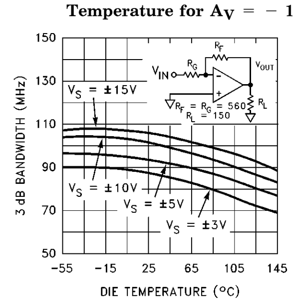
3 dB Bandwidth vs Supply Voltage for A_V = −1



Peaking vs Supply Voltage for A_V = −1



3 dB Bandwidth vs Temperature for A_V = − 1



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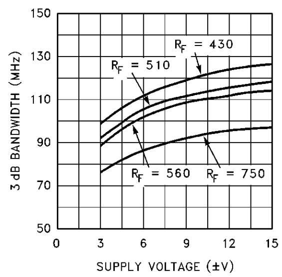
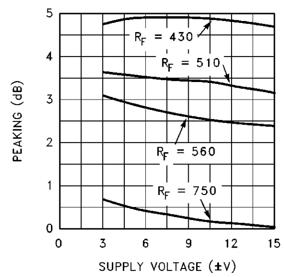
Typical Performance Curves — Contd.

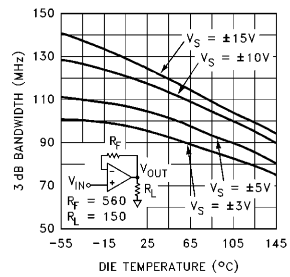
3 dB Bandwidth vs Supply Voltage for $A_V = +1$



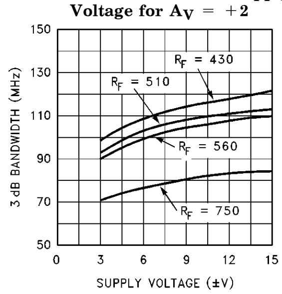
Peaking vs Supply Voltage for $A_V = +1$



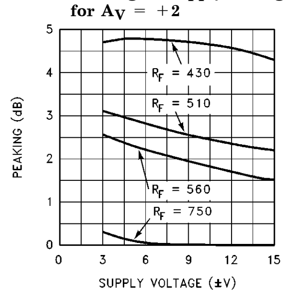
3 dB Bandwidth vs Temperature for $A_V = +1$



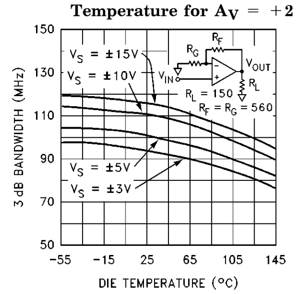
3 dB Bandwidth vs Supply Voltage for $A_V = +2$



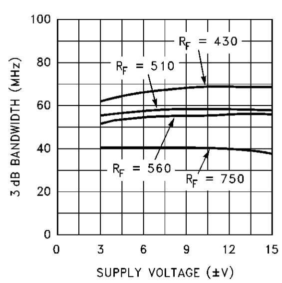
Peaking vs Supply Voltage for $A_V = +2$



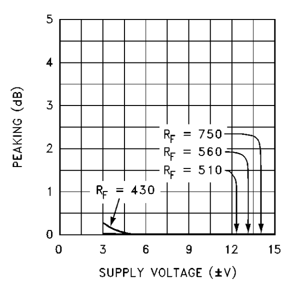
3 dB Bandwidth vs Temperature for $A_V = +2$



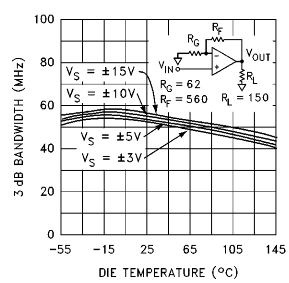
3 dB Bandwidth vs Supply Voltage for $A_V = +10$



Peaking vs Supply Voltage for $A_V = +10$



3 dB Bandwidth vs Temperature for $A_V = +10$



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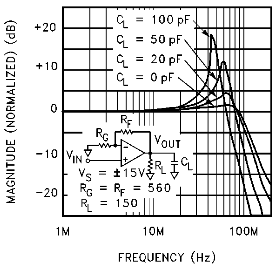
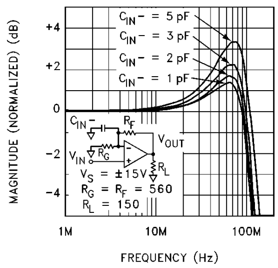
Typical Performance Curves — Contd.

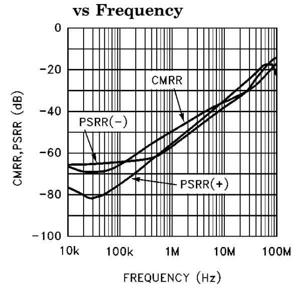
Frequency Response for Various C_L



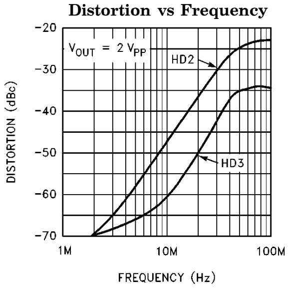
Frequency Response for Various C_{IN-}



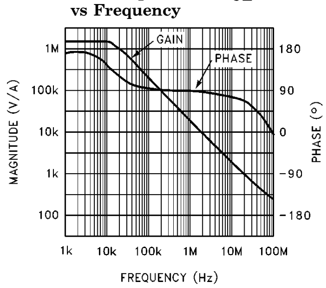
PSRR and CMRR vs Frequency



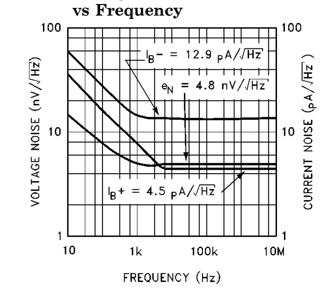
2nd and 3rd Harmonic Distortion vs Frequency



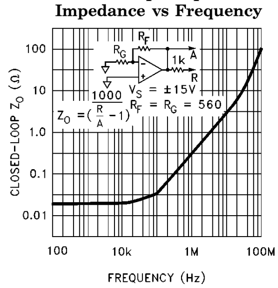
Transimpedance (R_{OL}) vs Frequency



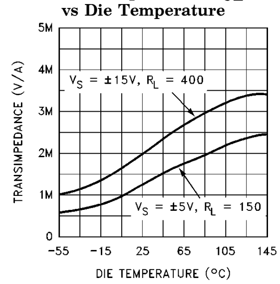
Voltage and Current Noise vs Frequency



Closed-Loop Output Impedance vs Frequency



Transimpedance (R_{OL}) vs Die Temperature



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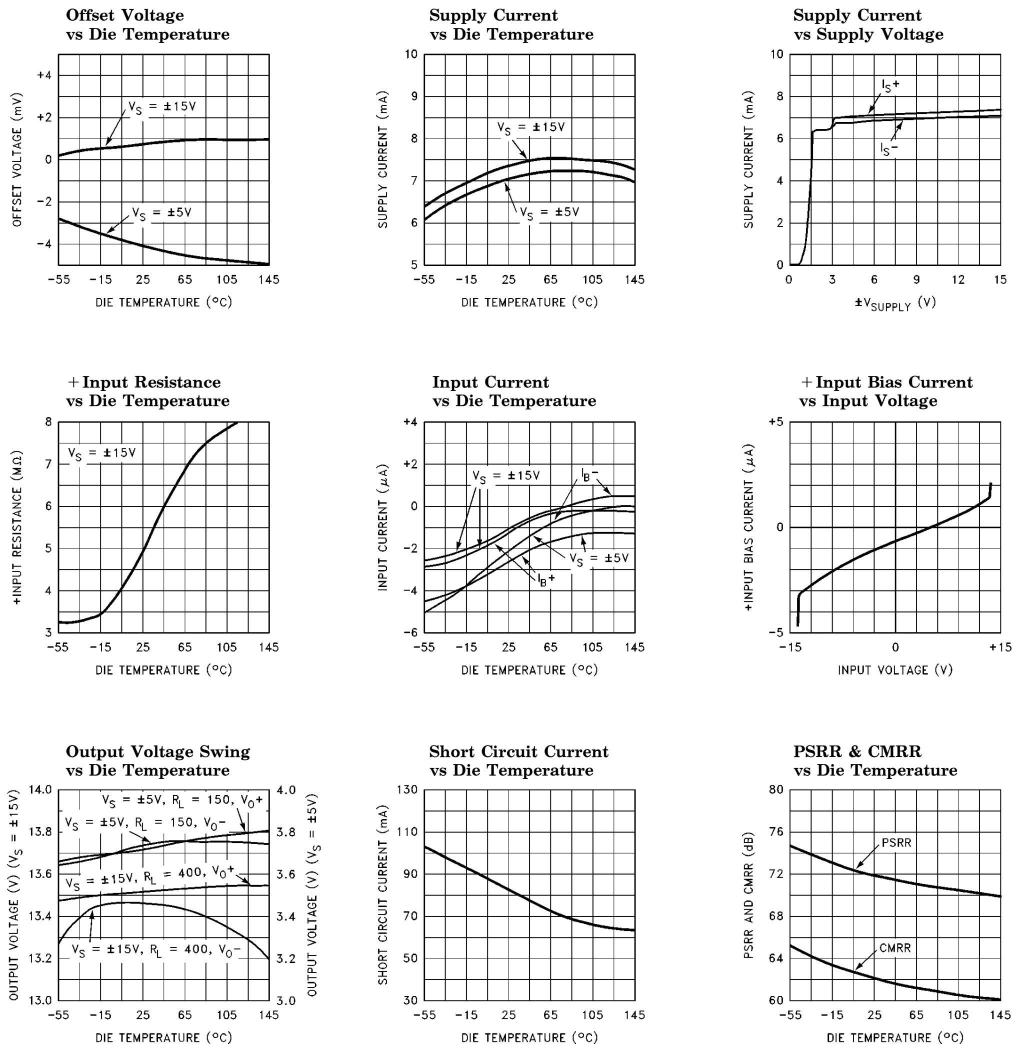
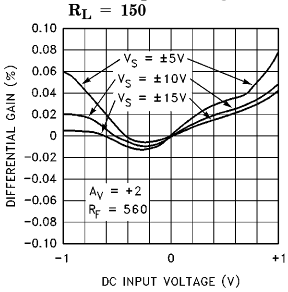
Typical Performance Curves — Contd.



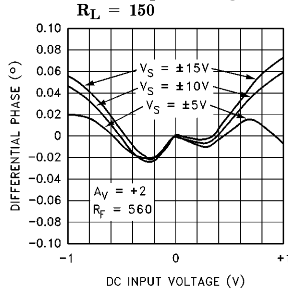
2166-5

Typical Performance Curves — Contd.

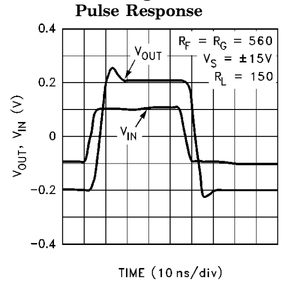
Differential Gain vs DC Input Voltage, R_L = 150



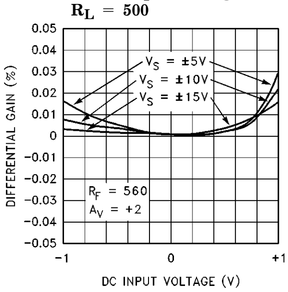
Differential Phase vs DC Input Voltage, R_L = 150



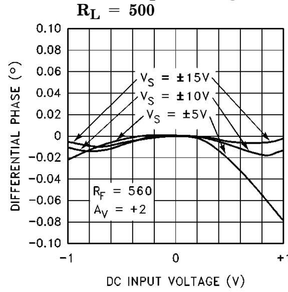
Small Signal Pulse Response



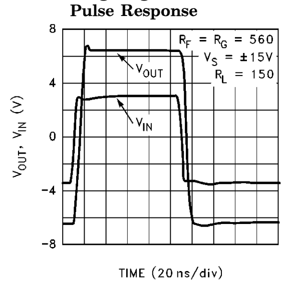
Differential Gain vs DC Input Voltage, R_L = 500



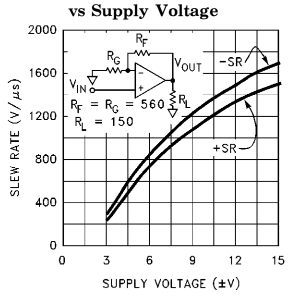
Differential Phase vs DC Input Voltage, R_L = 500



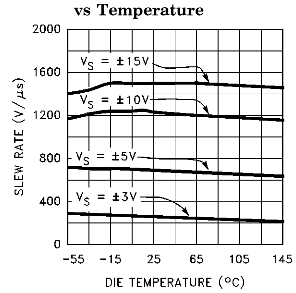
Large Signal Pulse Response



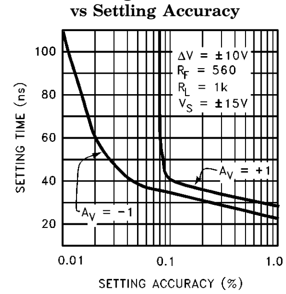
Slew Rate vs Supply Voltage



Slew Rate vs Temperature



Settling Time vs Settling Accuracy



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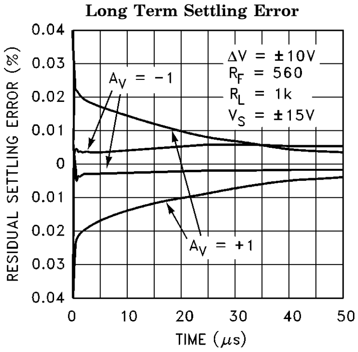
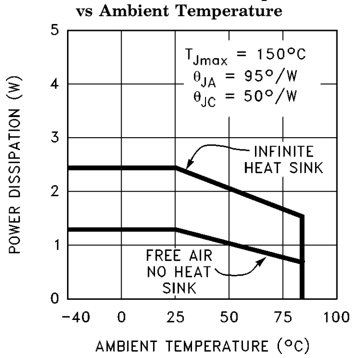
Typical Performance Curves — Contd.

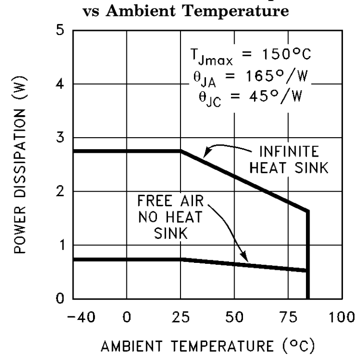
Long Term Settling Error



8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



8-Lead Plastic SO Maximum Power Dissipation vs Ambient Temperature



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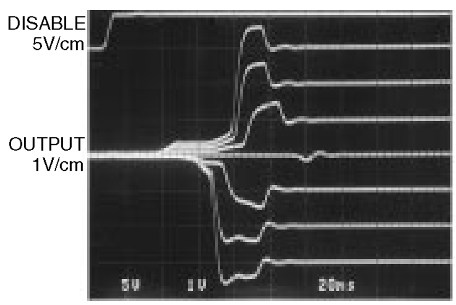
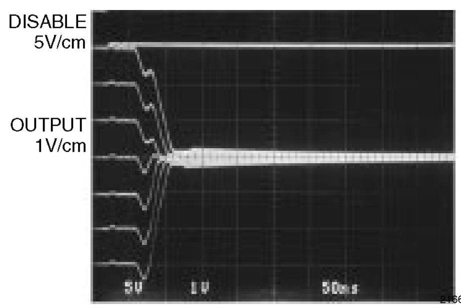
ENABLE Response for a Family of D.C. Inputs



$A_V = +2$, $R_L = 150$, $V_S = \pm 15V$

2166-8

DISABLE Response for a Family of D.C. Inputs

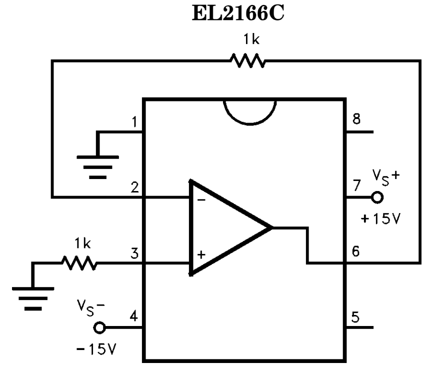


2166-9

$A_V = +2$, $R_L = 150$, $V_S = \pm 15V$

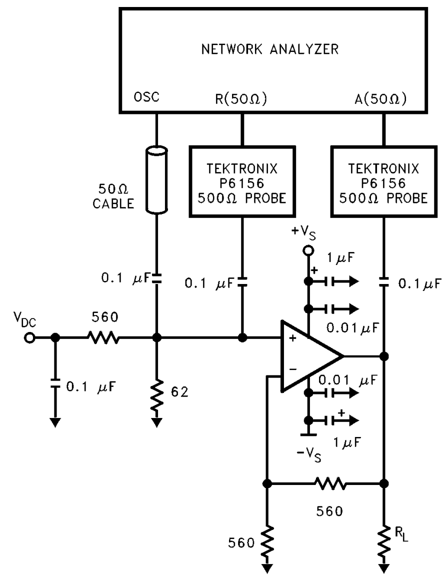
Burn-In Circuit

EL2166C



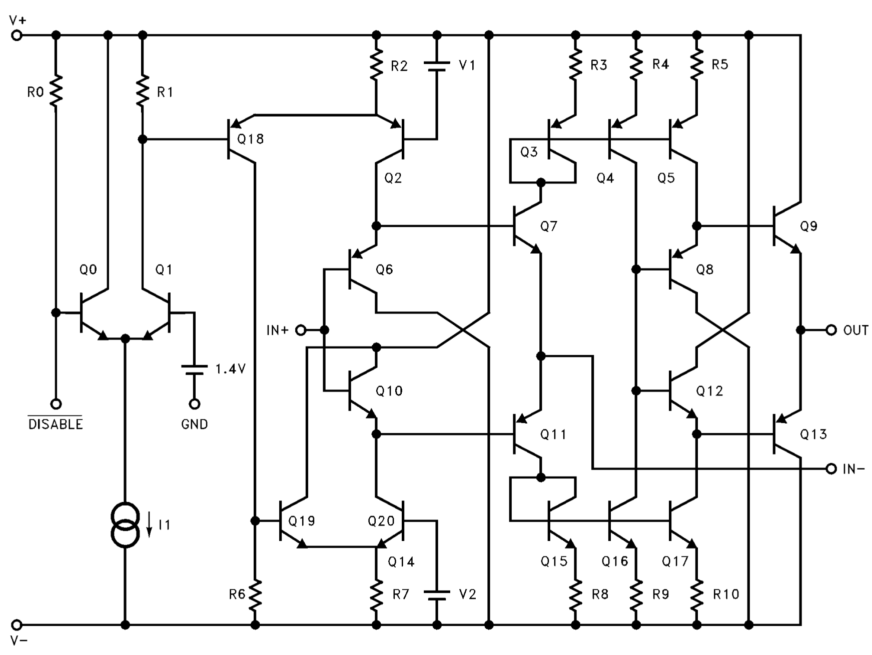
2166-10

Differential Gain and Phase Test Circuit



2166-11

Simplified Schematic



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Applications Information

Product Description

The EL2166C is a current mode feedback amplifier that offers wide bandwidth and good video specifications at a moderately low supply current. It is built using Elantec's proprietary complimentary bipolar process and is offered in industry standard pin-outs. Due to the current feedback architecture, the EL2166C closed-loop 3 dB bandwidth is dependent on the value of the feedback resistor. First the desired bandwidth is selected by choosing the feedback resistor, R_F, and then the gain is set by picking the gain resistor, R_G. The curves at the beginning of the Typical Performance Curves section show the effect of varying both R_F and R_G. The 3 dB bandwidth is only slightly dependent on the power supply voltage. The bandwidth reduces from 110 MHz to 95 MHz as supplies are varied from ±15V to ±5V. To compensate for this, smaller values of feedback resistor can be used at lower supply voltages.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible, below ¼″. The power supply pins must be well bypassed to reduce the risk of oscillation. A 1.0 μF tantalum capacitor in parallel with a 0.01 μF ceramic capacitor is adequate for each supply pin.

For good AC performance, parasitic capacitances should be kept to a minimum, especially at the inverting input (see Capacitance at the Inverting Input section). This implies keeping the ground plane away from this pin. Carbon resistors are acceptable, while use of wire-wound resistors should not be used because of their parasitic inductance. Similarly, capacitors should be low inductance for best performance. Use of sockets, particularly for the SO package, should be avoided. Sockets add parasitic inductance and capacitance which will result in peaking and overshoot.

Capacitance at the Inverting Input

Due to the topology of the current feedback amplifier, stray capacitance at the inverting input will affect the AC and transient performance of the EL2166C when operating in the non-inverting configuration. The characteristic curve of gain vs. frequency with variations of $C_{IN}-$ emphasizes this effect. The curve illustrates how the bandwidth can be extended over 30 MHz with some additional peaking with an additional 5 pF of capacitance at the $V_{IN}-$ pin for the case of $A_V = +2$. Higher values of capacitance will be required to obtain similar effects at higher gains.

In the inverting gain mode, added capacitance at the inverting input has little effect since this point is at a virtual ground and stray capacitance is therefore not "seen" by the amplifier.

Feedback Resistor Values

The EL2166C has been designed and specified with $R_F = 560\Omega$ for $A_V = +2$. This value of feedback resistor yields relatively flat frequency response with <1.5 dB peaking out to 110 MHz. As is the case with all current feedback amplifiers, wider bandwidth, at the expense of slight peaking, can be obtained by reducing the value of the feedback resistor. Inversely, larger values of feedback resistor will cause rolloff to occur at a lower frequency. By reducing R_F to 430Ω, bandwidth can be extended to 120 MHz with 4.5 dB of peaking. See the curves in the Typical Performance Curves section which show 3 dB bandwidth and peaking vs. frequency for various feedback resistors and various supply voltages.

Bandwidth vs Temperature

Whereas many amplifier's supply current and consequently 3 dB bandwidth drop off at high temperature, the EL2166C was designed to have little supply current variations with temperature. An immediate benefit from this is that the 3 dB bandwidth does not drop off drastically with temperature. With $V_S = \pm15V$ and $A_V = +2$, the bandwidth only varies from 115 MHz to 95 MHz over the entire die junction temperature range of $0°C < T < 150°C$.

Applications Information — Contd.

Supply Voltage Range

The EL2166C has been designed to operate with supply voltages from ±5V to ±15V. AC performance, including −3 dB bandwidth and differential gain and phase, shows little degradation as the supplies are lowered to ±5V. For example, as supplies are lowered from ±15V to ±5V, −3 dB bandwidth reduces only 15 MHz, and differential gain and phase remain less than 0.05%/0.02° respectively.

If a single supply is desired, values from +10V to +30V can be used as long as the input common mode range is not exceeded. When using a single supply, be sure to either 1) DC bias the inputs at an appropriate common mode voltage and AC couple the signal, or 2) ensure the driving signal is within the common mode range of the EL2166C.

Disable Function

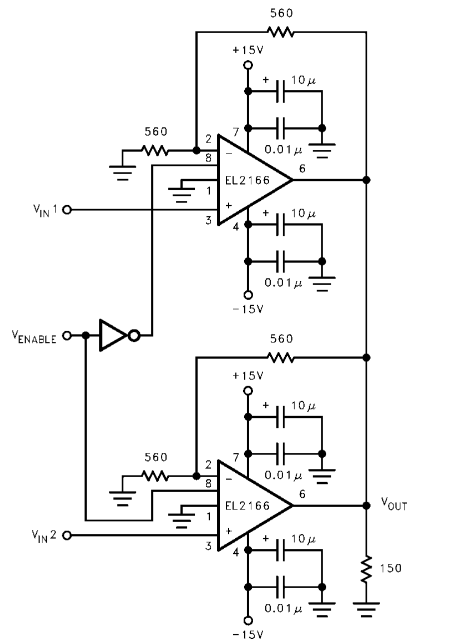
The EL2166C has a superior disable function that has been optimized for video performance. Time to disable/enable is around 75 ns.

During disable, the output of the EL2166C can withstand over 1500 V/μs slew rate signals at its output and the output does not draw excessive currents. The feed-through can be modeled as a 1.5 pF capacitor from $V_{IN}+$ to the output, and the output impedance can be modeled as 4.4 pF in parallel with 180 kΩ to ground when disabled. Consequently, multiplexing with the EL2166C is very easy. Simply tie the outputs of multiple EL2166Cs together and drive the /DISABLE pins with standard TTL or CMOS signals. The disable signal applied to the /DISABLE pin is referenced to the GND pin. The GND pin can be tied as low as the V_{S-} pin. This allows the EL2166C to be operated on a single supply. For example, one could tie the V_{S-} and GND pins to 0V and V_{S+} to +10V, and then use standard TTL or CMOS to drive the /DISABLE pin. Remember to keep the inputs of the EL2166C within their common mode range.

Multiplexing with the EL2166C

An example of multiplexing with the EL2166C and its response curve is shown below. Always be sure that no more than ±5V is applied between $V_{IN}+$ and $V_{IN}-$, which is compatible with standard video signals. This usually becomes an issue only when using the disable feature and amplifying large voltages.

Dual EL2166C Multiplexer



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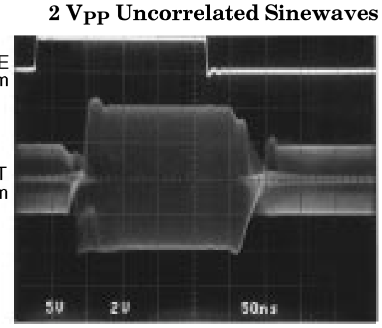
In the multiplexer above, suppose one amp is disabled and the other has amplified a signal to +10V at V_{OUT}. The voltage at pin 2 of the dis-

Dual EL2166C Multiplexer Switching 4 V_{PP} Uncorrelated Sinewaves to 2 V_{PP} Uncorrelated Sinewaves

V_{ENABLE} 5V/cm

V_{OUT} 2V/cm



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Applications Information — Contd.

abled amplifier will now be +5V due to the resistor divider action. Therefore, any applied voltage at pin 3 of the disabled amplifier must remain above 0V if the voltage between pins 2 and 3 of the disabled amplifier is to remain less than 5V. Also keep in mind that each disabled amplifier adds more capacitance to the bus, as discussed above. See Disable Function, and Driving Cables and Capacitive Loads in this section, and the Frequency Response for Various C_L curves in the Typical Performance Curve section.

Settling Characteristics

The EL2166C offers superb settling characteristics to 0.1%, typically in the 35 ns to 40 ns range. There are no aberrations created from the input stage which often cause longer settling times in other current feedback amplifiers. The EL2166C is not slew rate limited, therefore any size step up to ±10V gives approximately the same settling time.

As can be seen from the Long Term Settling Error curve, for $A_V = +1$, there is approximately a 0.02% residual which tails away to 0.01% in about 20 μs. This is a thermal settling error caused by a power dissipation differential (before and after the voltage step). For $A_V = -1$, due to the inverting mode configuration, this tail does not appear since the input stage does not experience the large voltage change as in the non-inverting mode. With $A_V = -1$, 0.01% settling time is slightly greater than 100 ns.

Power Dissipation

The EL2166C amplifier combines both high speed and large output current drive capability at a moderate supply current in very small packages. It is possible to exceed the maximum junction temperature allowed under certain supply voltage, temperature, and loading conditions. To ensure that the EL2166C remains within its absolute maximum ratings, the following discussion will help to avoid exceeding the maximum junction temperature.

The maximum power dissipation allowed in a package is determined by its thermal resistance and the amount of temperature rise according to

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}}$$

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage plus the power in the IC due to the load, or

$$P_{DMAX} = 2 * V_S * I_S + (V_S - V_{OUT}) * \frac{V_{OUT}}{R_L}$$

where I_S is the supply current. (To be more accurate, the quiescent supply current flowing in the output driver transistor should be subtracted from the first term because, under loading and due to the class AB nature of the output stage, the output driver current is now included in the second term.)

In general, an amplifier's AC performance degrades at higher operating temperature and lower supply current. Unlike some amplifiers, the EL2166C maintains almost constant supply current over temperature so that AC performance is not degraded as much over the entire operating temperature range. Of course, this increase in performance doesn't come for free. Since the current has increased, supply voltages must be limited so that maximum power ratings are not exceeded.

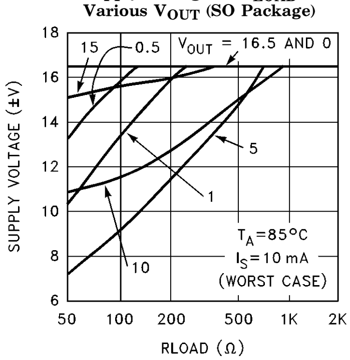
The EL2166C consumes typically 7.5 mA and maximum 10.0 mA. The worst case power in an IC occurs when the output voltage is at half supply, if it can go that far, or its maximum values if it cannot reach half supply. If we set the two P_{DMAX} equations equal to each other, and solve for V_S, we can get a family of curves for various loads and output voltages according to:

$$V_S = \frac{\frac{R_L * (T_{JMAX} - T_{AMAX})}{\theta_{JA}} + (V_{OUT})^2}{(2 * I_S * R_L) + V_{OUT}}$$

Applications Information — Contd.

The following curves show supply voltage ($\pm V_S$) vs R_{LOAD} for various output voltage swings for the 2 different packages. The curves assume worst case conditions of $T_A = +85°C$ and $I_S = 10$ mA.

Supply Voltage vs R_{LOAD} for Various V_{OUT} (SO Package)



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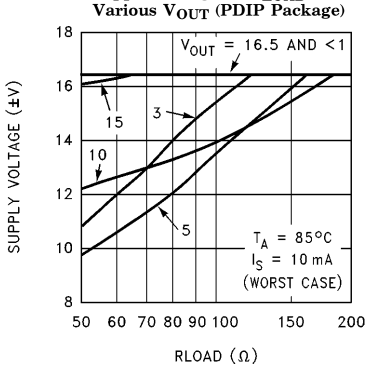
Supply Voltage vs R_{LOAD} for Various V_{OUT} (PDIP Package)



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The curves do not include heat removal or forcing air, or the simple fact that the package will probably be attached to a circuit board, which can also provide some form of heat removal. Larger temperature and voltage ranges are possible with heat removal and forcing air past the part.

Current Limit

The EL2166C has an internal current limit that protects the circuit in the event of the output being shorted to ground. This limit is set at 80 mA nominally and reduces with junction temperature. At a junction temperature of 150°C, the current limits at about 50 mA. If the output is shorted to ground, the power dissipation could be well over 1W. Heat removal is required in order for the EL2166C to survive an indefinite short.

Driving Cables and Capacitive Loads

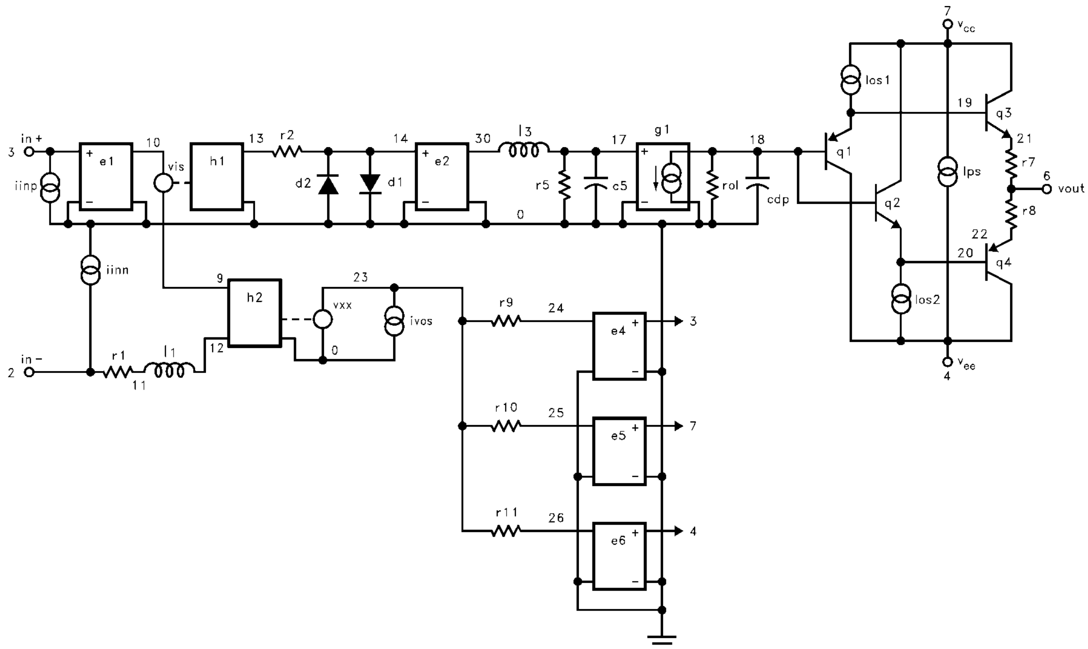
When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back termination series resistor will decouple the EL2166C from the capacitive cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without termination resistors. In these applications, an additional small value (5Ω–50Ω) resistor in series with the output will eliminate most peaking. The gain resistor, R_G, can be chosen to make up for the gain loss created by this additional series resistor at the output.

EL2166C Macromodel

```
* Revision A, May 1994
* AC Characteristics used CIN- (pin 2) = 1 pF; RF = 560Ω
* Connections:          +input
*                         |    -input
*                         |      |    +Vsupply
*                         |      |      |    -Vsupply
*                         |      |      |      |    output
*                         |      |      |      |      |
.subckt EL2166C/EL        3      2      7      4      6
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 130
l1 11 12 25nH
iinp 3 0 0.5µA
iinm 2 0 5µA
r12 3 0 2Meg
*
* Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
*
*e2 30 0 14 0 0.00166666666
l3 30 17 0.8µH
c5 17 0 1.25pF
r5 17 0 500
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
ro1 18 0 2Meg
cdp 18 0 2.9pF
*
* Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 4
r8 22 6 4
ios1 7 19 2mA
ios2 20 4 2mA
*
* Supply Current
*
ips 7 4 2mA
*
* Error Terms
*
ivos 0 23 2mA
vxx 23 0 0V
e4 24 0 3 0 1.35K
e5 25 0 7 0 1.0
e6 26 0 4 0 1.0
r9 24 23 562
r10 25 23 1K
r11 26 23 1K
*
* Models
*
.model qn npn (is=5e-15 bf=200 tf=0.1ns)
.model qp pnp (is=5e-15 bf=200 tf=0.1ns)
.model dclamp d (is=1e-30 ibv=0.266 bv=2.8 n=4)
.ends
```

TAB WIDE
TD is 2.6in
TD is 6.5in

EL2166C Macromodel — Contd.



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EL2166C

110 MHz Current Feedback Amplifier with Disable

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