DG408/883, DG409/883

Single 8-Channel/Differential 4-Channel CMOS Analog Multiplexers

June 1994

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **ON-Resistance 100Ω Maximum (+25°C)**
- **Low Power Consumption (P_D <11mW)**
- **Fast Switching Action**
  - **t_{TRANS} <250ns**
  - **$t_{ON/OFF(EN)}$ <150ns**
- **Low Charge Injection**
- **Upgrade from DG508A/DG509A**
- **TTL, CMOS Compatible**
- **Single or Split Supply Operation**

Applications

- **Data Acquisition Systems**
- **Audio Switching Systems**
- **Automatic Testers**
- **Hi-Rel Systems**
- **Sample and Hold Circuits**
- **Communication Systems**
- **Analog Selector Switch**

Description

The DG408/883 Single 8-Channel and DG409/883 Differential 4-Channel monolithic CMOS analog multiplexers are drop-in replacements for the popular DG508A and DG509A series devices. They each include an array of eight analog switches, a TTL/CMOS compatible digital decode circuit for channel selection, a voltage reference for logic thresholds and an ENABLE input for device selection when several multiplexers are present.

The DG408/883 and DG409/883 feature lower signal ON resistance (<100Ω) and faster switch transition time (t_{TRANS} <250ns) compared to the DG508A or DG509A. Charge injection has been reduced, simplifying sample and hold applications. The improvements in the DG408/883 series are made possible by using a high-voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. Power supplies may be single-ended from +5V to +34V, or split from ±5V to ±20V.

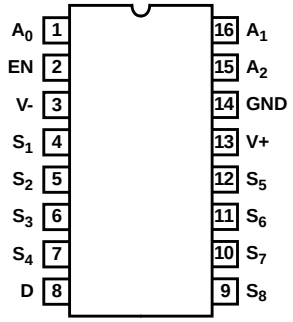
The analog switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a ±5V analog input range.

Ordering Information

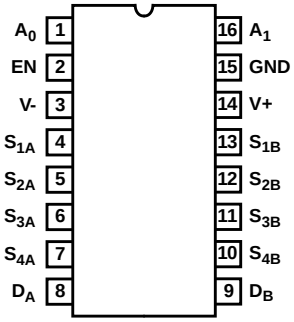
PART NUMBER	TEMPERATURE RANGE	PACKAGE
DG408AK/883	-55°C to +125°C	16 Lead CerDIP
DG409AK/883	-55°C to +125°C	16 Lead CerDIP

Pinouts

DG408/883
(CERDIP)
TOP VIEW

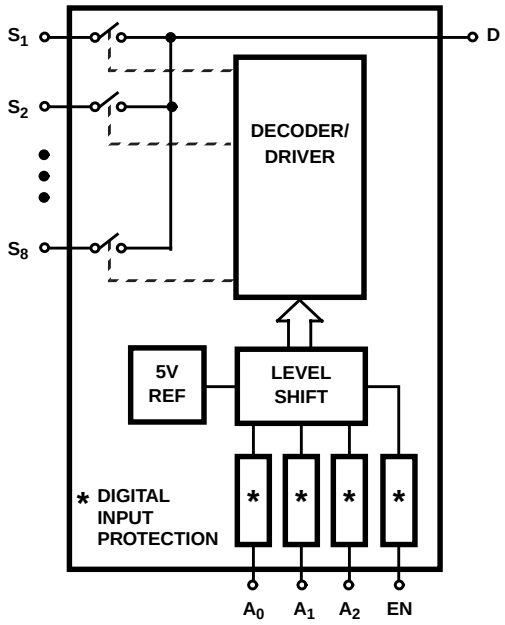


DG409/883
(CERDIP)
TOP VIEW

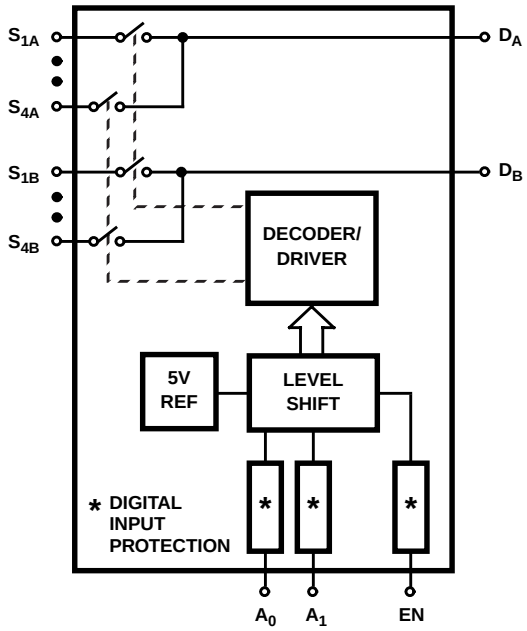


Functional Block Diagrams

DG408/883



DG409/883



Pin Description - (DG408/883)

PIN	SYMBOL	DESCRIPTION
1	A_0	Logic Decode Input (Bit 0, LSB)
2	EN	Enable Input
3	V-	Negative Power Supply Terminal
4	S_1	Source (Input) for Channel 1
5	S_2	Source (Input) for Channel 2
6	S_3	Source (Input) for Channel 3
7	S_4	Source (Input) for Channel 4
8	D	Drain (Output)
9	S_8	Source (Input) for Channel 8
10	S_7	Source (Input) for Channel 7
11	S_6	Source (Input) for Channel 6
12	S_5	Source (Input) for Channel 5
13	V+	Positive Power Supply Terminal (Substrate)
14	GND	Ground Terminal (Logic Common)
15	A_2	Logic Decode Input (Bit 2, MSB)
16	A_1	Logic Decode Input (Bit 1)

Pin Description - (DG409/883)

PIN	SYMBOL	DESCRIPTION
1	A_0	Logic Decode Input (Bit 0, LSB)
2	EN	Enable Input
3	V-	NegAtive Power Supply Terminal
4	S_{1A}	Source (Input) for Channel 1A
5	S_{2A}	Source (Input) for Channel 2A
6	S_{3A}	Source (Input) for Channel 3A
7	S_{4A}	Source (Input) for Channel 4A
8	D_A	Drain A (Output A)
9	D_B	Drain B (Output B)
10	S_{4B}	Source (Input) for Channel 4B
11	S_{3B}	Source (Input) for Channel 3B
12	S_{2B}	Source (Input) for Channel 2B
13	S_{1B}	Source (Input) for Channel 1B
14	V+	Positive Power Supply Terminal
15	GND	Ground Terminal (Logic Common)
16	A_1	Logic Decode Input (Bit 1, MSB))

TRUTH TABLE DG408/883

A_2	A_1	A_0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

TRUTH TABLE DG409/883

A_1	A_0	EN	ON SWITCH
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

NOTES:

1. V_{AH} Logic “1” ≥2.4V.
2. V_{AL} Logic “0” ≤0.8V.

Absolute Maximum Ratings

V+ to V- . . . . . +44.0V
GND to V- 25V
Digital Inputs (Note 1) . . . . . (V-) -2V to (V+) + 2V or 20mA, Whichever Occurs First
Current (Any Terminal, Except S or D) 30mA
Continuous Current, S or D 20mA
Peak Current, S or D 40mA
(Pulsed 1ms, 10% Duty Cycle)
Storage Temperature Range . . . . . -65^oC to $+125^oC$
Lead Temperature (Soldering, 10s) . . . . . $+300^oC$

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
CerDIP Package	$70^oC/W$	$20^oC/W$

Operating Temperature . . . . . -55^oC to $+125^oC$
Junction Temperature . . . . . $+175^oC$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $-55^oC \le T_A \le +125^oC$, V+ = +15V, V- = -15V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Drain-Source ON Resistance	$r_{DS(ON)}$	$V_D = \pm10V$, $V_{AL} = 0.8V$, $V_{AH} = 2.4V$, $I_S = -10mA$, Sequence Each Switch On	1, 3	$+25^oC$, -55^oC	-	100	Ω
			2	$+125^oC$	-	125	Ω
Difference In Drain-Source ON Resistance Between Channels	$\Delta r_{DS(ON)}$	$V_D = \pm10V$, $V_{AL} = 0.8V$, $V_{AH} = 2.4V$, $I_S = -10mA$, (Note 2)	1	$+25^oC$	-	15	Ω
Source OFF Leakage Current	$I_{S(OFF)}$	$V_S = \pm10V$, $V_D = \mp10V$, $V_{EN} = 0V$	1	$+25^oC$	-0.5	+0.5	nA
			2	$+125^oC$	-50	+50	nA
Drain OFF Leakage Current DG408/883	$I_{D(OFF)}$	$V_S = \pm10V$, $V_D = \mp10V$, $V_{EN} = 0V$	1	$+25^oC$	-1	+1	nA
			2	$+125^oC$	-200	+200	nA
DG409/883			1	$+25^oC$	-1	+1	nA
			2	$+125^oC$	-100	+100	nA
Drain ON Leakage Current DG408/883	$I_{D(ON)}$	$V_S = V_D = \pm10V$, $V_{AL} = 0.8V$, $V_{AH} = 2.4V$, $V_{EN} = 2.4V$, Sequence Each Switch On	1	$+25^oC$	-1	+1	nA
			2	$+125^oC$	-200	+200	nA
DG409/883			1	$+25^oC$	-1	+1	nA
			2	$+125^oC$	-150	+150	nA
Logic Input Current, Input Voltage High	I_{AH}	$V_{EN} = 0.8V$, $V_A = 2.4V$	1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-10	+10	µA
		$V_{EN} = 0.8V$, $V_A = 15V$			-10	+10	µA
Logic Input Current, Input Voltage Low	I_{AL}	$V_{EN} = 0V$, $V_A = 0V$	1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-10	+10	µA
		$V_{EN} = 2.4V$, $V_A = 0V$			-10	+10	µA
Positive Supply Current Standby	$I+_{(SB)}$	$V_{EN} = 0V$, $V_A = 0V$	1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-	75	µA

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: $-55^oC \le T_A \le +125^oC$, V+ = +15V, V- = -15V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Negative Supply Current Standby	$I_{-(SB)}$	V_{EN} = 0V, V_A = 0V	1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-75	-	µA
Positive Supply Current	I+	V_{EN} = 2.4V, V_A = 0V	1, 3	$+25^oC$, -55^oC	-	0.5	mA
			2	$+125^oC$	-	2	mA
Negative Supply Current	I-	V_{EN} = 2.4V, V_A = 0V	1, 2, 3	$+25^oC$, $+125^oC$, -55^oC	-0.5	-	mA

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $-55^oC \le T_A \le +125^oC$, V+ = +15V, V- = -15V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Switching Time of Multiplexer	t_{TRANS}		9, 10, 11	$+25^oC$, $+125^oC$, -55^oC	-	250	ns
Enable Turn ON Time	$t_{ON(EN)}$		9, 11	$+25^oC$, -55^oC	-	150	ns
			10	$+125^oC$	-	225	ns
Enable Turn OFF Time	$t_{OFF(EN)}$		9, 10, 11	$+25^oC$, $+125^oC$, -55^oC	-	150	ns
Break-Before-Make Interval	t_{OPEN}		9	$+25^oC$	10	-	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Table 3 Intentionally Left Blank.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 AND 2)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1 (Note 3), 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C and D Endpoints	1

NOTES:

1. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. $\Delta r_{DS(ON)} = r_{DS(ON)}$ MAX - $r_{DS(ON)}$ MIN.
3. PDA applies to Subgroup 1 only.

Die Characteristics

DIE DIMENSIONS:
1800µm x 3320µm x 485 ± 25µm

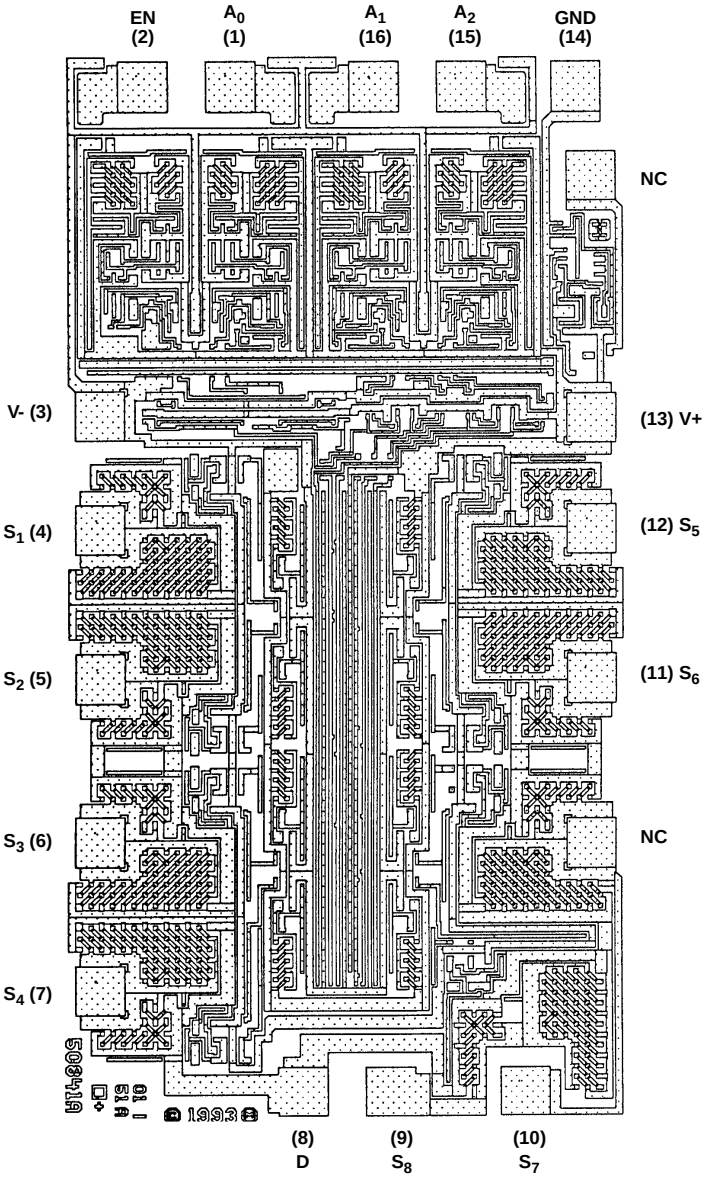
METALLIZATION:
Type: SiAl
Thickness: 12kÅ ± 1kÅ

GLASSIVATION:
Type: Nitride
Thickness: 8kÅ ± 1kÅ

WORST CASE CURRENT DENSITY:
9.1×10^4 A/cm^2

Metallization Mask Layout

DG408/883



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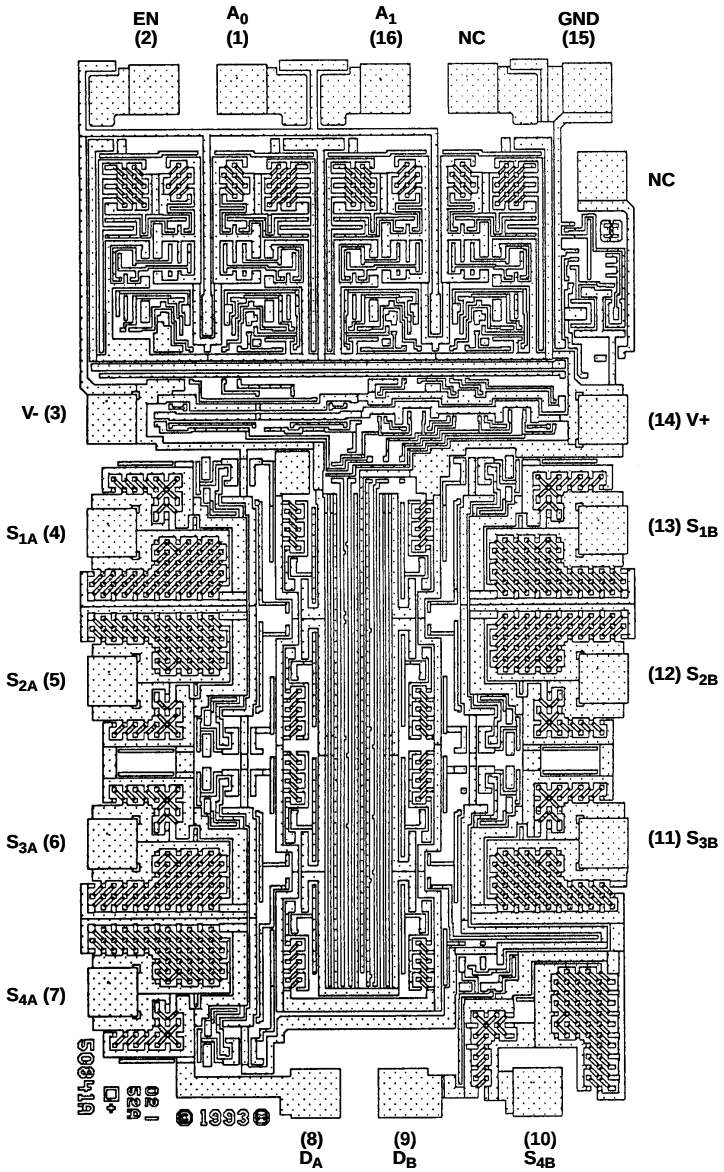
Metallization Mask Layout

DG409/883



Test Circuits

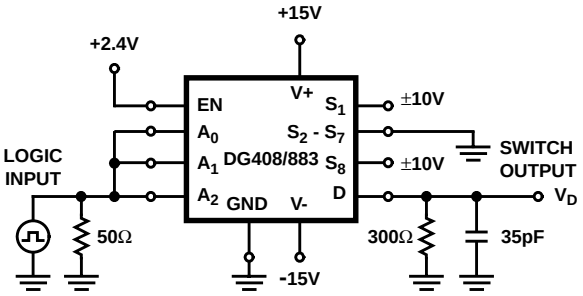


FIGURE 1A.

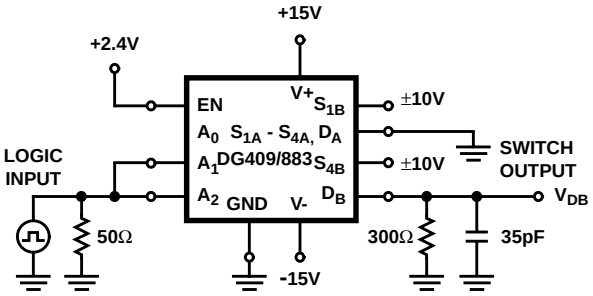


FIGURE 1B.

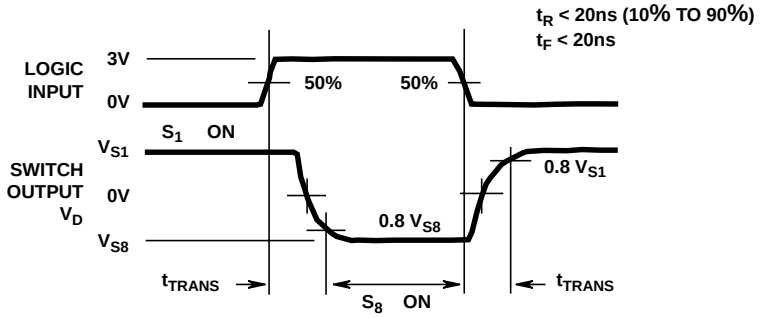


FIGURE 1C.

FIGURE 1. TRANSITION TIME

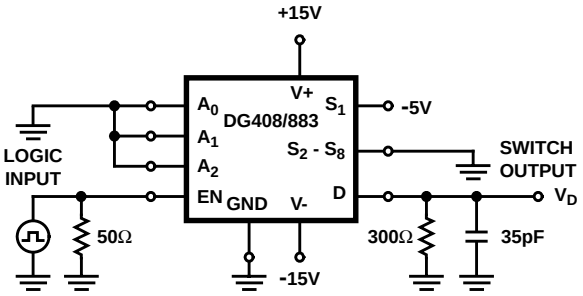


FIGURE 2A.

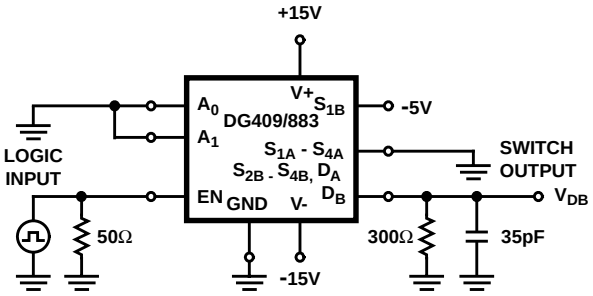


FIGURE 2B.

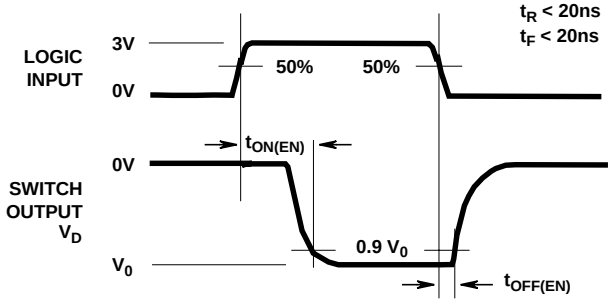


FIGURE 2C.

FIGURE 2. $t_{ON(EN)}$, $t_{OFF(EN)}$

Test Circuits (Continued)

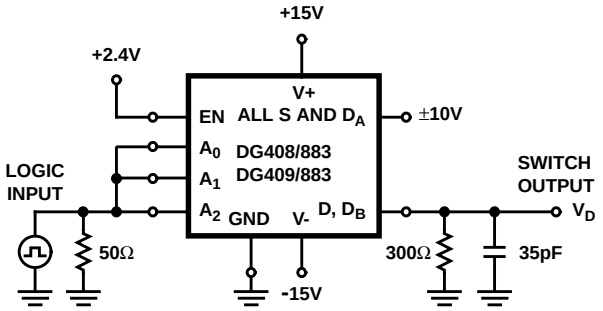


FIGURE 3A.

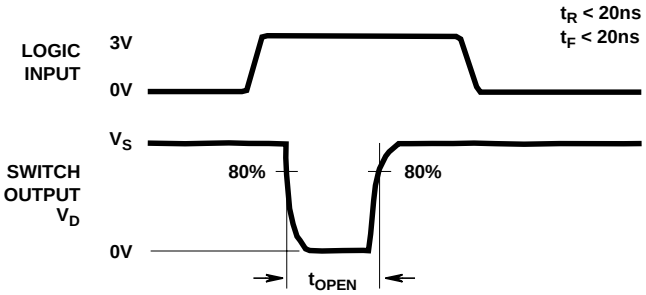
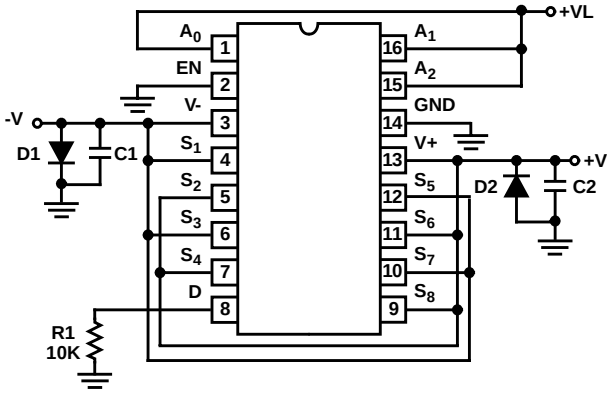


FIGURE 3B.

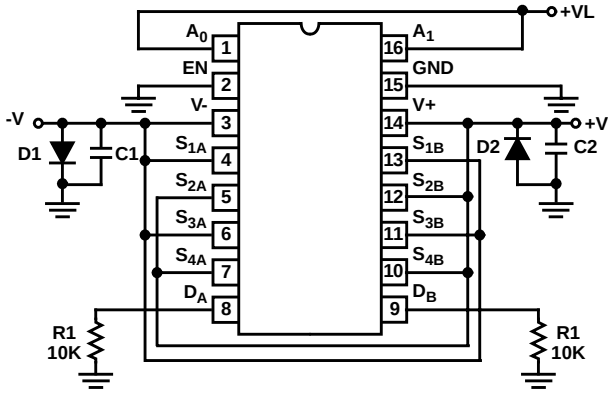
FIGURE 3. BREAK-BEFORE-MAKE INTERVAL

Burn-In Circuits

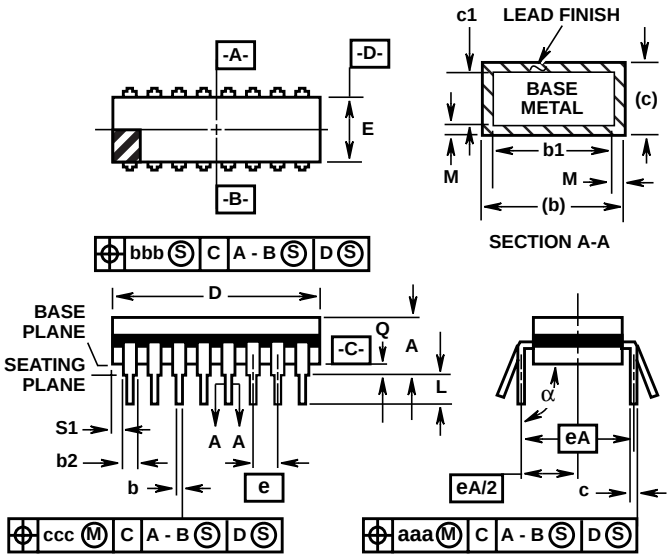
DG408/883



DG409/883



Ceramic Dual-In-Line Frit Seal Packages (CerDIP)



F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

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NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

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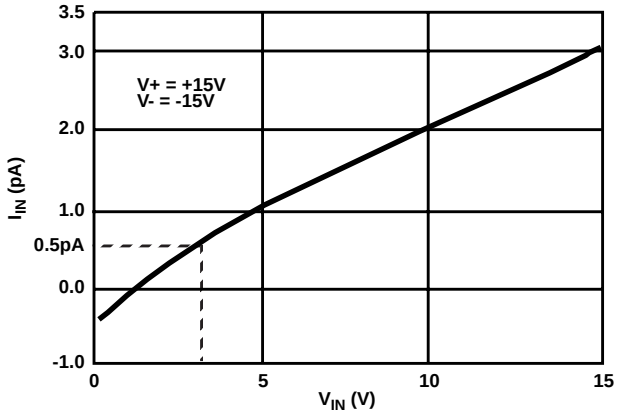
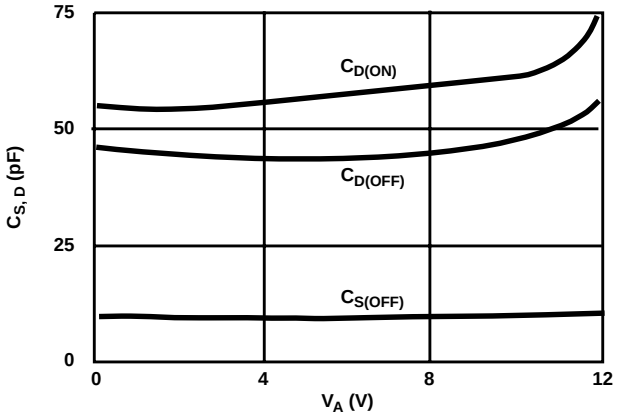
Typical Performance Curves

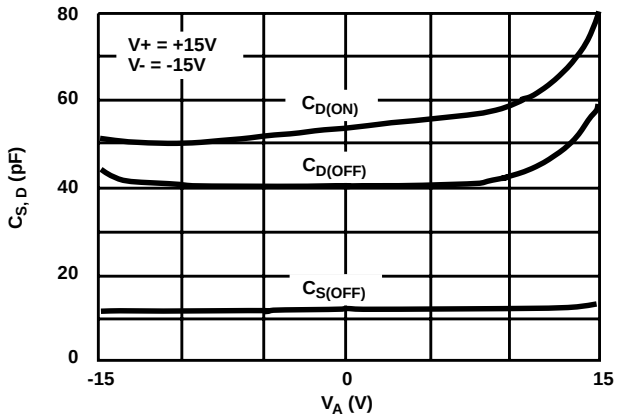
INPUT LOGIC CURRENT vs LOGIC INPUT VOLTAGE



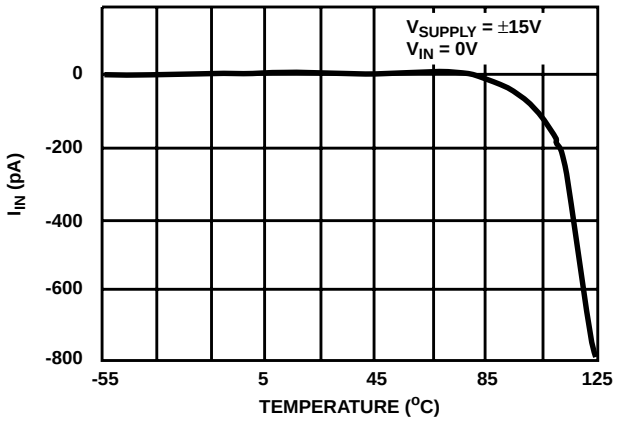
SOURCE/DRAIN CAPACITANCE vs ANALOG VOLTAGE (SINGLE 12V SUPPLY)



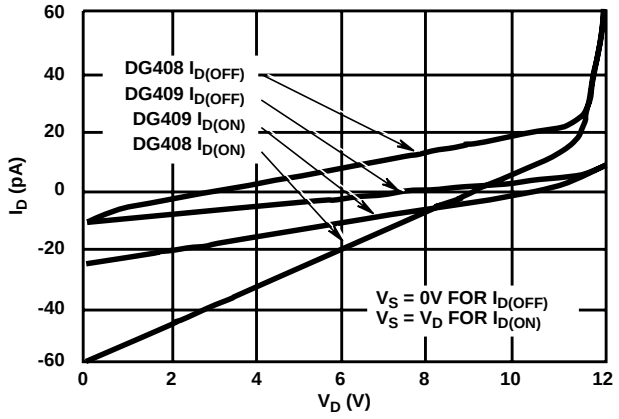
SOURCE/DRAIN CAPACITANCE vs ANALOG VOLTAGE



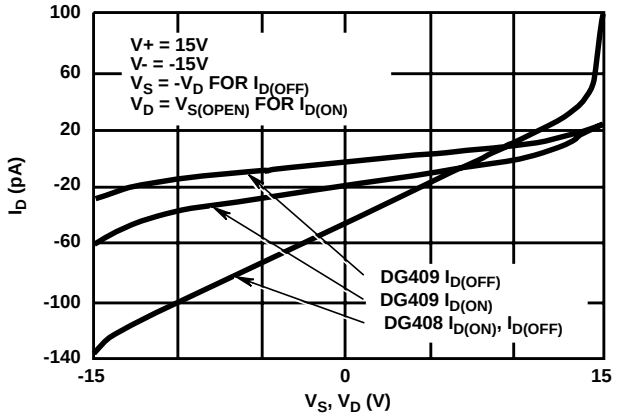
LOGIC INPUT CURRENT vs TEMPERATURE



DRAIN LEAKAGE CURRENT vs SOURCE/DRAIN VOLTAGE (SINGLE 12V SUPPLY)



DRAIN LEAKAGE CURRENT vs SOURCE/DRAIN VOLTAGE



DESIGN INFORMATION (Continued)

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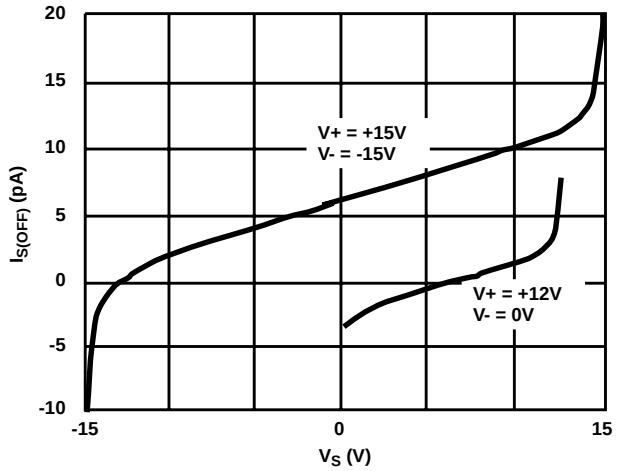
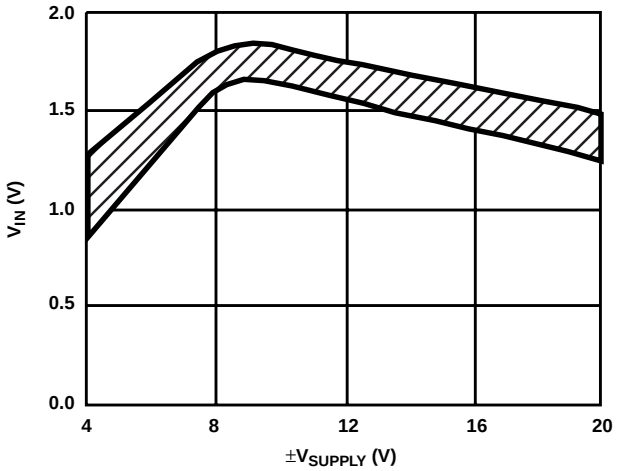
Typical Performance Curves (Continued)

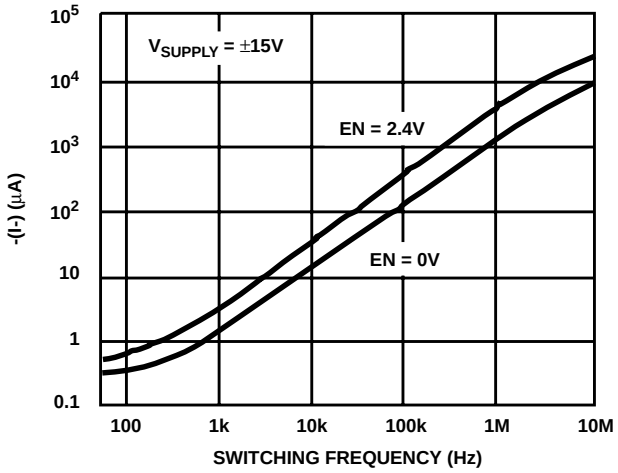
SOURCE LEAKAGE CURRENT vs SOURCE VOLTAGE



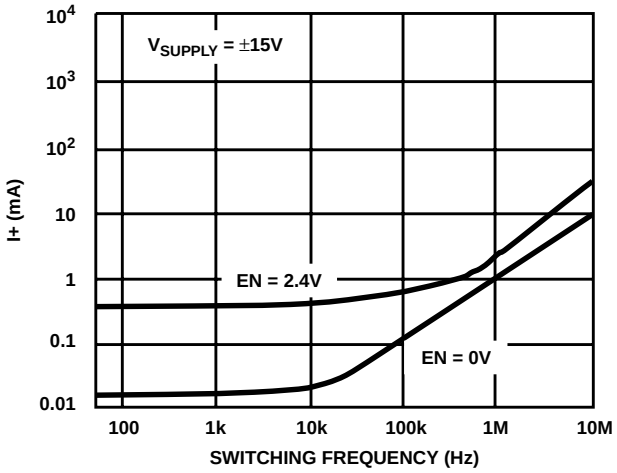
INPUT SWITCHING THRESHOLD vs SUPPLY VOLTAGE



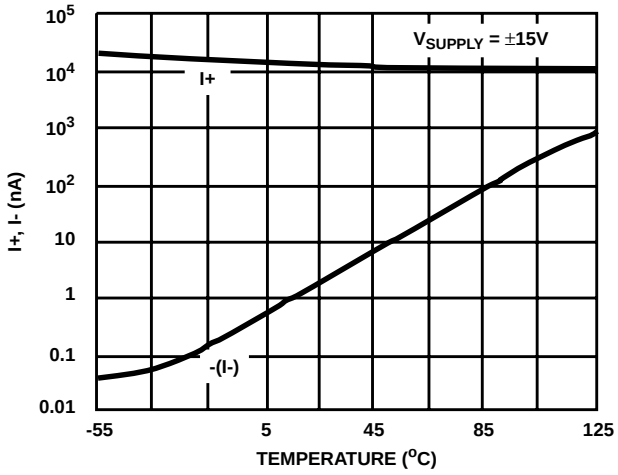
NEGATIVE SUPPLY CURRENT vs SWITCHING FREQUENCY



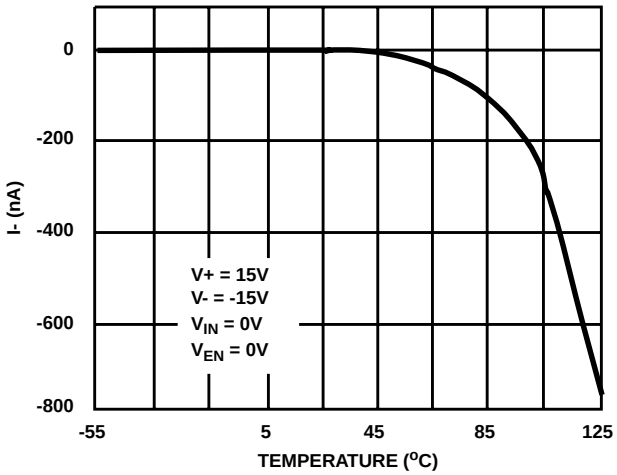
POSITIVE SUPPLY CURRENT vs SWITCHING FREQUENCY



I_{SUPPLY} vs TEMPERATURE (LOG SCALE)



NEGATIVE SUPPLY CURRENT vs TEMPERATURE



DESIGN INFORMATION (Continued)

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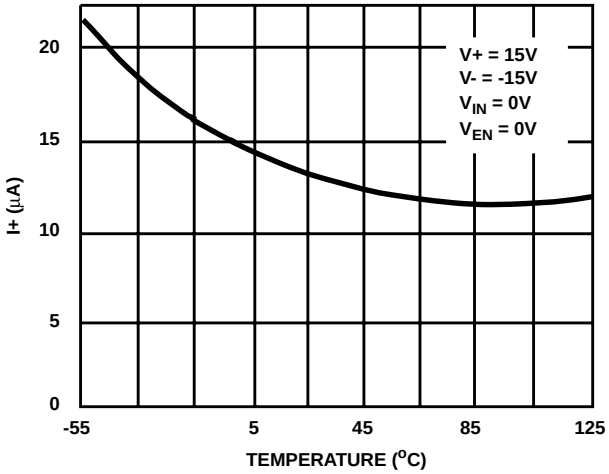
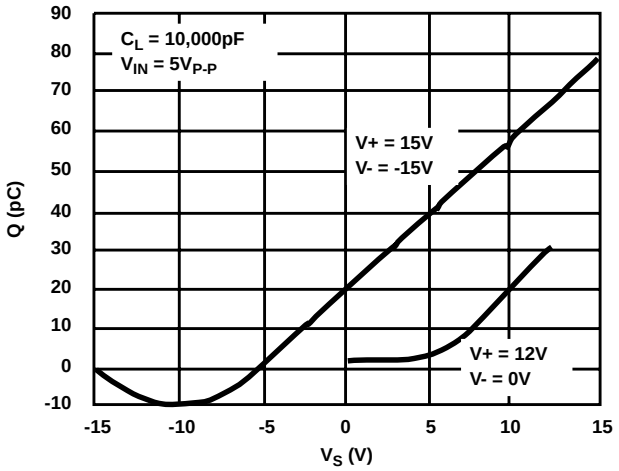
Typical Performance Curves (Continued)

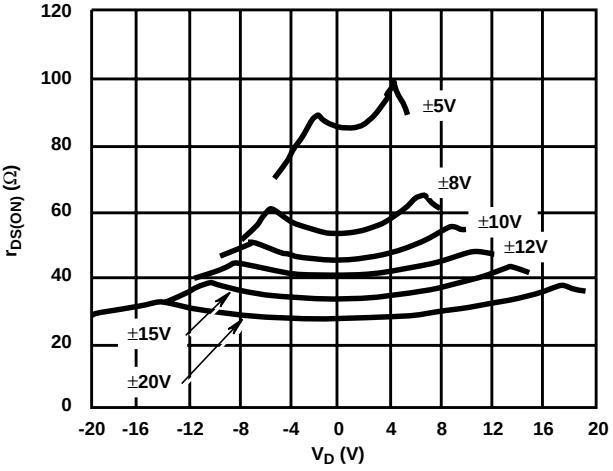
POSITIVE SUPPLY CURRENT vs TEMPERATURE (DG408)



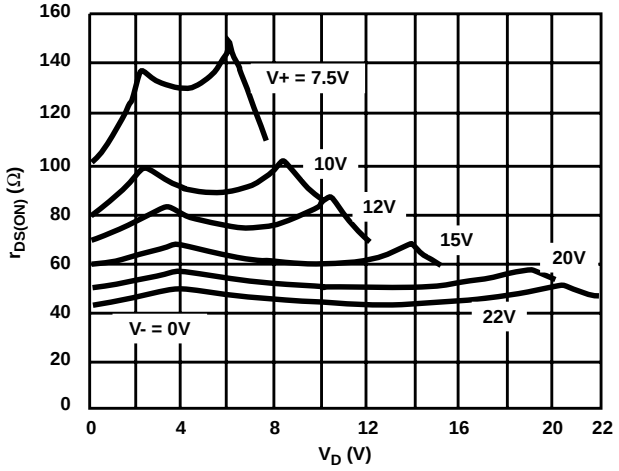
CHARGE INJECTION vs ANALOG VOLTAGE V_S (DG408, DG409)



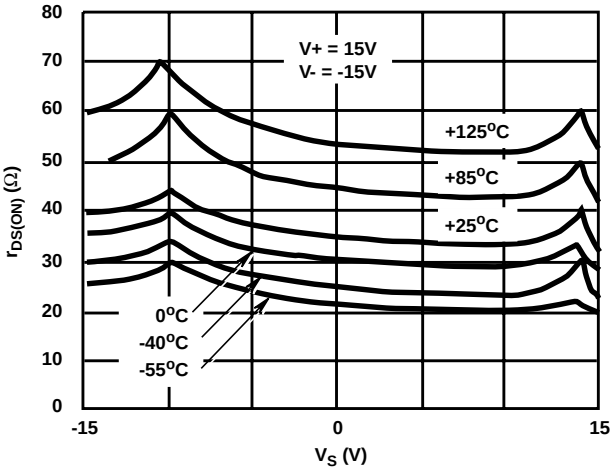
$r_{DS(ON)}$ vs V_D AND SUPPLY



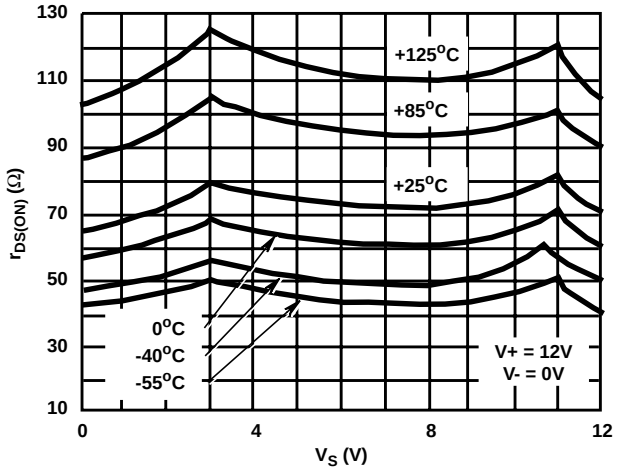
$r_{DS(ON)}$ vs V_D (SINGLE SUPPLY)



$r_{DS(ON)}$ vs V_S AND TEMPERATURE



$r_{DS(ON)}$ vs V_S AND TEMPERATURE (SINGLE SUPPLY)



DESIGN INFORMATION (Continued)

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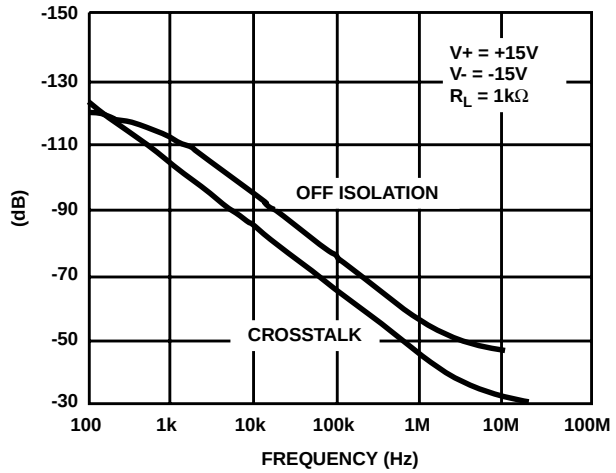
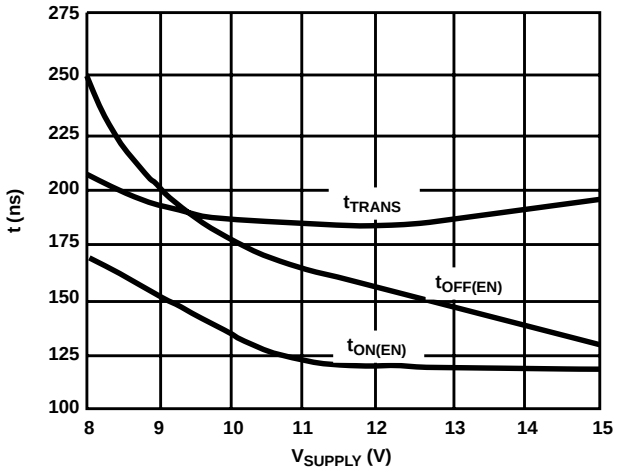
Typical Performance Curves (Continued)

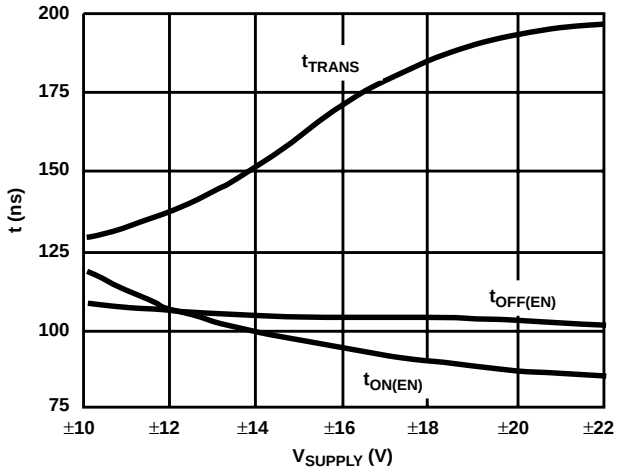
OFF ISOLATION AND CROSSTALK vs FREQUENCY



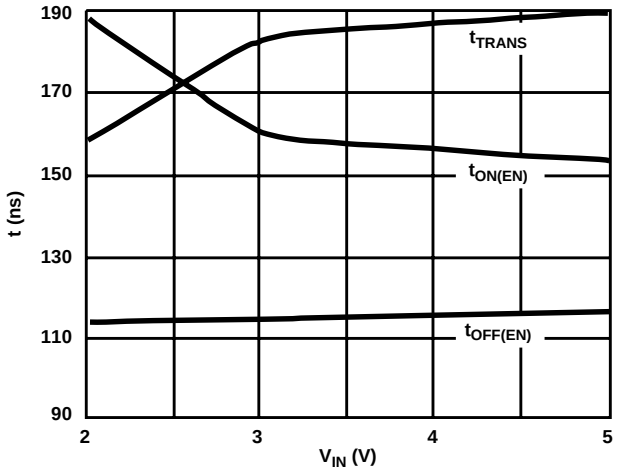
SWITCHING TIME vs SINGLE SUPPLY



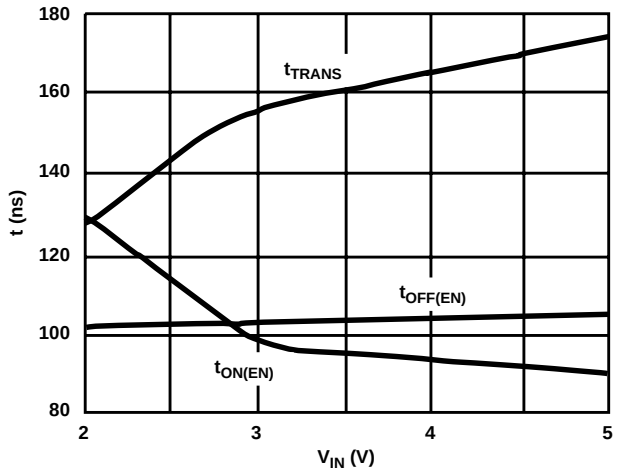
SWITCHING TIME vs BIPOLAR SUPPLY



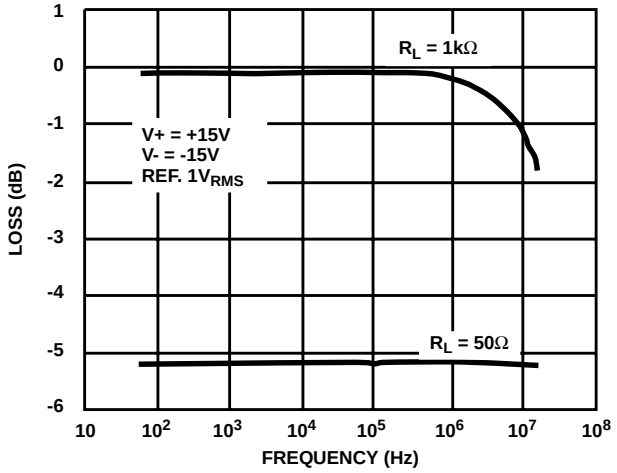
SWITCHING TIME vs V_{IN} (SINGLE SUPPLY)



SWITCHING TIME vs V_{IN} (BIPOLAR SUPPLY)



INSERTION LOSS vs FREQUENCY



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