

QuickSwitch® Products

High-Speed CMOS 12-Bit 2:1 Mux/Demux Switch With Resistor Termination on the Demux Side

QS316292
QS3162292

FEATURES/BENEFITS

- Enhanced N channel FET with no inherent diode to V_{CC}
- 50Ω bidirectional switches connect inputs to outputs
- Zero propagation delay, zero ground bounce
- TTL-compatible input and output levels
- Undershoot Clamp diodes on all switch and control inputs
- Available in 56-pin SSOP and TSSOP

DESCRIPTION

The QS316292 and QS3162292 are high-speed CMOS 12-Bit 2:1 Multiplexer/Demultiplexer switches with a 500Ω resistor termination to GND on the Demultiplexer side to eliminate floating nodes. The QS316292 adds a 25Ω series damping resistor to minimize undershoot, reflection noise, and charge sharing effects. The low ON resistance of the QS316292 allows inputs to be connected to outputs without adding propagation delay and without generating additional ground bounce noise.

APPLICATIONS

- Resource sharing
- Hot-docking (Application Note AN-13)
- Voltage translation (5V to 3.3V; Application Note AN-11)

Figure 1. Functional Block Diagram

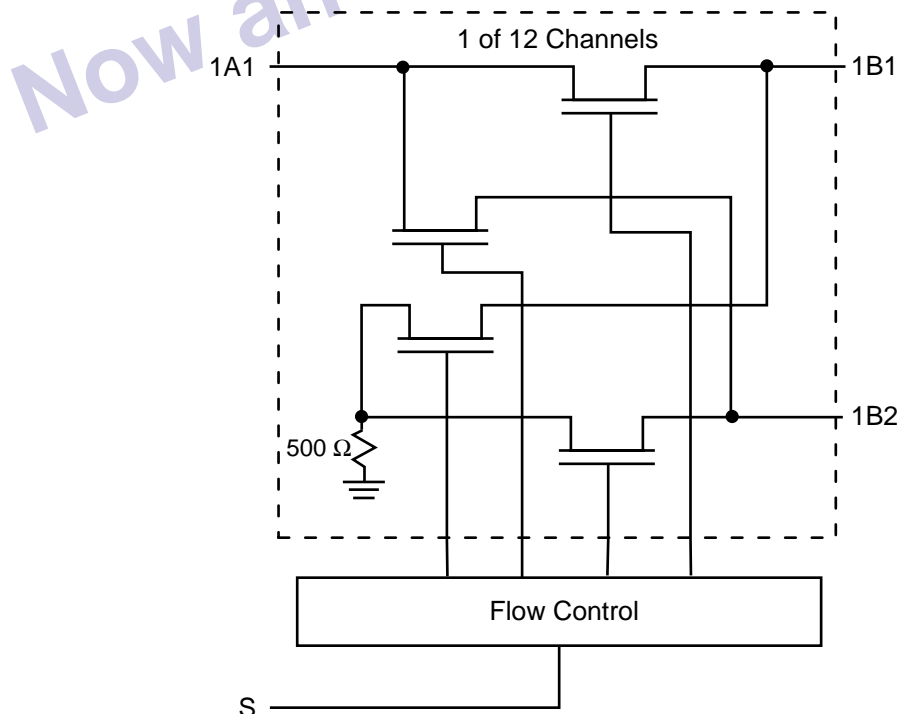


Table 1. Pin Description

Name	I/O	Function
1A1-12A1	I/O	Bus A
1Bn-12Bn	I/O	Bus B
S	I	Data select

Table 2. Function Table

S	iA1	Function
L	iB1	iA1 to iB1, iB2 to GND Via 500Ω
H	iB2	iA1 to iB2, iB1 to GND Via 500Ω

**Figure 2. Pin Configuration
(All Pins Top View)
SSOP (PV)
TSSOP (PA)**

S	1	56	NC
1A1	2	55	NC
NC	3	54	1B1
2A1	4	53	1B2
NC	5	52	2B1
3A1	6	51	2B2
NC	7	50	3B1
GND	8	49	GND
4A1	9	48	3B2
NC	10	47	4B1
5A1	11	46	4B2
NC	12	45	5B1
6A1	13	44	5B2
NC	14	43	6B1
7A1	15	42	6B2
NC	16	41	7B1
V _{CC}	17	40	7B2
8A1	18	39	8B1
GND	19	38	GND
NC	20	37	8B2
9A1	21	36	9B1
NC	22	35	9B2
10A1	23	34	10B1
NC	24	33	10B2
11A1	25	32	11B1
NC	26	31	11B2
12A1	27	30	12B1
NC	28	29	12B2

Table 3. Absolute Maximum Ratings

Supply Voltage to Ground	–0.5V to 7.0V
DC Switch Voltage V _S	–0.5V to 7.0V
DC Input Voltage V _{IN}	–0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20ns)	–3.0V
DC Output Current Max. Sink Current/Pin	120mA
Maximum Power Dissipation At T _A = 85°C, SSOP	0.93 watts
TSSOP	0.77 watts
T _{STG} Storage Temperature	–65° to 150°C

Note: ABSOLUTE MAXIMUM CONTINUOUS RATINGS are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum conditions is not implied.

Table 4. Capacitance

T_A = 25°C, f = 1MHz, V_{IN} = 0V, V_{OUT} = 0V

Pins	SSOP, TSSOP		Unit
	Typ	Max	
Control Inputs	4	5	pF
QuickSwitch Channels (Switch OFF)	7.5	9	pF

Note: Capacitance is guaranteed, but not production tested. For total capacitance while the switch is ON, please see Section 1 under “Input and Switch Capacitance.”

Table 5. DC Electrical Characteristics Over Operating Range

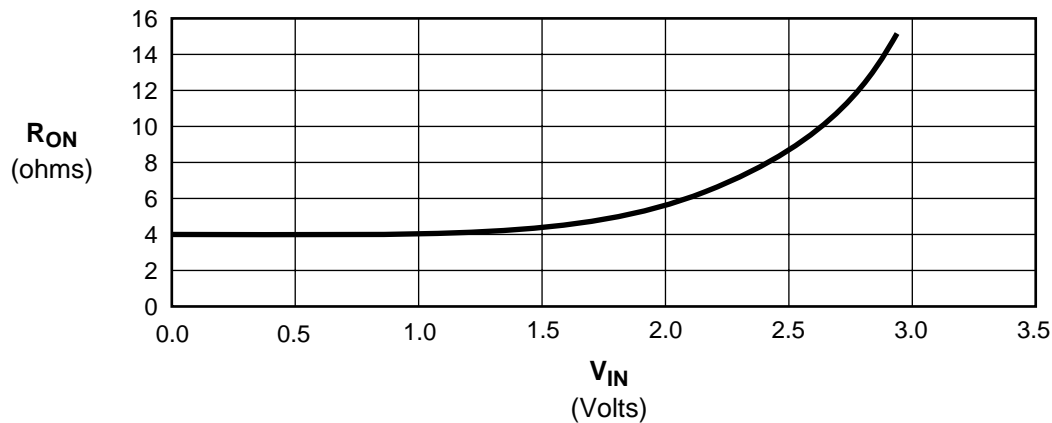
$T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions	Min	Typ ⁽¹⁾	Max	Unit	
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs	2.0	—	—	V	
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs	—	—	0.8	V	
I _{IN}	Input Leakage Current (Control Inputs)	0 ≤ V _{IN} ≤ V _{CC}	—	—	1	μA	
I _{OZ}	Off-State Current (Hi-Z)	0 ≤ V _{OUT} ≤ V _{CC} , Switches OFF	—	—	1	μA	
I _{OS}	Short Circuit Current	A(B) = 0V B(A) = V _{CC}	−100	—	—	mA	
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = −18mA	—	−0.7	−1.2	V	
V _H	Input Hysteresis at Control Pins		—	150	—	mV	
R _{ON}	Switch ON Resistance ⁽²⁾	V _{CC} = Min., V _{IN} = 0.0V I _{ON} = 30mA	QS316212	—	4	6	Ω
			QS3162212	20	28	40	
R _{ON}	Switch ON Resistance ⁽²⁾	V _{CC} = Min., V _{IN} = 2.4V I _{ON} = 15mA	QS316212	—	8	12	Ω
			QS3162212	20	35	48	
V _P	Pass Voltage ⁽³⁾	V _{IN} = V _{CC} = 5V, I _{OUT} = −5μA	3.7	4	4.2	V	

Notes:

1. Typical values indicate $V_{CC} = 5.0\text{V}$ and $T_A = 25^{\circ}\text{C}$.
2. For a diagram explaining the procedure for R_{ON} measurement, please see Section 1 under "DC Electrical Characteristics." Max. value of R_{ON} guaranteed, but not production tested.
3. Pass voltage is guaranteed, but not production tested.

Figure 3. Typical ON Resistance vs. V_{IN} at $V_{CC} = 5.0\text{V}$ (QS316292)



Note: For QS3162292, add 23Ω to R_{ON} shown.

Table 6. Power Supply Characteristics Over Operating Range

$T_A = -40^\circ\text{C}$ to 85°C , $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾	Typ	Max	Unit
I_{CCQ}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$, $V_{IN} = \text{GND}$ or V_{CC} , $f = 0$	0.1	3.0	μA
ΔI_{CC}	Power Supply Current Per Control Input HIGH ⁽²⁾	$V_{CC} = \text{Max.}$, $V_{IN} = 3.4\text{V}$, $f = 0$	—	1.5	mA
Q_{CCD}	Dynamic Power Supply Current Per MHz ⁽³⁾	$V_{CC} = \text{Max.}$, A and B Pins Open, Control Input Toggling @ 50% Duty Cycle	—	0.25	mA/MHz

Notes:

1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input ($V_{IN} = 3.4\text{V}$). A and B pins do not contribute to ΔI_{CC} .
3. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is guaranteed, but not production tested.

Table 7. Switching Characteristics Over Operating Range

$T_A = -40^\circ\text{C}$ to 85°C , $V_{CC} = 5.0\text{V} \pm 10\%$

$C_{LOAD} = 50\text{pF}$, $R_{LOAD} = 500\Omega$ unless otherwise noted.

Symbol	Description ⁽¹⁾		Min	Typ	Max	Unit
t_{PLH}	Data Propagation Delay ^(2,3) iA1 to iBn, iBn to iA1	QS316292	—	—	0.25	ns
t_{PHL}		QS3162292	—	—	1.25	
t_{PZL}	Switch Turn-on Delay ⁽⁴⁾ S to iA1 or iBn	QS316292	1.5	—	6.5	ns
t_{PZH}		QS3162292	1.5	—	7.5	
t_{PLZ}	Switch Turn-off Delay ⁽²⁾ S to iA1, iBn	QS316292	1.5	—	6.2	ns
t_{PHZ}		QS3162292	1.5	—	6.8	

Notes:

1. See Test Circuit and Waveforms. Minimums guaranteed but not production tested.
2. This parameter is guaranteed, but not production tested.
3. The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25ns for QS316292 and 1.25ns for QS3162292 for $C_L = 50\text{pF}$. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
4. Switch turn-on delay from S to iBn is guaranteed, but not production tested.