

January 1996

Features

- Devices QML Qualified in Accordance with MIL-PRF-38535
- Detailed Electrical and Screening Requirements are Contained in SMD# 5962-96712 and Intersil's QM Plan
- 1.25 Micron Radiation Hardened SOS CMOS
- Total Dose >300K RAD (Si)
- Single Event Upset (SEU) Immunity: <1 x 10⁻¹⁰ Errors/Bit/Day (Typ)
- SEU LET Threshold >100 MEV-cm²/mg
- Dose Rate Upset >10¹¹ RAD (Si)/s, 20ns Pulse
- Dose Rate Survivability >10¹² RAD (Si)/s, 20ns Pulse
- Latch-Up Free Under Any Conditions
- Military Temperature Range -55°C to +125°C
- Significant Power Reduction Compared to ALSTTL Logic
- DC Operating Voltage Range 4.5V to 5.5V
- Input Logic Levels
 - VIL = 0.8V Max
 - VIH = VCC/2 Min
- Input Current ≤ 1μA at VOL, VOH
- Fast Propagation Delay 14ns (Max), 9ns (Typ)

Description

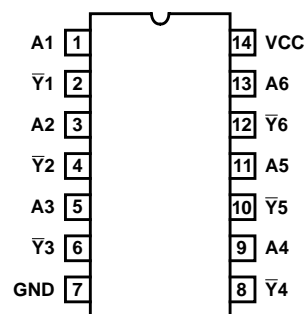
The Intersil ACTS04MS is a Radiation Hardened Hex Inverter.

The ACTS04MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

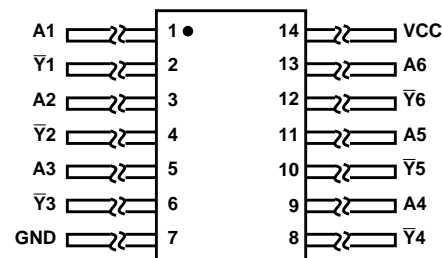
The ACTS04MS is supplied in a 14 lead Ceramic Flatpack (K suffix) or a Ceramic Dual-In-Line Package (D suffix).

Pinouts

14 PIN CERAMIC DUAL-IN-LINE MIL-STD-1835
DESIGNATOR CDIP2-T14, LEAD FINISH C
TOP VIEW



14 PIN CERAMIC FLATPACK MIL-STD-1835
DESIGNATOR CDFP3-F14, LEAD FINISH C
TOP VIEW



TRUTH TABLE

INPUTS	OUTPUTS
An	Yn
L	H
H	L

NOTE: L = Logic Level Low, H = Logic level High

Functional Diagram



Ordering Information

PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
5962F9671201VCC	-55°C to +125°C	MIL-PRF-38535 Class V	14 Lead SBDIP
5962F9671201VXC	-55°C to +125°C	MIL-PRF-38535 Class V	14 Lead Ceramic Flatpack
ACTS04D/Sample	25°C	Sample	14 Lead SBDIP
ACTS04K/Sample	25°C	Sample	14 Lead Ceramic Flatpack
ACTS04HMSR	25°C	Die	Die

Die Characteristics

DIE DIMENSIONS:

88 mils x 88 mils
2240mm x 2240mm

METALLIZATION:

Type: AlSi
Metal 1 Thickness: $7.125\text{\AA} \pm 1.125\text{\AA}$
Metal 2 Thickness: $9\text{\AA} \pm 1\text{\AA}$

GLASSIVATION:

Type: SiO₂
Thickness: 8kÅ ± 1kÅ

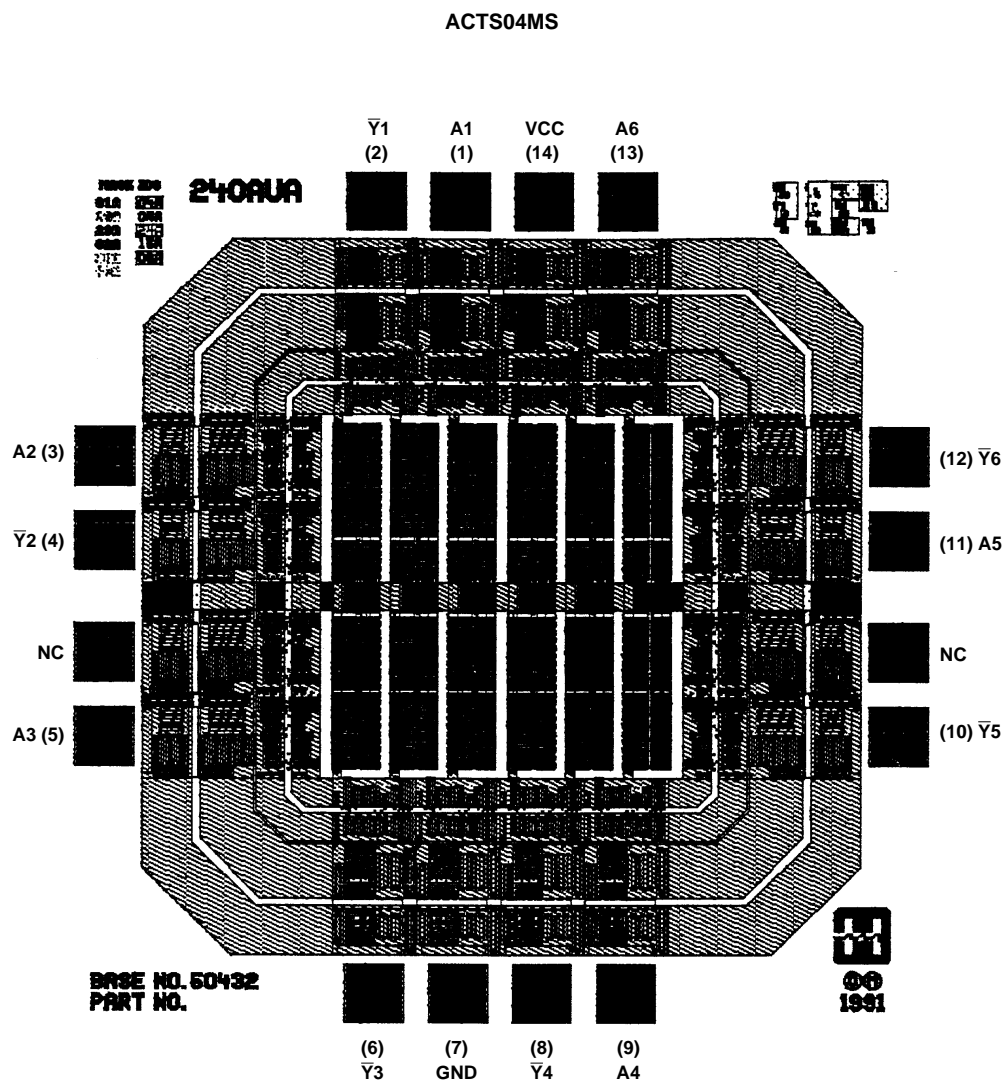
WORST CASE CURRENT DENSITY:

$$< 2.0 \times 10^5 \text{ A/cm}^2$$

BOND PAD SIZE:

4.3 mils x 4.3 mils
> 110µm x 110µm

Metallization Mask Layout



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>

Sales Office Headquarters

NORTH AMERICA

Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE

Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA

Intersil (Taiwan) Ltd.
Taiwan Limited
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029