Design Considerations for ESD Protection Using ESD Protection Diode Arrays

Introduction

As electronic appliances become more pervasive, and with the continuing trend to scale transistor sizes down to pack more performance and functions into a silicon die, Electrostatic Discharge (ESD) protection is becoming a prominent system requirement. California Micro Devices manufactures a family of integrated ESD Protection Diode Arrays which are designed to meet the most stringent ESD requirements in existence today - the IEC-1000-4-2 International Standard for ESD testing. This application note addresses issues that designers should be aware of to derive maximum benefit from employing such ESD Protection Diode Arrays.

The IEC-1000-4-2 ESD Model

The IEC-1000-4-2 ESD model has evolved into the most accepted method of characterizing and testing the ability of electronic equipment to withstand ESD in a controlled environment. In this standard, the ESD pulse is simulated by charging a 150pF capacitor to a high voltage and discharging it through a 330 Ohm resistor into the equipment under test. The discharge can be conducted directly through electrical contact with the test point (contact discharge), or indirectly across an air gap (air discharge). Contact discharge is the preferred test method, since air discharges tend to be unpredictable and are, therefore, not repeatable. The standard also specifies four levels of test severity as outlined in Table 1. Note that there is no implied equivalence between contact and air discharge testing at each level.

Level	Contact Discharge Test Voltage (KV)	Air Discharge Test Voltage (KV)
1	2	2
2	4	4
3	6	8
4	8	15
x[1)]	Special	Special

1) "x" is an open level. The level has to be specified in the dedicated equipment specification. If higher voltages than those shown are specified, special test equipment may be needed.

Table 1: IEC-1000-4-2 Test Levels

ESD Protection Schemes

There are a variety of ways to protect electronic systems from damage by ESD. They range from mechanically "deflecting" the ESD pulse from entering the system by judicious placement of ground shields around user accessible points, to providing alternate shunt paths to dissipate the ESD energy so that it does not damage sensitive internal components. For a detailed discussion on ESD and the various protection schemes that are commonly used, refer to the California Micro Devices Application Note AP-208, "Electro-static Discharge Protection of High Performance Integrated Circuits".

California Micro Devices offers a family of ESD protection diode arrays designed to withstand level-4 contact discharge as defined in the IEC-1000-4-2 standard, as shown in Table 2.

Part Number	Number of Channels	Typical Loading Capacitance @ 2.5V
PACDN004	2	3.5 pF
PACDN006	6	3.0 pF
PACDN002	17	7.5 pF
PACDN007	18	7.5 pF

Table 2: ESD Protection Diode Arrays

Each channel of these arrays utilizes a pair of diodes as the basic ESD protection mechanism (see Figure 1). In operation, V_P is generally connected to the system power supply, and V_N to ground. The Channel I/O pin is connected to the device or I/O line being protected. When a positive (with respect to ground) ESD pulse strikes the Channel I/O pin, diode D1 conducts and steers the ESD current pulse into the system supply line. Thus the voltage at the Channel I/O pin is clamped at the power supply voltage plus the forward voltage of D1. Similarly, for a negative ESD strike, D2 conducts and clamps the voltage at the Channel I/O pin at one forward voltage of D2 below ground. Thus the device or I/O line being protected will see a substantially lower voltage than the applied ESD peak voltage.

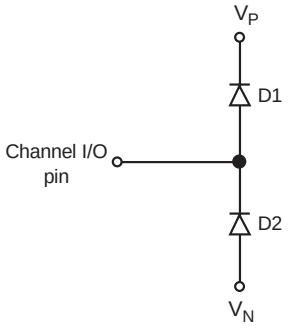

Figure 1: Schematic of one ESD Protection Channel

C0140398A

A major advantage of this ESD protection circuit is the low loading capacitance that can be achieved for a given level of protection relative to other schemes using Zener or breakdown diodes. Since the forward voltage drops of D1 and D2 are much lower than the breakdown voltage of Zener or other breakdown diodes, the power dissipation of D1 and D2 when subjected to an ESD strike is much lower. Hence D1 and D2 can be much smaller physically, resulting in significantly lower junction capacitance. For example, the PAC DN006 has a typical channel loading capacitance of just 3pF. It is not uncommon for Zener or breakdown protection devices to have loading capacitance of 100 pF or more. Capacitive loading is a serious problem in high speed applications such as video ports, as it slows down signal edges and distorts the signal.

Characteristics of the IEC-1000-4-2 ESD Pulse

The IEC-1000-4-2 standard ESD model specifies an ESD current pulse that has an extremely fast rise time (between 700pS and 1 nS), as shown in Figure 2. Furthermore, any ESD generator compliant with this standard must be calibrated to the waveform parameters shown in Table 3. This fast rise time dictates that care must be exercised in the design and layout of protection circuits. This application note will explain these issues and establish design guidelines to ensure maximum benefit from the use of these ESD Protection Diode Arrays.

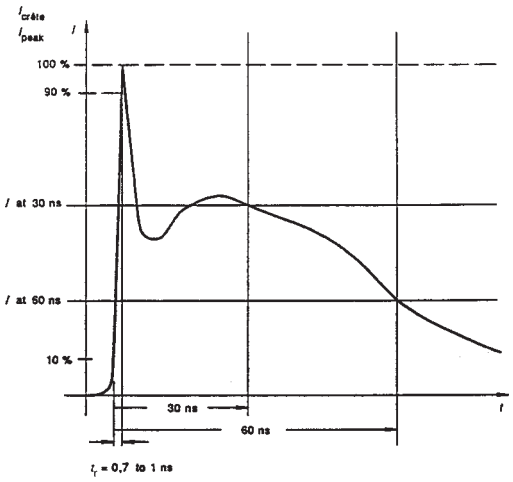

Figure 2: IEC-1000-4-2 Compliant ESD Current Pulse Waveform

Effects of Parasitic inductance in the ESD Current Path

To begin with, let us examine the effect of parasitic inductances in the ESD current path. If not properly controlled, these parasitic inductances can add substantially to the clamp voltage of the ESD protection diodes. Figure 3 illustrates the effect of parasitic inductance (L_1) in the positive supply return when a positive (with respect to GND) ESD pulse is applied. In this case, diode D1 conducts and steers the ESD current pulse (I_{ESD}) into the V_{CC} line. The clamp voltage (V_X) seen by the device being protected is given by:

$$(1) \quad V_X = V_{F1} + L_1 \times dI_{ESD}/dt + V_{CC}$$

where V_{F1} is the forward voltage drop of the diode D1, and assuming that V_{CC} is a perfect power supply with zero output impedance.

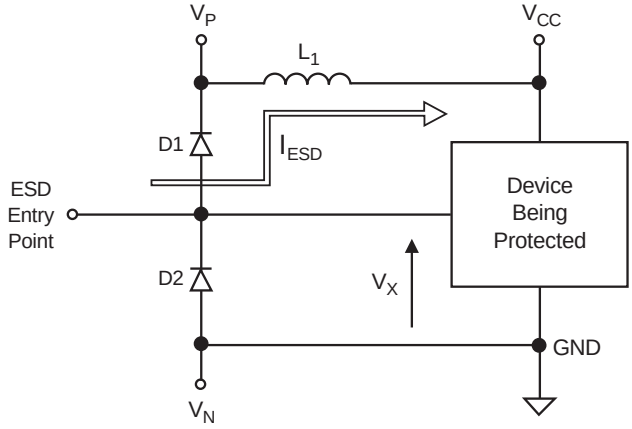

Figure 3: Effect of parasitic inductance in the V_{CC} line on ESD clamp voltage.

As explained in a previous section, a level-4 contact discharge ESD pulse, compliant with the IEC-100-4-2 ESD model, typically results in a current pulse that rises from zero to a peak amplitude of 30A in 1 nS. Thus dI_{ESD}/dt can be approximated by 30×10^{-9}. Assuming that L_1 is 10 nH for example, it will contribute 300 V to V_X. The forward drop of the diode D1 is typically well under 30V under the same peak current for ESD Protection Arrays such as the PAC DN006. So

Level	Test Voltage KV	First peak current of discharge (±10%) A	Rise time t_r nS	Current (±30%) at 30 nS A	Current (±30%) at 60 nS A
1	2	7.5	0.7 to 1	4	2
2	4	15	0.7 to 1	8	4
3	6	22.5	0.7 to 1	12	6
4	8	30	0.7 to 1	16	8

Table 3: IEC-1000-4-2 ESD Waveform Parameters

V_X is dominated by the contribution of L_1.
A similar situation occurs for parasitic inductance in the ground return path. In this case, the clamping voltage for negative ESD pulses is increased due to the presence of inductance in the ground path.

These parasitic inductances can be minimized by following a few simple rules in the layout of the printed circuit board:

- Use V_{CC} and ground planes for power and ground distribution whenever possible.
- Keep the printed circuit traces from the V_P and V_N pins of the ESD Protection Diode Array to the V_{CC} and Ground planes short and wide. Ideally, connect the V_P and V_N pins directly through multiple vias to the V_{CC} and Ground planes.

Effect of Output Impedance of the Power Supply

From Equation (1) above, it can be seen that V_{CC} also adds directly to the positive clamp voltage V_X. It is easy to make the assumption that power supplies will always keep the output voltage constant regardless of loading conditions. While this is a reasonable assumption for low frequency load variations that are within the load regulation range of the power supply, it is not the case when the power supply is being forced to absorb a level-4 ESD current pulse. Under this condition, the power supply can exhibit an output impedance much higher than when it is operating under normal operating conditions. For each Ohm of output impedance, V_{CC} will be increased by a peak voltage of 30V. Thus the peak value of V_X will be increased by the same amount.

A simple, yet effective, solution to this is to connect a high frequency bypass capacitor between the V_P pin and the ground plane, with minimal PCB trace lengths to minimize inductance. It is imperative that this bypass capacitor has low internal series inductance. For this reason, electrolytic capacitors should be avoided. In general, a ceramic chip capacitor in the range of 0.1 uF to 0.2 uF should be adequate. The inclusion of the bypass capacitor also helps in alleviating the effect of parasitic inductance in the V_{CC} return path. A Zener diode with a breakdown voltage slightly above the maximum value of V_{CC} can also be connected in parallel with the bypass capacitor to mitigate the effects of parasitic series inductance inherent in the capacitor.

The example PCB layout shown in Figure 4 shows how parasitic inductances in the V_{CC} and ground paths can be minimized while incorporating the bypass capacitor as well. In this example, the PAC DN006 is used as the Protection Diode Array.

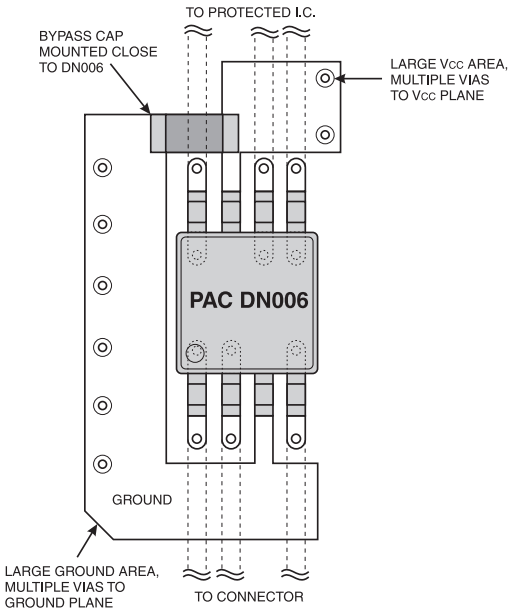

Figure 4: PCB layout example using the PAC DN006.

Maximizing Effectiveness of ESD protection Diodes

Most CMOS VLSI integrated circuits have built-in ESD protection diode networks that are similar to those used in California Micro Device's ESD Protection Diode Arrays. However, they are usually designed to withstand much lower ESD voltages. In addition, when these devices are powered up, they are prone to "ESD-induced latch-up". This is a phenomenon whereby the parasitic SCR inherent in all bulk CMOS processes is triggered by excessive current flowing through these built-in ESD protection diodes. This is usually a destructive event. Hence it is important to minimize the current flowing through these internal diodes under an ESD strike. By employing external ESD protection devices such as the ESD Protection Diode Array, the ESD current is diverted through the external protection diodes, reducing the current that flows through the internal diodes. Maximum benefit can be derived by forcing most, if not all, of the ESD current to flow through the external diode. This can be achieved by inserting a series resistor between the external diode network and the device being protected as shown in Figure 5.

The choice of value of the series resistor is dependent on the application. In general, when the protected pin is a logic input pin, the value of this resistor can be quite high without affecting the normal operation of the protected device. This is due to the fact that CMOS logic inputs typically have input resistance in the Mega-Ohms range. Here, the only concern would be the degradation in input rise and fall times resulting

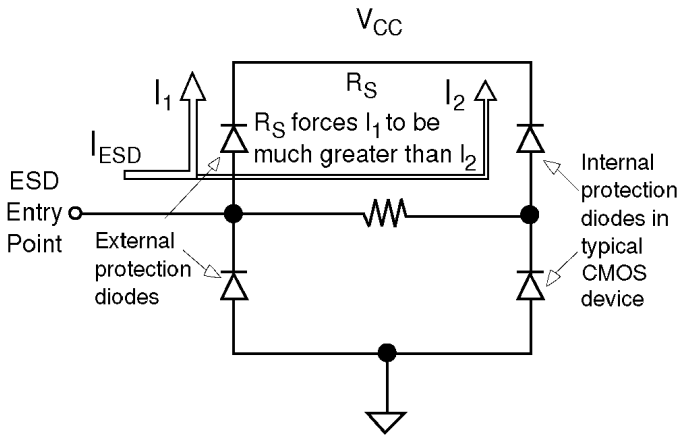

Figure 5: Using series resistor to force ESD current through external protection diode.

from the RC filter formed by the series resistor and the input capacitance of the pin. For output or I/O pins, the value of the series resistor should generally be much lower than the output resistance of the output drivers. Otherwise degradation in output levels may occur.

Physical Placement of Protection Diode Array and Protected Component in Printed Circuit Board

The location of the ESD Protection Diode Array in a PCB relative to the component to be protected is crucial to realizing good ESD protection. In general, it is preferable to place the ESD Protection Diode Array close to the point of entry of any expected ESD. This ensures that the ESD energy is absorbed and dissipated safely as quickly as possible on entry to minimize disturbance to the rest of the system.

The placement of the component to be protected is also critical. This is, again, due to the effect of the parasitic PCB trace inductance on the ESD current pulse with its fast rise time. Consider the two PCB layout examples in Figure 5. In case (a), the component to be protected is placed "upstream" from the Protection Diode Array and connected to it with a long PCB trace which has an effective inductance of L_S. In this case, L_S would resist the flow of ESD current into the Protection Diode Array, forcing most of the ESD current to flow into the protected component, thus defeating the purpose of the Protection Diode Array. Simply exchanging the placement of these two devices as in case (b) will result in much improved ESD tolerance for the system. The protected component is now connected "downstream" from the Protection Diode Array, where L_S acts to divert ESD current away from the protected component and into the Protection Diode Array where it can be dissipated safely.

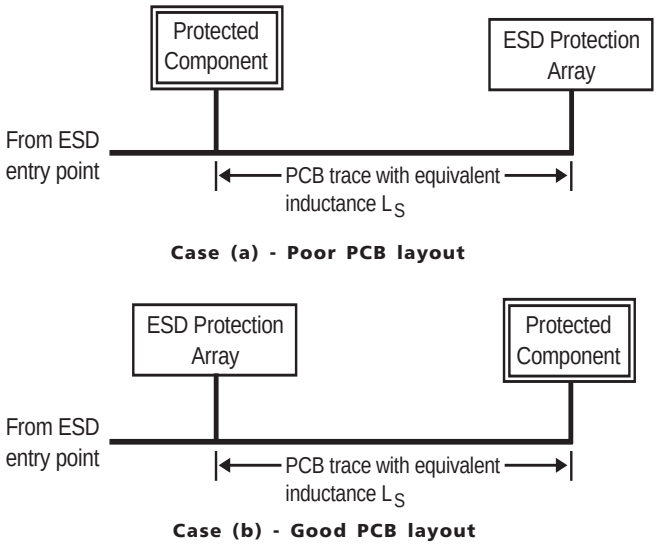

Figure 6: Placement of ESD Protection Array and component to be protected.

Conclusion

Compliance to the IEC-1000-4-2 ESD standard is fast becoming a system requirement, even in consumer electronics. California Micro Devices provides a family of easy to use ESD Protection Diode Arrays to help designers achieve the highest level of ESD protection (level 4) specified in that standard. This family ranges from a two-channel array to a highly integrated 18-channel array, all offering very low loading capacitance for high speed signal applications.

Due to the very fast rise time inherent in the ESD current pulse, designers must be aware of the significance of parasitic inductances in the ESD current path and non-ideal behavior of circuit elements, and deal with them in the design in order to achieve maximum benefits from deploying any ESD protection devices, including California Micro Device's family of ESD Protection Diode Arrays. This Application Note has explored these issues and recommended guidelines to help the system designers achieve ESD tolerant systems.