PRELIMINARY

Integrated Circuit Systems, Inc.

ICS8430-01
HIGH FREQUENCY SYNTHESIZER

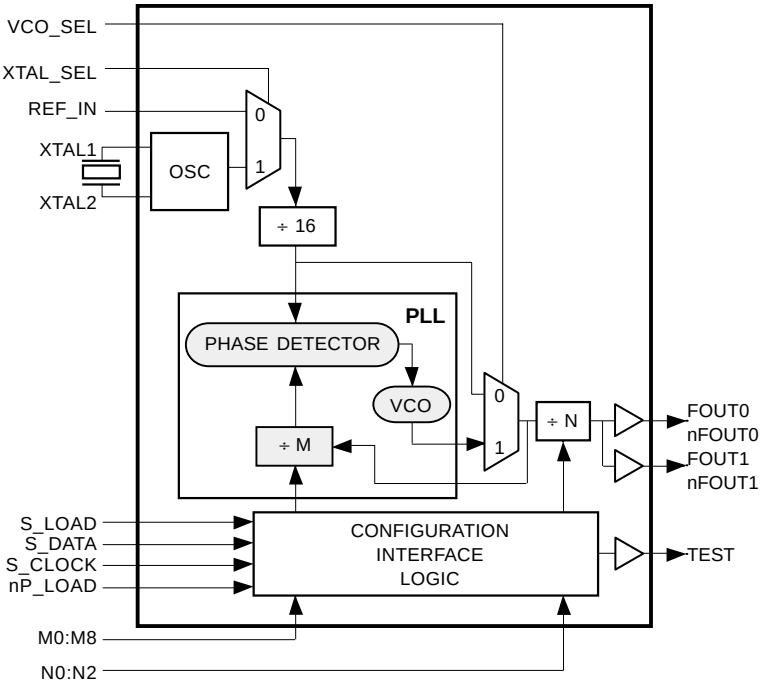
GENERAL DESCRIPTION

The ICS8430-01 is a general purpose, dual output high frequency synthesizer and a member of the HiPerClockS™ family of High Performance Clocks Solutions from ICS. The VCO operates at a frequency range of 280MHz to 400MHz. The output frequency can be programmed using the serial or parallel interfaces to the configuration logic. With the output configured to divide the VCO frequency by 2 output frequency steps as small as 0.5MHz can be achieved using a 16MHz crystal or reference clock.

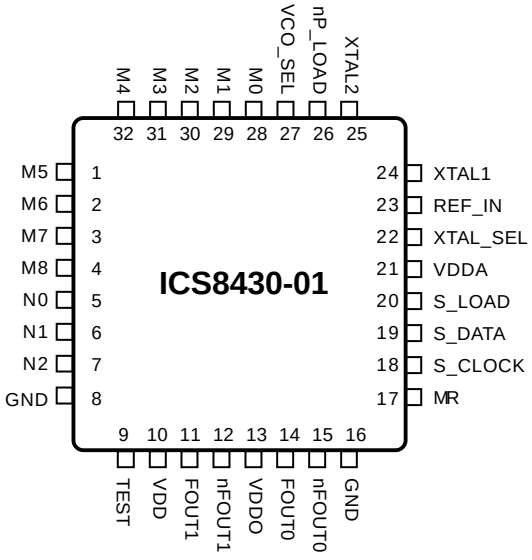
FEATURES

- Fully integrated PLL
- Dual differential 3.3V LVPECL output
- 23MHz to 400MHz output frequency
- ±25ps peak-to-peak output jitter
- Parallel interface for programming counter and output dividers during power-up
- Serial 3 wire interface
- Selectable crystal oscillator interface and LVCMOS reference input
- LVCMOS control inputs
- 3.3V supply voltage
- 32 lead low-profile QFP(LQFP), 7mm x 7mm x 1.4mm package body, 0.8mm package lead pitch
- 0°C to 70°C ambient operating temperature

BLOCK DIAGRAM



PIN ASSIGNMENT



32-Lead LQFP
Y Package
Top View

The Advance Information presented herein represents a product currently in design or being considered for design. The noted characteristics are design targets. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

FUNCTIONAL DESCRIPTION

The ICS8430-01 features a fully integrated PLL and therefore requires no external component for setting the loop bandwidth. A series-resonant , fundamental crystal is used as the input to the on-chip oscillator. The output of the oscillator is divided by 16 prior to the phase detector. With a 16MHz crystal this provides a 1MHz reference frequency. The VCO of the PLL operates over a range of 280MHz to 400MHz. The output of the loop divider is also applied to the phase detector.

The phase detector and the loop filter force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve lock. The output of the VCO is scaled by a divider prior to being sent to each of the LVPECL output buffers. The divider provides a 50% output duty cycle.

The programmable features of the ICS8430-01 support two input modes and programmable PLL loop divider and output divider. The two input operational modes are parallel and serial. Figure 1 shows the timing diagram for each mode. In parallel mode the nP_LOAD input is initially LOW. The data on inputs M0 through M8 and N0 through N2 is passed directly to the ripple counter. On the LOW-to-HIGH transition of the nP_LOAD input the data is latched and the ripple counter remains loaded until the next LOW transition on nP_LOAD or until a serial event occurs. As a result the M and N bits can be hardwired to set the ripple counter to a specific default state that will automatically occur during power-up. The TEST output is LOW when operating in the parallel input mode. The relationship between the VCO frequency, the crystal frequency and the loop divider is defined as follows:

$$fVCO = \frac{fxtal}{16} \times M$$

The M count and the required values of M0 through M8 are shown in Table4B, Programmable VCO Frequency Function Table. The frequency out is defined as follows:

$$fout = \frac{fVCO}{N} = \frac{fxtal}{16} \times \frac{M}{N}$$

Serial operation occurs when nP_LOAD is HIGH and S_LOAD is LOW. The shift register is loaded by sampling the S_DATA bits with the rising edge of S_CLOCK. The contents of the shift register are loaded into the ripple counter when S_LOAD transitions from LOW-to-HIGH. The ripple counter divide values are latched on the HIGH-to-LOW transition of S_LOAD. If S_LOAD is held HIGH data at the S_DATA input is passed directly to the ripple counter on each rising edge of S_CLOCK. The serial mode can be used to program the M and N bits and test bits T1 and T0. The internal registers T0 and T1 determine the state of the TEST output as follows:

T1	T0	TEST Output
0	0	LOW
0	1	S_Data clocked into register
1	0	Output of M divider
1	1	CMOS Fout

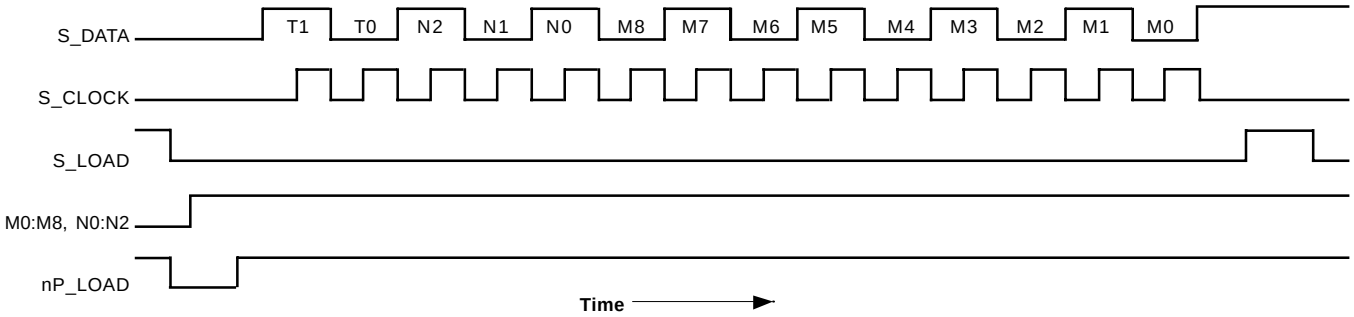


FIGURE 1. PARALLEL & SERIAL LOAD OPERATIONS

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
28, 29, 30 31, 32, 1, 2	M0, M1, M2 M3, M4, M5, M6	Input	Pulldown	M counter/divider inputs. Data latched on LOW-to-HIGH transistion of nP_LOAD input. LVCMOS / LVTTL interface levels.
3, 4	M7, M8	Input	Pullup	
5, 7	N0, N2	Input	Pulldown	Determines output divider value as defined in Table 3 Function Table. LVCMOS / LVTTL interface levels.
6	N1	Input	Pullup	
8, 16	GND	Power		Power supply ground pin. Connect to ground.
9	TEST	Output		Test output which is ACTIVE in the serial mode of operation. Output driven LOW in parallel mode. LVCMOS interface levels.
10	VDD	Power		Core power supply pin.
11, 12	FOUT1, nFOUT1	Output		Differential output for the synthesizer. 3.3V LVPECL interface levels.
13	VDDO	Power		Output power supply connection. Connect to 3.3V.
14, 15	FOUT0, nFOUT0	Output		Differential output for the synthesizer. 3.3V LVPECL interface levels.
17	MR	Input	Pulldown	Resets the reference frequency and output dividers. Loads data present at the M bits into counter. LVCMOS / LVTTL interface levels.
18	S_CLOCK	Input	Pulldown	Clocks in serial data present at S_DATA input into the shift register on the rising edge of S_CLK.
19	S_DATA	Input	Pulldown	Shift register serial input. Data sampled on the rising edge of S_CLK.
20	S_LOAD	Input	Pulldown	Controls transition of data from shift register into the ripple counter. LVCMOS / LVTTL interface levels.
21	VDDA	Power		Analog power supply pin. Connect to 3.3V.
22	XTAL_SEL	Input	Pullup	Selects between crystal or reference inputs as the PLL reference source. LVCMOS / LVTTL interface levels. Selects XTAL inputs when HIGH. Selects REF_IN when LOW.
23	REF_IN	Input	Pulldown	Reference clock input. LVCMOS / LVTTL interface levels.
24, 25	XTAL1, XTAL2	Input		Crystal oscillator inputs.
26	nP_LOAD	Input	Pulldown	Parallel load input. Determines when data present at M8:M0 is loaded into ripple counter. LVCMOS / LVTTL interface levels.
27	VCO_SEL	Input	Pullup	Determines whether synthesizer is in PLL or bypass mode. LVCMOS / LVTTL interface levels.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
CIN	Input Capacitance					pF
RPULLUP	Input Pullup Resistor			51		KΩ
RPULLDOWN	Input Pulldown Resistor			51		KΩ

TABLE 3. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Min	Typ	Max	Units
Crystal Cut	Mode of Oscillation				
Frequency Tolerance					ppm
Frequency Stability					ppm
Drive Level					µW
Equivalent Series Resistance (ESR)					Ω
Shunt Capacitiance					pF
Series Pin Inductance					nH
Aging					ppm

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	4.6V
Inputs	-0.5V to VDD+0.5 V
Outputs	-0.5V to VDD+0.5V
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any conditions beyond those listed in the *DC Electrical Characteristics* or *AC Electrical Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. PARALLEL AND SERIAL MODES FUNCTION TABLE

INPUTS							Conditions
MR	nP_LOAD	M	N	S_LOAD	S_CLOCK	S_DATA	
H	X	X	X	X	X	X	Reset. M and N counters reset.
L	L	Data	Data	X	X	X	Data on M and N inputs passed directly to ripple counter. TEST output forced LOW.
L	↑	Data	Data	X	X	X	Data is latched into input registers and remains loaded until next LOW transition or until a serial event occurs.
L	H	X	X	L	↑	Data	Serial input mode. Shift register is loaded with data on S_DATA on each rising edge of S_CLOCKt
L	H	X	X	↑	L	Data	Contents of the shift register are passed to the ripple counter.
L	H	X	X	↓	L	Data	Ripple counter divide values are latched.
L	H	X	X	L	X	X	Parallel or serial input do not affect shift registers.

TABLE 4B. PROGRAMMABLE VCO FREQUENCY FUNCTION TABLE

VCO Frequency (MHz)	M Count	256	128	64	32	16	8	4	2	1
		M8	M7	M6	M5	M4	M3	M2	M1	M0
250	250	0	1	1	1	1	1	0	1	0
251	251	0	1	1	1	1	1	0	1	1
252	252	0	1	1	1	1	1	1	0	0
253	253	0	1	1	1	1	1	1	0	1
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
498	498	1	1	1	1	1	0	0	1	0
499	499	1	1	1	1	1	0	0	1	1
500	500	1	1	1	1	1	0	1	0	0

TABLE 4C. PROGRAMMABLE OUTPUT DIVIDER FUNCTION TABLE

Input			N Divider Value	Output Frequency (MHz)	
N2	N1	N0		Min	Max
0	0	0	1	280	400
0	0	1	1.5	186.66	266.66
0	1	0	2	140	200
0	1	1	3	93.33	133.33
1	0	0	4	70	100
1	0	1	6	46.66	66.66
1	1	0	8	35	50
1	1	1	12	23.33	33.33

TABLE 5. DC ELECTRICAL CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
VDD, VDDA, VDDO	Power Supply Voltage			3.135	3.3	3.465	V
IDD	Quiescent Power Supply Current		VDDx = 3.465V			110	mA
VIH	Input High Voltage	All except REF_IN, XTAL1, XTAL2	3.135 ≤ VDDx ≤ 3.465V	2		3.765	V
		REF_IN	VDDx = 3.465V	1.8		3.8	V
			VDDx = 3.135V	1.7		3.4	V
VIL	Input Low Voltage	All except REF_IN, XTAL1, XTAL2	3.135 ≤ VDDx ≤ 3.465V	-0.3		0.8	V
		REF_IN	VDDx = 3.465V	-0.3		1.6	V
			VDDx = 3.135V	-0.3		1.5	V
IIH	Input High Current	M0-M6, N0, N2 MR, S_CLOCK, S_DATA, S_LOAD, REF_IN, nP_LOAD	VDDx = VIN = 3.465V			150	µA
		M7, M8, N1, XTAL_SEL, VCO_SEL	VDDx = VIN = 3.465V			5	µA
IIL	Input Low Current	M0-M6, N0, N2 MR, S_CLOCK, S_DATA, S_LOAD, REF_IN, nP_LOAD	VDDx = 3.465V, VIN = 0V	-150			µA
		M7, M8, N1, XTAL_SEL, VCO_SEL	VDDx = 3.465V, VIN = 0V	-5			µA
VOH	Output High Voltage; NOTE 1, 2	FOUT0, nFOUT0, FOUT1, nFOUT1	VDDx = 3.3V	2.1			V
		TEST	VDDx = 3.135	2.4			V
VOL	Output Low Voltage; NOTE 1, 2	FOUT0, nFOUT0, FOUT1, nFOUT1	VDDx = 3.3V			1.6	V
		TEST	VDDx = 3.135			0.5	V
VPPO	Peak-to-Peak Output Voltage	FOUT0, nFOUT0, FOUT1, nFOUT1	3.135 ≤ VDDx ≤ 3.465V	0.6			V

NOTE 1: FOUT0, nFOUT0, FOUT1, nFOUT1 outputs terminated with 50Ω to VDDO-2V.
NOTE 2: These levels are specified for VDDO = 3.3V. Output levels will vary 1:1 with VDDO.

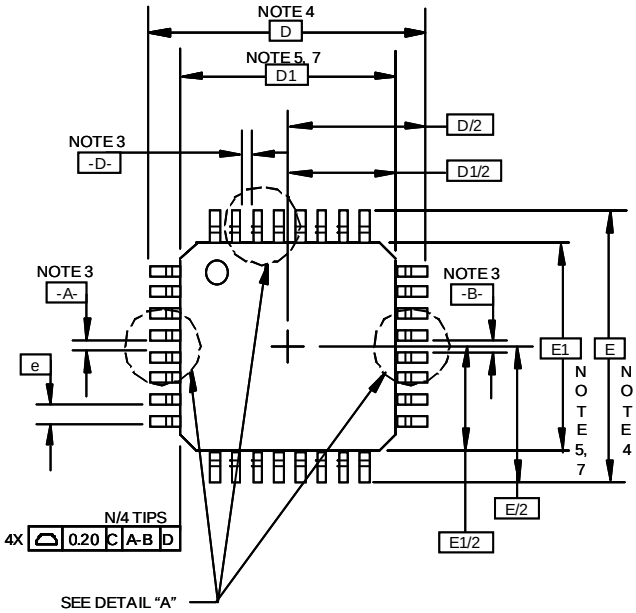
TABLE 6. INPUT FREQUENCY CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

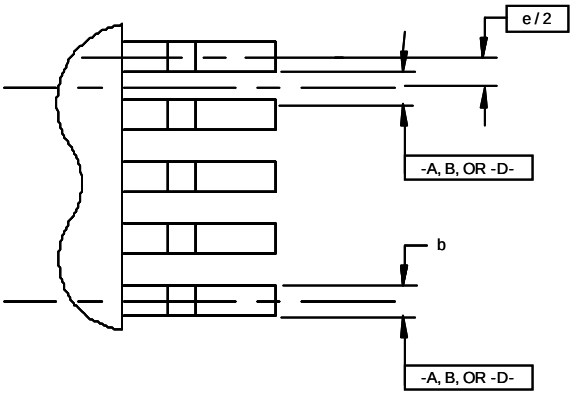
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
fMAXIN	Maximum Input Frequency	REF		10		25	MHz
		XTAL		10		25	MHz
		S_CLOCK				TBD	MHz
tR	Input Rise Time	REF	Measured at 20% to 80% points			TBD	ns
tF	Input Fall Time	REF	Measured at 20% to 80% point			TBD	ns
tDC	Input Reference Duty Cycle	REF		TBD		TBD	%

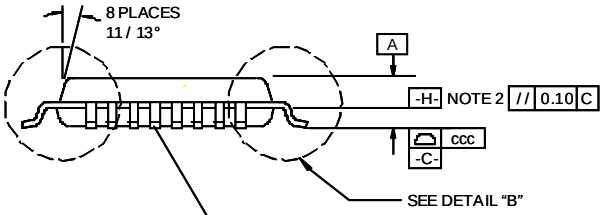
TABLE 7. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ TO $70°C$

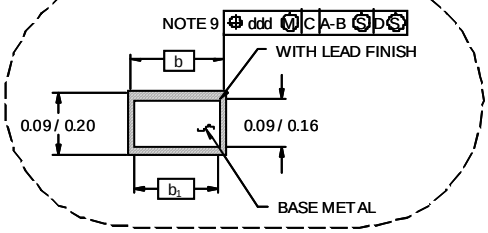
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
FMAX	Maximum Output Frequency		3.135 ≤ VDDx ≤ 3.465V	23		400	MHz
tjit(cc)	Peak Cycle-to-Cycle Jitter					50	ps
tsk(o)	Output Skew					TBD	ps
tDC	Output Duty Cycle			47		53	%
tR	Output Rise Time	FOUT0, nFOUT0 FOUT1, nFOUT1	20% to 80%	300		800	ps
tF	Output Fall Time	FOUT0, nFOUT0 FOUT1, nFOUT1	20% to 80%	300		800	ps
tS	Setup Time	M, N to nP_LOAD		TBD			ns
		S_DATA to S_CLOCK		TBD			ns
		S_CLOCK to S_LOAD		TBD			ns
tH	Hold Time	M, N to nP_LOAD		TBD			ns
		S_DATA to S_CLOCK		TBD			ns
		S_CLOCK to S_LOAD		TBD			ns
tLOCK	PLL Lock Time					TBD	ms
tPW	Pulse Width	nP_LOAD				TBD	ns
		S_LOAD				TBD	ns

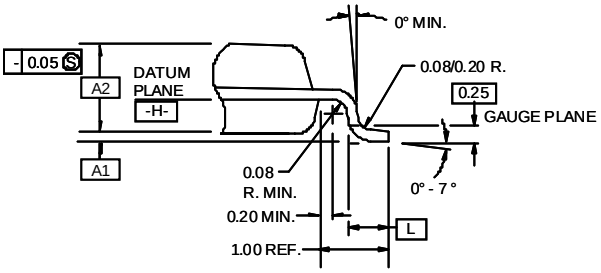
PACKAGE OUTLINE AND DIMENSIONS - Y SUFFIX











NOTES:

1. ALL DIMENSIONS AND TOLERANCING CONFORM TO ANSI Y14.5-1982
2. DATUM PLANE -H- LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DATUMS A-B AND -D- TO BE DETERMINED AT CENTERLINE BETWEEN LEADS WHERE LEADS EXIT PLASTIC AT DATUM PLANE -H- .
4. TO BE DETERMINED AT SEATING PLACE -C- .
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
6. "N" IS THE TOTAL NUMBER OF TERMINALS.
7. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE -H-.
8. PACKAGE TOP DIMENSIONS ARE SMALLER THAN BOTTOM DIMENSIONS AND TOP OF PACKAGE WILL NOT OVERHANG BOTTOM OF PACKAGE.
9. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
10. CONTROLLING DIMENSION: MILLIMETER.
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-026, VARIATION ABA.
12. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE.

SYMBOL	JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			NOTE
	BBA			
	MIN	NOM	MAX	
A			1.60	
A1	0.05		0.15	12
A2	1.35	1.4	1.45	
D		9.00 BSC.		4
D1		7.00 BSC.		7, 8
E		9.00 BSC.		4
E1		7.00 BSC.		7, 8
L	0.45	0.60	0.75	
N		32		
e		0.80 BSC.		
b	0.30	0.37	0.45	
b1	0.30	0.35	0.40	9
ccc			0.10	
ddd			0.20	

ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8430AY-01	ICS8430AY-01	32 Lead LQFP		0°C to 70°C
ICS8430AY-01T	ICS8430AY-01	32 Lead LQFP on Tape and Reel		0°C to 70°C