LOW SKEW CLOCK DRIVER/ BUFFER FOR MOBILE PC WITH FOUR SO-DIMMS

QS5814

FEATURES:

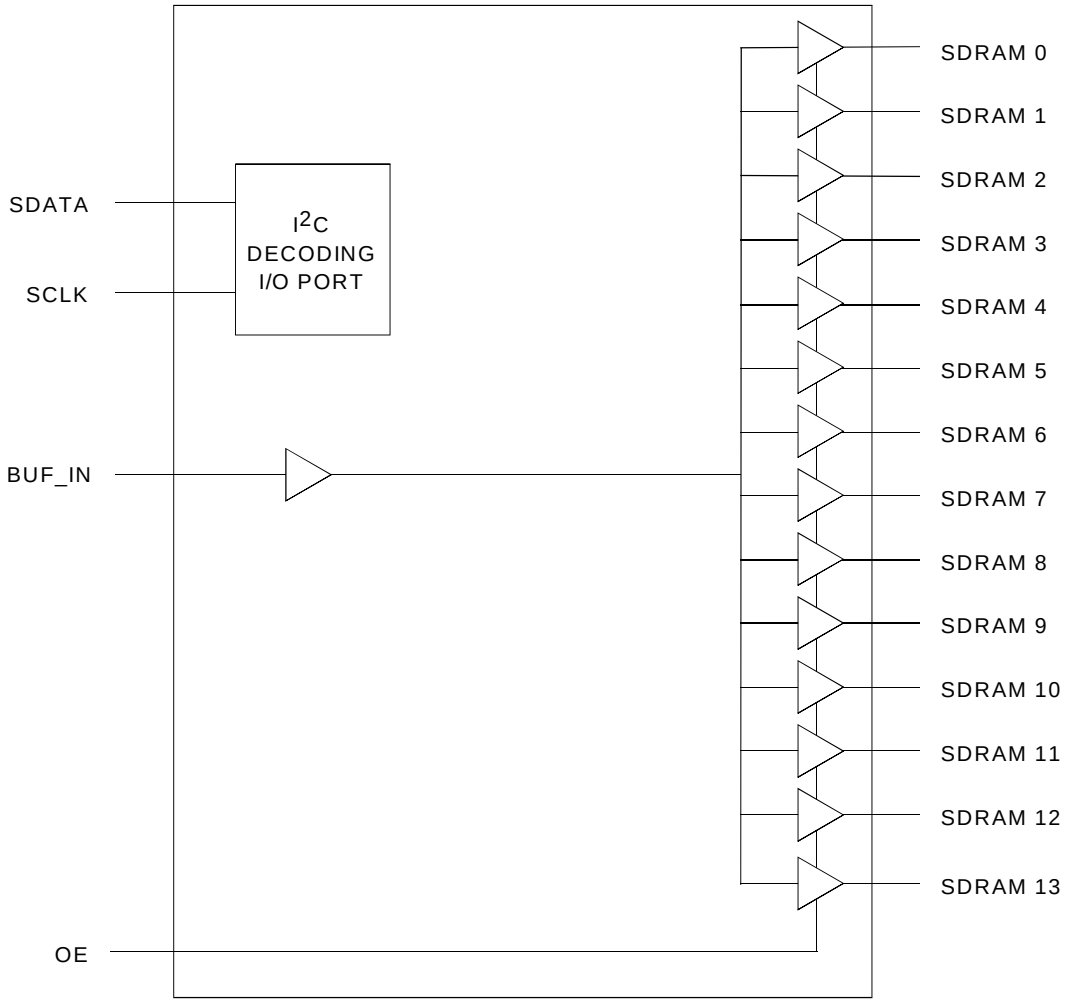
- 1 to 14 output buffer/driver
- Tri-state pin for testing
- I^2C programming capability
- Power Supply Voltage 3.3V ±5%
- Low Skew Outputs (<200ps)
- Multiple V_{DD} and GND for noise reduction
- 28 Pin SSOP package

DESCRIPTION

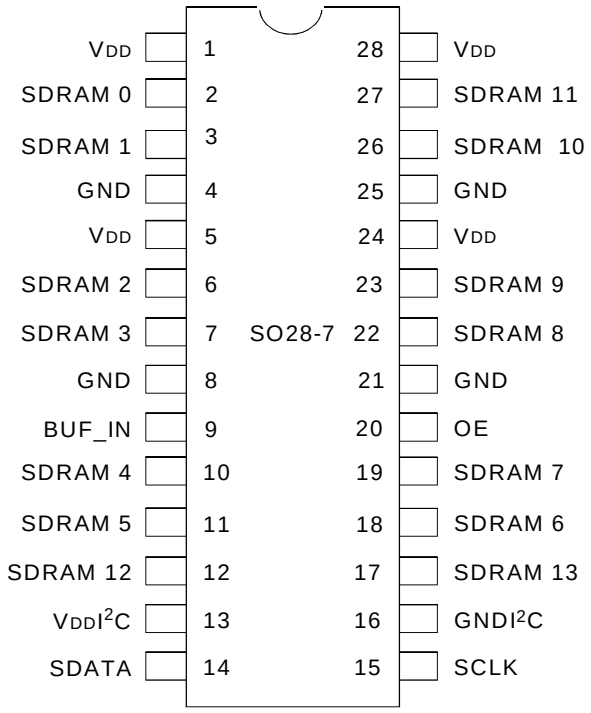
The QS5814 is a high speed, low noise non-inverting buffer designed for SDRAM clock buffer applications. Out of the 14 outputs, 12 could be used to drive up to four SDRAM SO-DIMMS, and the remaining can be used for external feedback to a PLL stage for synchronization to master clock.

The QS5814 also includes an I^2C interface, which can enable or disable each output clock when the lines are not used. By turning the outputs on and off, I^2C will aid in reducing the Electro Magnetic Interference (EMI).

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max.	Unit
V_{DD}	Supply Voltage to Ground	– 0.5 to 4.6V	V
V_{OH}	DC Output Voltage	– 0.5 to + 4.6V	V
V_{IL}	DC Output Voltage	– 0.5 to + 4.6	V
V_I	DC Input Diode Current	– 20	mA
T_A	Maximum Power Dissipation at T_A = 85°C	600	mW
T_{STG}	Storage Temperature	–65 to 150	°C

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

PIN DESCRIPTION

Pin Name	Description
SDRAM (0:5)	SDRAM Byte 0 Clock Outputs.
SDRAM (6:11)	SDRAM Byte 1 Clock Outputs.
SDRAM (12:13)	SDRAM Byte 2 Clock Outputs.
BUF_IN	Input for Buffers.
OE	Tri-State Output Enable. When asserted LOW, clock outputs are high impedance. It has 100kΩ internal pull up to V_{DD}.
SDATA	I^2C Data Input. It has 100kΩ internal pull up to V_{DD}.
SCLK	I^2C Data Input. It has 100kΩ internal pull up to V_{DD}.
V_{DD}	3.3V power supply for output buffers.
GND	Ground for output buffers.
$GNDI^2C$	Ground for I^2C circuitry.
$V_{DD}I^2C$	3.3V Power Supply for I^2C circuitry.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = – 40°C to +85°C

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Voltage Level	For all Inputs	2	—	—	V
V_{IL}	Input LOW Voltage Level	For all inputs except I^2C inputs (SDATA and SCLK)	—	—	0.8	V
I_{IH}	Input High Current	$V_{IN} = V_{DD}$	– 5	—	5	µA
I_{IL}	Input Low Current	V_{IN} = 0V	– 5	—	5	µA
		V_{IN} = 0V; Inputs with 100k pull up	– 100	—	—	
I_{DD}	Supply Current	C_L = 0pF; f_{IN}@66.66MHz(1)	—	50	70	mA
		C_L = 30pF; f_{IN}@66.66MHz(1)	—	135	155	
		C_L = 0pF; f_{IN}@100MHz(1)	—	75	105	
		C_L = 30pF; f_{IN}@100MHz(1)	—	195	230	
		BUF_IN 0 or V_{DD}	—	—	500	µA
V_{OH}	Output High Voltage	I_{OH} = –36mA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL} = 25mA	—	—	0.4	V
V_{OLI^2C}	Output Low Voltage	SDATA I_{OLI^2C} = 3mA	—	—	0.4	V

NOTE:
1. Typical values are at V_{CC} = 3.3V, +25°C ambient.

AC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max.	Unit
t_R	Rise Time(1)	0.4V to 2.4V; C_L = 30pF	—	—	2.2	ns
t_F	Fall Time(1)	2.4V to 0.4V; C_L = 30pF	—	—	2.2	ns
Dt	Duty Cycle(1)	V_T = 1.5V; C_L = 30pF	45	50	55	%
T_{SK}	Skew (output-to-output)(1)	V_T = 1.5V; C_L = 30pF for all outputs	—	—	200	ps
T_{PHL} or T_{PLH}	Propagation Delay	V_T = 1.5V	—	—	6	ns
$T_{PROP\ EN}$	Enable Delay	V_T = 1.5V	—	—	8	ns
$T_{PROP\ DIS}$	Disable Delay	V_T = 1.5V	—	—	8	ns

NOTE:
1. Guaranteed by design, not subject to 100% production testing.

OPERATING CHARACTERISTICS , T_A = 25ºC

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Voltage	3.135	3.3	3.465	V
T_A	Operating Temperature	-40	25	85	°C
C_L	Load Capacitance	—	—	30	pF
C_{IN}	Input Capacitance(1)	—	—	15	pF

I²C SERIAL INTERFACE CONTROL

The I²C interface permits individual enable/disable of each clock output: any unused outputs may be disabled to reduce the EMI. The QS5814 is a slave receiver device. It can read back the data stored in the latches for verification.

The data transfer rate supported by the I²C interface is 100k bits/sec. Data is transferred in bytes (with the addition of start, stop, acknowledge bits) in sequential order from the lowest to highest byte with the ability to stop after any complete byte has been transferred. The first two bytes transferred must be a Command Code followed by a Byte Count. Both of these bytes are ignored by the device.

The I²C address of the QS5814 is:

A7	A6	A5	A4	A3	A2	A1
1	1	0	1	0	0	1

Address A0 is the read/write bit and is set to 0 for writes and 1 for reads. During read back, the first byte read is a Byte Count representing the number of bytes following (fixed at 3).

SERIAL CONFIGURATION COMMAND BITMAPS

Byte 0: SDRAM Active/Inactive Register
(1 = Enable, 0 = Disable), Default = Enable

Bit	Pin #	Description
Bit 7	11	SDRAM 5 (Active/Inactive)
Bit 6	10	SDRAM 4 (Active/Inactive)
Bit 5	—	Initialize to 0
Bit 4	—	Initialize to 0
Bit 3	7	SDRAM 3 (Active/Inactive)
Bit 2	6	SDRAM 2 (Active/Inactive)
Bit 1	3	SDRAM 1 (Active/Inactive)
Bit 0	2	SDRAM 0 (Active/Inactive)

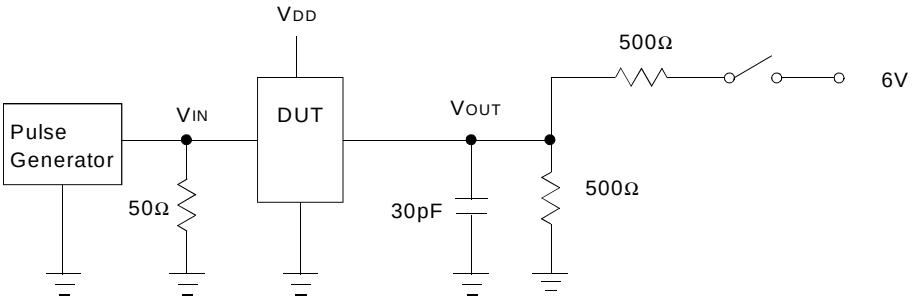
Byte 1: SDRAM Active/Inactive Register
(1 = Enable, 0 = Disable), Default = Enable

Bit	Pin #	Description
Bit 7	27	SDRAM 11 (Active/Inactive)
Bit 6	26	SDRAM 10 (Active/Inactive)
Bit 5	23	SDRAM 9 (Active/Inactive)
Bit 4	22	SDRAM 8 (Active/Inactive)
Bit 3	—	Initialize to 0
Bit 2	—	Initialize to 0
Bit 1	19	SDRAM 7 (Active/Inactive)
Bit 0	18	SDRAM 6 (Active/Inactive)

Byte 2: SDRAM Active/Inactive Register
(1 = Enable, 0 = Disable), Default = Enable

Bit	Pin #	Description
Bit 7	17	SDRAM 13 (Active/Inactive)
Bit 6	12	SDRAM 12 (Active/Inactive)
Bit 5	—	Reserved, 1 at power up, set to 0
Bit 4	—	Reserved, 1 at power up, set to 0
Bit 3	—	Reserved, 1 at power up, set to 0
Bit 2	—	Reserved, 1 at power up, set to 0
Bit 1	—	Reserved, 1 at power up, set to 0
Bit 0	—	Reserved, 1 at power up, set to 0

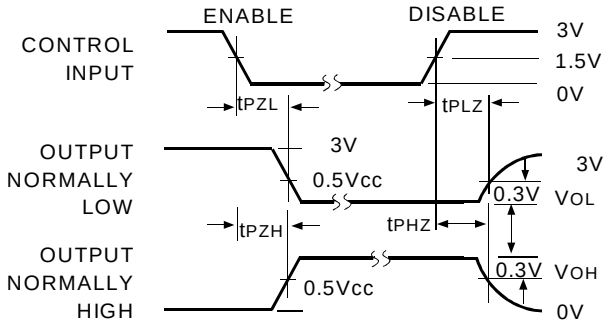
TEST CIRCUIT



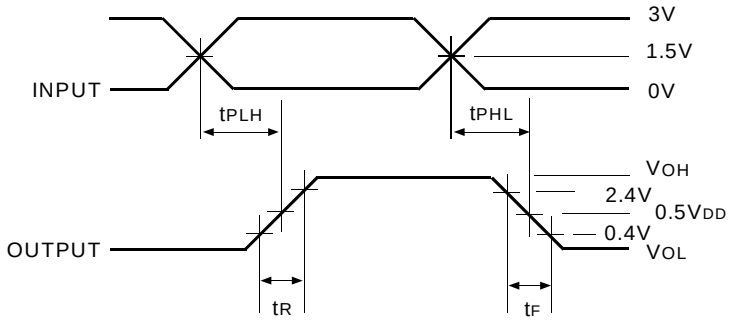
Parameter Tested	Switch Position
tPLZ, tPZL	Closed
All Others	Open

AC TIMING DIAGRAM

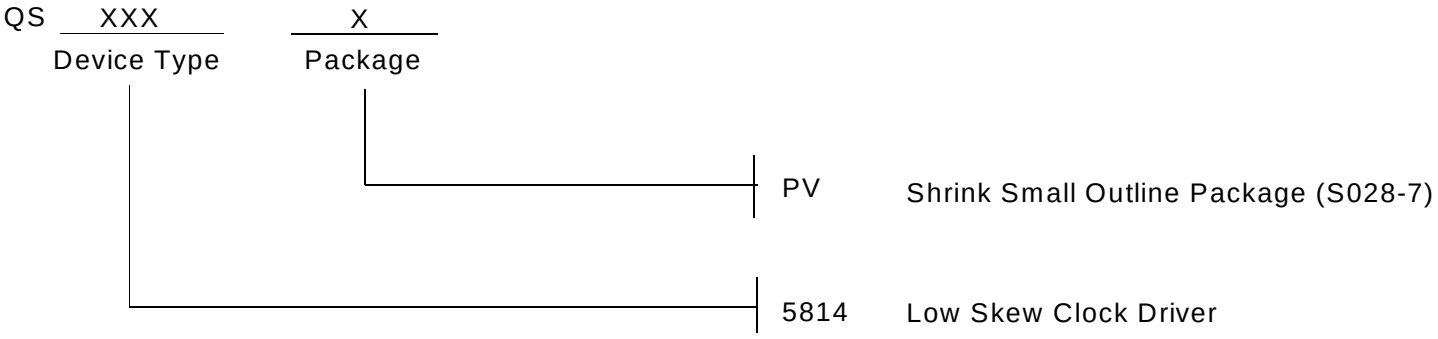
ENABLE AND DISABLE TIMES



PROPAGATION DELAY



ORDERING INFORMATION



CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com*

**To search for sales office near you, please click the sales button found on our home page or dial the 800# above and press 2.*