# LOW SKEW PLL CLOCK DRIVER TURBOCLOCK™ JR.

**QS59910**

## FEATURES:

- Eight zero delay outputs
- Selectable positive or negative edge synchronization
- Synchronous output enable
- Output frequency: 25MHz to 85MHz
- TTL outputs
- 3 skew grades:
  QS59910-2: $t_{SKEW0}$ <250ps
  QS59910-5: $t_{SKEW0}$ <500ps
  QS59910-7: $t_{SKEW0}$ <750ps
- 3-level input for PLL range control
- PLL bypass for DC testing
- External feedback, internal loop filter
- 46mA $I_{OL}$ high drive outputs
- Low Jitter: <200ps peak-to-peak
- Outputs drive 50Ω terminated lines
- Pin compatible with Cypress CY7B9910
- Available in SOIC Package

## DESCRIPTION:

The QS59910 is a high fanout phase lock loop clock driver intended for high performance computing and data-communications applications. The QS59910 has eight zero delay TTL outputs.

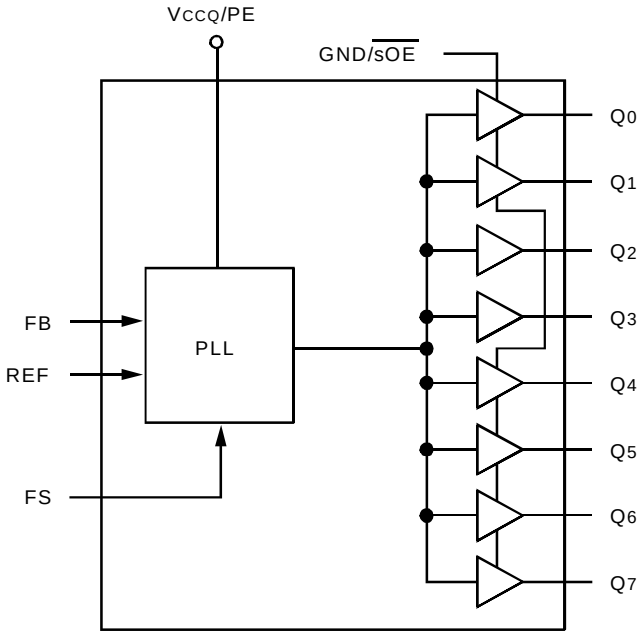
The QS59910 maintains Cypress CY7B9910 compatibility while providing two additional features: Synchronous Output Enable (GND/$\overline{sOE}$), and Positive/Negative Edge Synchronization ($V_{CCQ}$/PE). When the GND/$\overline{sOE}$ pin is held low, all the outputs are synchronously enabled (CY7B9910 compatibility). However, if GND/$\overline{sOE}$ is held high, all the outputs except Q2 and Q3 are synchronously disabled.

Furthermore, when the $V_{CCQ}$/PE is held high, all the outputs are synchronized with the positive edge of the REF clock input (CY7B9910 compatibility). When $V_{CCQ}$/PE is held low, all the outputs are synchronized with the negative edge of REF.

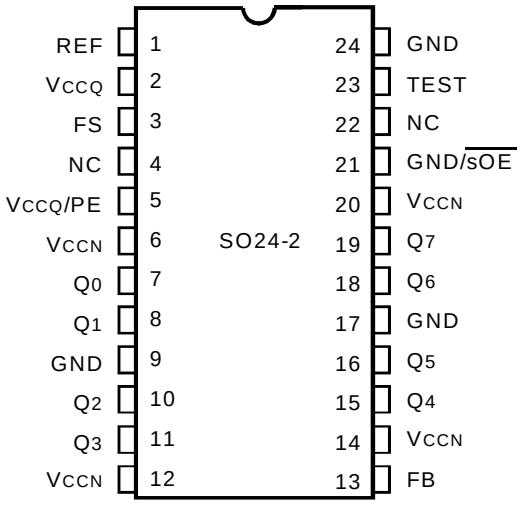
The FB signal is compared with the input REF signal at the phase detector in order to drive the VCO. Phase differences cause the VCO of the PLL to adjust upwards or downwards accordingly.

An internal loop filter moderates the response of the VCO to the phase detector. The loop filter transfer function has been chosen to provide minimal jitter (or frequency variation) while still providing accurate responses to input frequency changes.

## FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION




**SOIC**
**TOP VIEW**

## ABSOLUTE MAXIMUM RATINGS (1)

| Symbol | Rating | Max. | Unit |
|---|---|---|---|
| | Supply Voltage to Ground | –0.5 to +7 | V |
| $V_I$ | DC Input Voltage | –0.5 to +7 | V |
| | Maximum Power Dissipation ($T_A$ = 85°C) | 530 | mW |
| $T_{STG}$ | Storage Temperature Range | –65°C to +150°C | °C |

**NOTE:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## CAPACITANCE ($T_A$ = 25° C, f = 1MHz, $V_{IN}$ = 0V)

| Parameter | Description | Typ. | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 5 | 7 | pF |

**NOTE:**
1. Capacitance applies to all inputs except TEST and FS. It is characterized but not production tested.

## PIN DESCRIPTION

| Pin Name | Type | Description |
|---|---|---|
| REF | IN | Reference Clock Input |
| FB | IN | Feedback Input |
| TEST (1) | IN | When MID or HIGH, disables PLL (except for conditions of Note 1). REF goes to all outputs. Set LOW for normal operation. |
| GND/ $\overline{sOE}$ (1) | IN | Synchronous Output Enable. When HIGH, it stops clock outputs (except $Q_2$ and $Q_3$) in a LOW state - $Q_2$ and $Q_3$ may be used as the feedback signal to maintain phase lock. Set GND/$\overline{sOE}$ LOW for normal operation. |
| $V_{CCQ}$/PE | IN | Selectable positive or negative edge control. When LOW/HIGH the outputs are synchronized with the negative/positive edge of the reference clock. |
| FS (2) | IN | Frequency range select. 3 level input.<br>FS = GND: 25 to 35MHz.<br>FS = MID (or open): 35 to 60MHz<br>FS = $V_{CC}$: 60 to 85MHz |
| $Q_0$ - $Q_7$ | OUT | 8 clock output |
| $V_{CCN}$ | PWR | Power supply for output buffers |
| $V_{CCQ}$ | PWR | Power supply for phase locked loop and other internal circuitry |
| GND | PWR | Ground |

**NOTES:**
1. When TEST = MID and GND/$\overline{sOE}$ = HIGH, PLL remains active.
2. This input is wired to Vcc, GND, or unconnected. Default is MID level. If it is switched in the real time mode, the outputs may glitch, and the PLL may require an additional lock time before all data sheet limits are achieved.

## RECOMMENDED OPERATING RANGE

| Symbol | Description | QS59910-5, -7 (Industrial) | | QS59910-2 (Commercial) | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $V_{CC}$ | Power Supply Voltage | 4.5 | 5.5 | 4.75 | 5.25 | V |
| $T_A$ | Ambient Operating Temperature | -40 | +85 | 0 | +70 | °C |

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

| Symbol | Parameter | Conditions | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Logic HIGH (REF, FB Inputs Only) | | 2 | — | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Logic LOW (REF, FB Inputs Only) | | — | 0.8 | V |
| $V_{IHH}$ | Input HIGH Voltage (1) | 3-Level Inputs Only | | $V_{CC}$–1 | — | V |
| $V_{IMM}$ | Input MID Voltage (1) | 3-Level Inputs Only | | $V_{CC}$/2–0.5 | $V_{CC}$/2+0.5 | V |
| $V_{ILL}$ | Input LOW Voltage (1) | 3-Level Inputs Only | | — | 1 | V |
| $I_{IN}$ | Input Leakage Current (REF, FB Inputs Only) | $V_{IN}$ = $V_{CC}$ or GND<br>$V_{CC}$ = Max. | | — | ±5 | µA |
| $I_3$ | 3-Level Input DC Current (TEST, FS) | $V_{IN}$ = $V_{CC}$ | HIGH Level | — | ±200 | µA |
| | | $V_{IN}$ = $V_{CC}$/2 | MID Level | — | ±50 | |
| | | $V_{IN}$ = GND | LOW Level | — | ±200 | |
| $I_{PU}$ | Input Pull-Up Current ($V_{CCQ}$/PE) | $V_{CC}$ = Max., $V_{IN}$ = GND | | — | ±100 | µA |
| $I_{PD}$ | Input Pull-Down Current (GND/$\overline{sOE}$) | $V_{CC}$ = Max., $V_{IN}$ = $V_{CC}$ | | — | ±100 | µA |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min., $I_{OH}$ = –16mA | | — | — | V |
| | | $V_{CC}$ = Min., $I_{OH}$ = –40mA | | 2.4 | — | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min., $I_{OL}$ = 46mA | | — | 0.45 | V |
| $I_{OS}$ | Output Short Circuit Current (2) | $V_{CC}$ = Max., $V_O$ = GND | | — | – 250 | mA |

**NOTES:**
1. These inputs are normally wired to $V_{CC}$, GND, or unconnected. Internal termination resistors bias unconnected inputs to $V_{CC}$/2. If these inputs are switched, the function and timing of the outputs may be glitched, and the PLL may require an additional $t_{LOCK}$ time before all datasheet limits are achieved.
2. QS59910 is to be measured at 25°C with 10:1 duty cycle, one output at a time, and one second maximum.

## POWER SUPPLY CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{CCQ}$ | Quiescent Power Supply Current | $V_{CC}$ = Max., TEST = MID, REF = LOW, GND/$\overline{sOE}$ = LOW, All outputs unloaded | 10 | 40 | mA |
| $\Delta I_{CC}$ | Power Supply Current per Input HIGH | $V_{CC}$ = Max., $V_{IN}$ = 3.4V | 0.4 | 1.5 | mA |
| $I_{CCD}$ | Dynamic Power Supply Current per Output | $V_{CC}$ = Max., $C_L$ = 0pF | 100 | 160 | µA/MHz |
| $I_{TOT}$ | Total Power Supply Current | $V_{CC}$ = 5V, $F_{REF}$ = 25MHz, $C_L$ = 240pF (1) | 53 | — | mA |
| | | $V_{CC}$ = 5V, $F_{REF}$ = 33MHz, $C_L$ = 240pF (1) | 63 | — | mA |
| | | $V_{CC}$ = 5V, $F_{REF}$ = 66MHz, $C_L$ = 240pF (1) | 117 | — | mA |

**NOTE:**
1. For eight outputs, each loaded with 30pF.

## INPUT TIMING REQUIREMENTS

| Symbol | Description (1) | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_R$, $t_F$ | Maximum input rise and fall times, 0.8V to 2V | — | 10 | ns/V |
| $t_{PWC}$ | Input clock pulse, HIGH or LOW | 3 | — | ns |
| $D_H$ | Input duty cycle | 10 | 90 | % |
| $R_{EF}$ | Reference Clock Input | 25 | 85 | MHz |

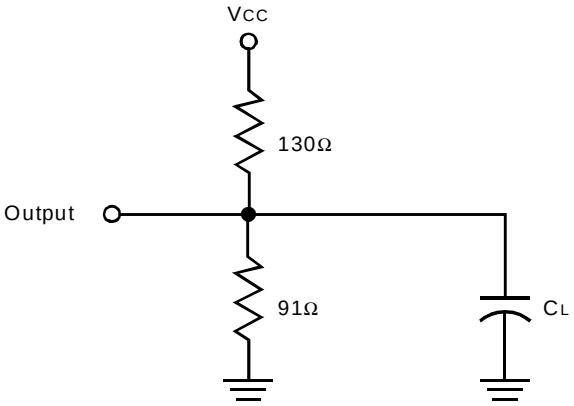
**NOTE:**
1. Where pulse width implied by $D_H$ is less than $t_{PWC}$ limit, $t_{PWC}$ limit applies.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

| Symbol | Parameter | | QS59910-2 | | | QS59910-5 | | | QS59910-7 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| $F_{REF}$ | REF Frequency Range | FS = LOW | 25 | — | 35 | 25 | — | 35 | 25 | — | 35 | MHz |
| | | FS = MID | 35 | — | 60 | 35 | — | 60 | 35 | — | 60 | |
| | | FS = HIGH | 60 | — | 85 | 60 | — | 85 | 60 | — | 85 | |
| $t_{RPWH}$ | REF Pulse Width HIGH (1,7) | | 3 | — | — | 3 | — | — | 3 | — | — | ns |
| $t_{RPWL}$ | REF Pulse Width LOW (1,7) | | 3 | — | — | 3 | — | — | 3 | — | — | ns |
| $t_{SKEW}$ | Zero Output Skew (All Outputs) (1,3) | | — | 0.1 | 0.25 | — | 0.25 | 0.5 | — | 0.3 | 0.75 | ns |
| $t_{DEV}$ | Device-to-Device Skew (1,2,4) | | — | — | 0.75 | — | — | 1.25 | — | — | 1.65 | ns |
| $t_{PD}$ | REF Input to FB Propagation Delay (1,6) | | –0.25 | 0 | 0.25 | –0.5 | 0 | 0.5 | –0.7 | 0 | 0.7 | ns |
| $t_{ODCV}$ | Output Duty Cycle Variation from 50% (1) | | –1.2 | 0 | 1.2 | –1.2 | 0 | 1.2 | –1.2 | 0 | 1.2 | ns |
| $t_{ORISE}$ | Output Rise Time (1) | | 0.15 | 1 | 1.5 | 0.15 | 1 | 1.5 | 0.15 | 1.5 | 2.5 | ns |
| $t_{OFALL}$ | Output Fall Time (1) | | 0.15 | 1 | 1.5 | 0.15 | 1 | 1.5 | 0.15 | 1.5 | 2.5 | ns |
| $t_{LOCK}$ | PLL Lock Time (5) | | — | — | 0.5 | — | — | 0.5 | — | — | 0.5 | ms |
| $t_{JR}$ | Cycle-to-Cycle Output Jitter | RMS | — | — | 25 | — | — | 25 | — | — | 25 | ps |
| | | Peak-to-Peak | — | — | 200 | — | — | 200 | — | — | 200 | |

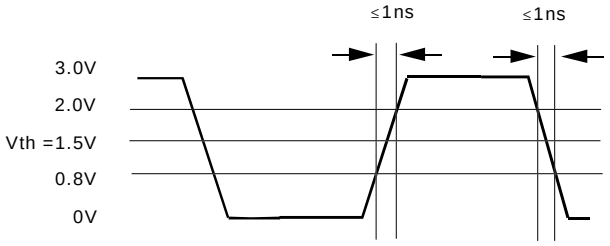
**NOTES:**
1. All timing tolerances apply for $F_{NOM} \geq 25$MHz.
2. Skew is the time between the earliest and the latest output transition among all outputs with the specified load.
3. $t_{SKEW}$ is the skew between all outputs. See AC test loads.
4. $t_{DEV}$ is the output-to-output skew between any two devices operating under the same conditions ($V_{CC}$, ambient temperature, air flow, etc.)
5. $t_{LOCK}$ is the time that is required before synchronization is achieved. This specification is valid only after $V_{CC}$ is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until $t_{PD}$ is within specified limits.
6. $t_{PD}$ is measured with REF input rise and fall times (from 0.8V to 2V) of 1ns.
7. Refer to Input Timing Requirements for more detail.

## AC TEST LOADS AND WAVEFORMS

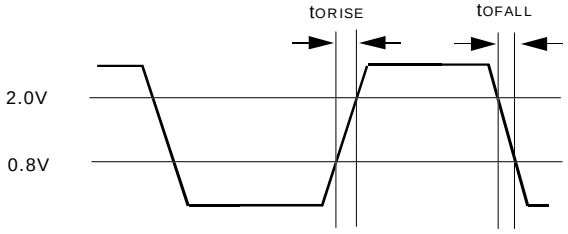



$C_L$ = 50pF ($C_L$ = 30pF for -2 and -5 devices)

**TEST LOAD**

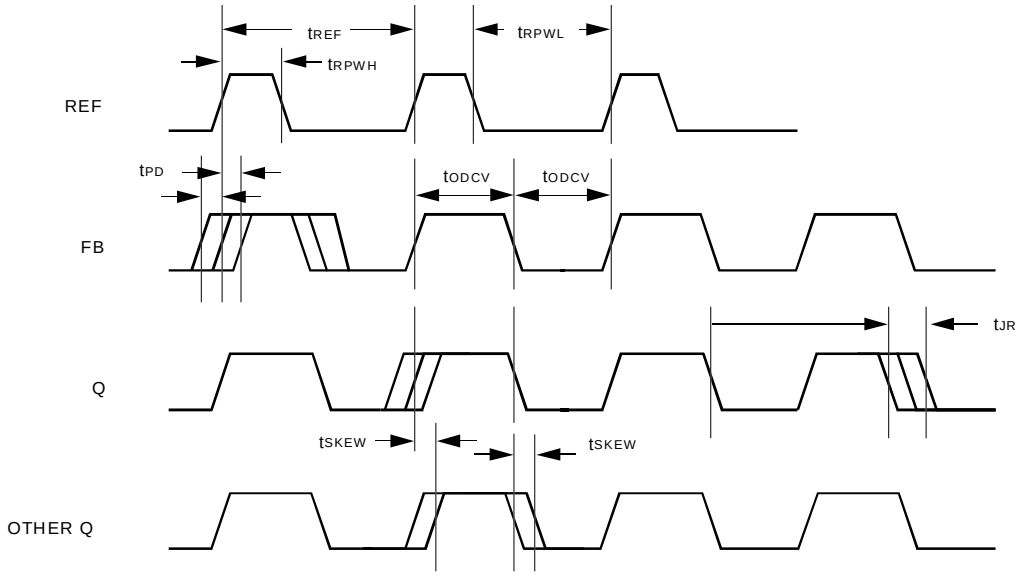



**TTL INPUT TEST WAVEFORM**




**TTL OUTPUT WAVEFORM**

## AC TIMING DIAGRAM




**NOTES:**

Skew: The time between the earliest and the latest output transition among all outputs when all are loaded with 50pF (30pF for -2 and -5) and terminated with 50Ω to 2.06V.

$t_{SKEW}$: The skew between all outputs.

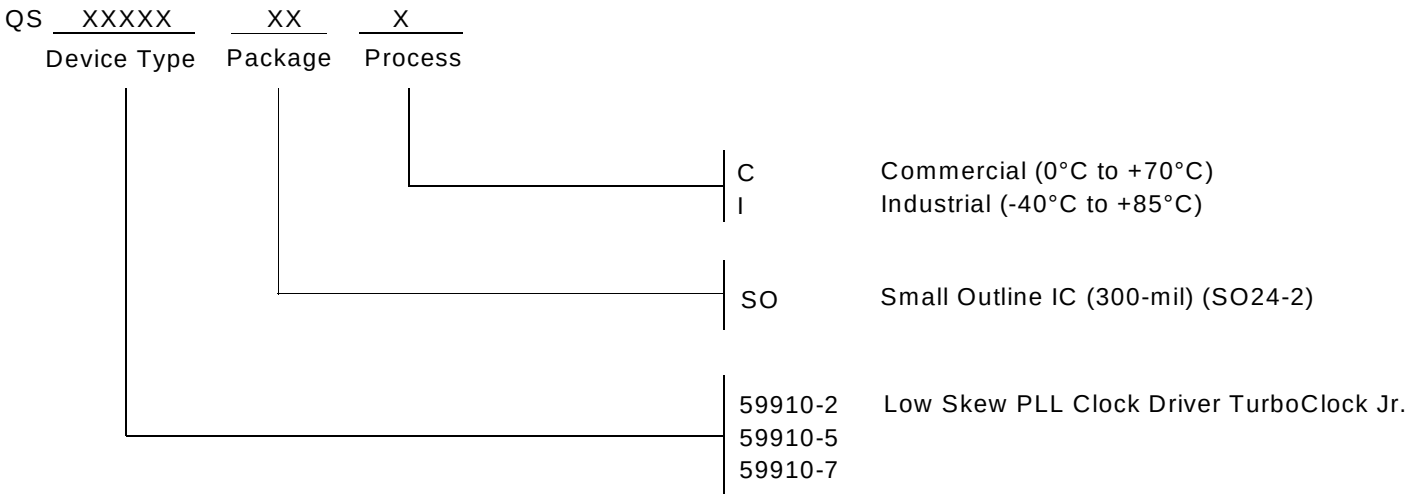
$t_{DEV}$: The output-to-output skew between any two devices operating under the same conditions ($V_{CC}$, ambient temperature, air flow, etc.)

$t_{ODCV}$: The deviation of the output from a 50% duty cycle.

$t_{ORISE}$ and $t_{OFALL}$ are measured between 0.8V and 2V.

$t_{LOCK}$: The time that is required before synchronization is achieved. This specification is valid only after $V_{CC}$ is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until $t_{PD}$ is within specified limits.

# ORDERING INFORMATION

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