## FEATURES

## Specified for $V_{\text {DD }}$ of 2.7 V to 5.25 V

Throughput rate of 1MSPS
Low Power:
tbd mW typ at tbdMSPS with 3V Supplies
8.6 mW typ at 1MSPS with 5V Supplies Wide Input Bandwidth:

70dB typ SNR at 100kHz Input Frequency +2.5V Intemal Reference
On-chip CLK oscillator
Flexible Power/ Throughput Rate Management No Pipeline Delays
High Speed Parallel Interface
Sleep Mode: 50nA typ.
24-Pin SOIC and TSSOP Packages

## GENERAL DESCRIPTION

The AD 7492 is a 12-bit high speed, low power, succes-sive-approximation ADC. The part operates from a single 2.7 V to 5.25 V power supply and feature throughput rates up to 1M SPS. The part contains a low-noise, wide bandwidth track/hold amplifier which can handle bandwidths up to 10 MHz .
The conversion process and data acquisition are controlled using standard control inputs allowing easy interfacing to microprocessors or DSPs. The input signal is sampled on the falling edge of CONVST and conversion is also initiated at this point. The BUSY goes high at the start of conversion and goes low 810ns later to indicate that the conversion is complete. There are no pipeline delays associated with the part. The conversion result is accessed via standard $\overline{\mathrm{CS}}$ and $\overline{\mathrm{RD}}$ signals over a high speed parallel interface.
The AD 7492 uses advanced design techniques to achieve very low power dissipation at high throughput rates. With 3V supplies and tbd MSPS throughput rate, on average the AD 7492 consumes typically just tbd mA. With 5V supplies and 1M SPS, the average current consumption is typically 1.72 mA . The part also offers flexible power/ throughput rate management. Operating the AD 7492 with 3 V supplies and 500 ksps throughput reduces the current consumption to tbd $\mu \mathrm{A}$. At 5 V supplies and 500 ksps , the part consumes 1.24 mA .
It is also possible to operate the part in a full sleep mode and a partial sleep mode, where the part wakes up to do a conversion and automatically enters a sleep mode at the end of conversion. The type of sleep mode is hardware

selected by the PS/FS pin. Using these sleep modes allow very low power dissipation numbers at lower throughput rates. In this mode, the AD7492 can be operated with 3V supplies at 100 ksps , and consume an average current of just tbd uA. At 5 V supplies and 100 ksps , the average current consumption is $230 \mu \mathrm{~A}$.
The analog input range for the part is 0 to REF IN. The +2.5 V reference is supplied internally and is available for external referencing. The conversion rate is determined by the internal clock.

## PRODUCT HIGHLIGHTS

1. High Throughput with Low Power Consumption. The AD7492 offers 1MSPS throughput with 4 mW power consumption.
2. Flexible Power/T hroughput $R$ ate $M$ anagement

The conversion time is determined by an internal clock. The part also features two sleep modes, partial \& full, to maximize power efficiency at lower throughput rates.
3.No Pipeline Delay.

The part features a standard successive-approximation ADC with accurate control of the sampling instant via a CONVST input and once off conversion control.
4.F lexible Digital Interface.

The $\mathrm{V}_{\text {DRIVE }}$ feature controls the voltage levels on the I/O digital pins.
5.Fewer Peripheral Components.

The AD7492 optimizes pcb space by using an internal Ref and internal CLK.

REV. PrA 10/99

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## NOTES

${ }^{1} \mathrm{~T}$ emperaturerangesasfollows: A Version:- $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$.
${ }^{4}$ Sampletested $@+25^{\circ} \mathrm{C}$ toensurecompliance.
${ }^{5}$ SeePowerv. T hroughputRatesection.
Specificationssubjecttochangewithoutnotice.

## TMINGSPECIFICATIONS ${ }^{1}{ }_{\left(V_{00}=\right.}=+2.7 \mathrm{~V}_{\text {to }}+5.25, \mathrm{~T}_{\mathrm{A}}=T_{\text {mum }}$ to $T_{\text {wex }}$ unless otherwise noted.)

| Parameter | Limit at $\mathrm{T}_{\text {min }}, \mathrm{T}_{\text {max }}$ AD7492 | Units | Description |
| :---: | :---: | :---: | :---: |
| tconvert | 810 | ns max |  |
| $\mathrm{t}_{\text {Wakeup }}$ | 1 | $\mu \mathrm{s}$ max | Partial Sleep Wake-Up Time |
|  | 500 | $\mu \mathrm{s}$ max | Full Sleep Wake-Up Time |
| $t_{1}$$t_{2}{ }^{2}$ | 10 | ns min | CONVST Pulsewidth |
|  | 10 | ns max | $\overline{\text { CONVST }}$ to BUSY Delay, $\mathrm{V}_{\text {D }}=5 \mathrm{~V}$ |
|  | 30 | ns max | CONVST to BUSY Delay, $\mathrm{V}_{\mathrm{DD}}=3 \mathrm{~V}$ |
| $t_{3}$ | 0 | ns max | BUSY to $\overline{C S}$ Setup Time |
| $t_{4}{ }^{3}$ | 0 | ns max | $\overline{\mathrm{CS}}$ to $\overline{\mathrm{RD}}$ Setup Time |
| $\mathrm{t}_{5}$ | 20 | ns min | $\overline{\mathrm{RD}}$ Pulsewidth |
| $\mathrm{t}_{6}{ }^{3}$ | 15 | ns min | Data Access Time After Falling Edge of $\overline{\mathrm{RD}}$ |
| $\mathrm{t}_{7}{ }^{4}$ | 8 | ns max | Bus Relinquish Time After Rising Edge of $\overline{\mathrm{RD}}$ |
| $\mathrm{t}_{8}$ | 0 | ns max | $\overline{\mathrm{CS}}$ to $\overline{\mathrm{RD}} \mathrm{H}$ old T ime |
| $\mathrm{t}_{9}$ | 140 | ns min | Acquisition Time |
| $\mathrm{t}_{10}$ | 100 | ns min | Quiet Time |

NOTES
${ }^{1}$ Sample tested at $+25^{\circ} \mathrm{C}$ to ensure compliance. All input signals are specified with $\mathrm{tr}=\mathrm{tf}=5 \mathrm{~ns}\left(10 \%\right.$ to $90 \%$ of $\left.\mathrm{V}_{\mathrm{DD}}\right)$ and timed from a voltage level of 1.6 V . See Figure 1.
${ }^{2} \mathrm{t}_{2}$ is 35 ns max @ $+125^{\circ} \mathrm{C}$.
${ }^{3} \mathrm{M}$ easured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.8 V or 2.0 V .
${ }^{4} \mathrm{t}_{7}$ is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1 . The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. T his means that the time, $\mathrm{t}_{7}$, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

Specifications subject to change without notice.


Figure 1. Load Circuitfor Digital Output Timing Specifications

## ABSOLUTE MAXIMUM RATINGS ${ }^{1}$

( $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}$ unless otherwise noted)

| $A V_{D D}$ to $A G N D / D G N D$ | -0.3 V to +7 V |
| :---: | :---: |
|  | -0.3 V to +7 V |
| $V_{\text {drive }}$ to AGND/DGND | -0.3 V to +7 V |
| $A V_{D D}$ to $D V_{D D}$ | -0.3 V to +0.3 V |
| $V_{\text {DRIVE }}$ to DV ${ }_{\text {DD }}$ | -0.3 V to DVDD + 0.3 V |
| AGND TO DGND | -0.3 V to +0.3 V |

Analog Input Voltage to AGND-0.3 V to AVDD +0.3 V
Digital InputVoltageto D GND $\quad-0.3 \mathrm{~V}$ to DVDD +0.3 V
REF IN to AGND $\quad-0.3 \mathrm{~V}$ to AVDD +0.3 V
Input Current to Any Pin Except Supplies ${ }^{2} \quad \pm 10 \mathrm{~mA}$
Operating Temperature Range

Commercial (A and B Version)
Storage Temperature Range

$$
-40^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C}
$$

$$
-65^{\circ} \mathrm{C} \text { to }+150^{\circ} \mathrm{C}
$$

Junction Temperature

$$
+150^{\circ} \mathrm{C}
$$

SOIC, TSSOP Package Dissipation

$$
+450 \mathrm{~mW}
$$

$\theta_{\mathrm{JA}}$ Thermal Impedance
$\theta_{\mathrm{Jc}}$ Thermal Impedance
Lead Temperature, Soldering
Vapor Phase ( 60 secs)
Infrared (15 secs)
$75^{\circ} \mathrm{C} / \mathrm{W}$ (SOIC) $115^{\circ} \mathrm{C} / \mathrm{W}$ (TSSOP)
$25^{\circ} \mathrm{C} / \mathrm{W}$ (SOIC)
$35^{\circ} \mathrm{C} / \mathrm{W}$ (TSSOP)

$$
+215^{\circ} \mathrm{C}
$$

$$
+220^{\circ} \mathrm{C}
$$

## NOTES

${ }^{1}$ Stresses abovethoselisted under A bsoluteM aximum Ratings may causepermanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions abovethoselisted in theoperational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect devicereliability.
${ }^{2}$ T ransient currents of up to 100 mA will not cause SCR latch-up.

## ORDERING GUIDE

| Model | Temperature Range | Resolution (Bits) | Package Options ${ }^{1}$ |
| :---: | :---: | :---: | :---: |
| AD 7492ARU | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 12 | RU-24 |
| AD 7492AR | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 12 | R-24 |
| EVAL-AD 7492C ${ }^{2}$ |  |  | Evaluation Board |
| EVAL-CONTROL BOARD ${ }^{3}$ |  |  | Controller Board |
| HSC-INTERFACE BOARD |  |  | Evaluation High Speed Interface |
| Board |  |  |  |

NOTES
${ }^{1} \mathrm{R}=\mathrm{SOIC} ; \mathrm{RU}=\mathrm{TSSOP}$.
${ }^{2}$ This can be used as a stand-alone evaluation board or in conjunction with the EVAL-CONTROL BOARD for evaluation/demonstration purposes.
${ }^{3}$ This board is a complete unit allowing a $P C$ to control and communicate with all Analog $D$ evices evaluation boards ending in the $C B$ designators.

## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulateon the human body and test equipment and can discharge without detection. Although the AD 7492 features proprietary ESD protection circuitry, permanent damagemay occur on devices subjected to high energy electrostatic discharges. T herefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

## Preliminary Technical Data

## PIN FUNCTION DESCRIPTION

| Pin <br> Mnemonic | Function |
| :---: | :---: |
| $\overline{\bar{C}} \bar{S}$ | Chip Select. Active low logic input used in conjunction with $\overline{\mathrm{RD}}$ to access the conversion result. The conversion result is placed on the data bus following the falling edge of both $\overline{\mathrm{CS}}$ and $\overline{\mathrm{RD}} . \overline{\mathrm{CS}}$ and $\overline{\mathrm{RD}}$ are both connected to the same AND gate on the input so the signals are interchangeable. $\overline{\mathrm{CS}}$ can be hardwired permanently low. |
| $\overline{\mathrm{R}} \overline{\mathrm{D}}$ | Read Input. Logic Input used in conjunction with $\overline{\mathrm{CS}}$ to access the conversion result. The conversion result is placed on the data bus following the falling edge of both $\overline{\mathrm{CS}}$ and $\overline{\mathrm{RD}} . \overline{\mathrm{CS}}$ and $\overline{\mathrm{RD}}$ are both connected to same AND gate on the input so the signals are interchangeable. $\overline{\mathrm{CS}}$ and $\overline{\mathrm{RD}}$ can be hardwired permanently low in which case, the data bus is always active and the result of the new conversion is clocked out slightly before to the BUSY line going low. |
| $\overline{\mathrm{C}} \overline{\mathrm{O}} \overline{\mathrm{N}} \overline{\mathrm{V}} \overline{\mathrm{S}} \overline{\mathrm{T}}$ | Conversion Start Input. Logic Input used to initiate conversion. The input track/hold amplifier goes from track mode to hold mode on the falling edge of $\overline{\text { CONVST }}$ and the conversion process is initiated at this point. The conversion input can be as narrow as 15 ns . If the CONVST input is kept low for the duration of conversion and is still low at the end of conversion, the part will automatically enter a sleep mode. The type of sleep mode is determined by the $\mathrm{PS} / \overline{\mathrm{FS}}$ pin. If the part enters a sleep mode, the next rising edge of CONVST wakes up the part. Wake-up time for the part is typically $1 \mu \mathrm{~s}$. |
| PS/ $\overline{\mathrm{F}} \bar{S}$ | Partial sleep/full sleep mode. This pin determines the type of sleep mode the part will enter if the CONVST pin is kept low for the duration of the conversion and is still low at the end of conversion. In partial sleep mode the internal reference circuit and oscillator circuit is not powered down and draws typically $200 \mu \mathrm{~V}$. In full sleep mode all of the analog circuitry is powered down and the current drawn is negligible. |
| BU SY | BUSY Output. Logic Output indicating the status of the conversion process. The BUSY signal goes high after the falling edge of $\overline{\text { CONVST }}$ and stays high for the duration of conversion. Once conversion is complete and the conversion result is in the output register, the BUSY line returns low. The track/ hold returns to track mode just prior to the falling edge of BUSY and the acquisition time for the part begins when BUSY goes low. If the CONVST input is still low when BUSY goes low, the part automatically enters its sleep mode on the falling edge of BUSY. |
| REF OUT | Reference Out. The output voltage from this pin is $2.5 \mathrm{~V} \pm 1 \%$. |
| $A V_{D D}$ | Analog Supply Voltage, +2.7 V to +5.25 V . This is the only supply voltage for all analog circuitry on the $A D 7492$. The $A V_{D D}$ and $D V_{D D}$ voltages should ideally be at the same potential and must not be more than 0.3 V apart even on a transient basis. This supply should be decoupled to AGND. |
| DV ${ }_{\text {D }}$ | Digital Supply Voltage, +2.7 V to +5.25 V . This is the supply voltage for all digital circuitry on the AD 7492 apart from the output drivers and input circuitry. $T$ he $D V_{D D}$ and $A V_{D D}$ voltages should ideally be at the same potential and must not be more than 0.3 V apart even on a transient basis. This supply should be decoupled to DGND. |
| AGND | Analog Ground. Ground reference point for all analog circuitry on the AD7492. All analog input signals should be referred to this AGND voltage. The AGND and DGND voltages should ideally be at the same potential and must not be more than 0.3 V apart even on a transient basis. |
| D G N D | Digital Ground. This is the ground reference point for all digital circuitry on the AD7492. The DGND and AGND voltages should ideally be at the same potential and must not be more than 0.3 V apart even on a transient basis. |
| $V_{\text {IN }}$ | Analog Input. Single-ended analog input channel. The input range is 0 V to REFIN. The analog input presents a high dc input impedance. |
| $V_{\text {Drive }}$ | Supply Voltage for the Output Drivers and Digital Input circuitry, +2.7 V to +5.25 V . This voltage determines the output high voltage for the data output pins and the trigger levels for the digital inputs. It allows the $A V_{D D}$ and $D V_{D D}$ to operate at 5 V (and maximize the dynamic performance of the $A D C$ ) while the digital input and output pins can interface to 3 V logic. |
| D B 0-D B 11 | Data Bit 0 to DB11. Parallel digital outputs that provide the conversion result for the part. These are three-state outputs that are controlled by $\overline{\mathrm{CS}}$ and $\overline{\mathrm{RD}}$. The output high voltage level for these outputs is determined by the $\mathrm{V}_{\text {drive }}$ input. |

## TERMINOLOGY

## Integral Nonlinearity

This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point $1 / 2$ LSB below the first code transition, and full scale, a point $1 / 2$ LSB above the last code transition.
Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

## Offset Error

This is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, i.e., AGND + 1 LSB.

## Gain Error

The last transition should occur at the analog value $11 / 2$ LSB below the nominal full scale. The first transition is a 1/2 LSB above the low end of the scale (zero in the case of AD7492). The gain error is the deviation of the actual difference between the first and last code transitions from the ideal difference between the first and last code transitions with offset errors removed.

## Track/Hold Acquisition Time

The track/hold amplifier returns into track mode after the end of conversion. Track/H old acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within $\pm 1$ LSB, after the end of conversion.

## Signal to (Noise + Distortion) Ratio

This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. $N$ oise is the sum of all nonfundamental signals up to half the sampling frequency ( $\mathrm{f}_{\mathrm{s}} / 2$ ), excluding dc . The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N -bit converter with a sine wave input is given by:

$$
\text { Signal to }(N \text { oise }+ \text { Distortion })=(6.02 N+1.76) d B
$$

Thus for a 12 -bit converter, this is 74 dB and for a 10-bit converter is 62 dB .

## Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7492 it is defined as:

$$
\operatorname{THD} \quad(\mathrm{dB})=20 \log \frac{\sqrt{\left(\mathrm{~V}_{2}^{2}+\mathrm{V}_{3}^{2}+\mathrm{V}_{4}^{2}+\mathrm{V}_{5}^{2}+\mathrm{V}_{6}^{2}\right)}}{\mathrm{V}_{1}}
$$

where $V_{1}$ is the rms amplitude of the fundamental and $V_{2}$, $V_{3}, V_{4}, V_{5}$ and $V_{6}$ are the rms amplitudes of the second through the sixth harmonics.

## Preliminary Technical Data

## Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $\mathrm{f}_{\mathrm{s}} / 2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

## Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of $\mathrm{mfa} \pm \mathrm{nfb}$ where $\mathrm{m}, \mathrm{n}=0,1,2,3$, etc. Intermodulation distortion terms are those for which neither $m$ nor $n$ is equal to zero. For example, the second order terms include ( $\mathrm{fa}+\mathrm{fb}$ ) and ( $\mathrm{fa}-\mathrm{fb}$ ), while the third order terms include $(2 \mathrm{fa}+\mathrm{fb})$, $(2 \mathrm{fa}-\mathrm{fb})$, $(\mathrm{fa}+2 \mathrm{fb})$ and $(\mathrm{fa}-2 \mathrm{fb})$.
The AD7492 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dB .

## Aperture Delay

In a sample/hold, the time required after the hold command for the switch to open fully is the aperture delay. The sample is, in effect, delayed by this interval, and the hold command would have to be advanced by this amount for precise timing.

## Aperture Jitter

A perture jitter is the range of variation in the aperture delay. In other words, it is the uncertainty about when the sample is taken. Jitter is the result of noise which modulates the phase of the hold command. This specification establishes the ultimate timing error, hence the maximum sampling frequency for a given resolution. This error will increase as the input $\mathrm{dV} / \mathrm{dt}$ increases.

## Preliminary Technical Data

## CIRCUIT DESCRIPTION CONVERTER OPERATION

The AD 7492 is a 12 -bit successive approximation analog-to-digital converter based around a capacitive DAC. The AD 7492 can convert analog input signals in the range 0 V to $\mathrm{V}_{\text {REF }}$. Figure 2 shows a very simplified schematic of the ADC. The Control Logic, SAR and the Capacitive DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition.


Figure 2. Simplified Block Diagram of AD7492
Figure 3 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in Position A. The comparator is held in a balanced condition and the sampling capacitor acquires the signal on $\mathrm{V}_{\mathrm{IN}_{\mathrm{N}}}$.


Figure 3. ADC Acquisition Phase
Figure 4 shows the ADC during conversion. When conversion starts SW2 will open and SW1 will move to position $B$, causing the comparator to become unbalanced. The ADC then runs through its successive approximation routine and brings the comparator back into a balanced condition. When the comparator is rebalanced, the conversion result is available in the SAR register.


Figure 4. ADC Conversion Phase

## TYPICAL CONNECTION DIAGRAM

Figure 5 shows a typical connection diagram for the AD 7492. Conversion is initiated by a falling edge on $\overline{\text { CONVST. Once }} \overline{\text { CONVST }}$ goes low the BUSY signal goes high, and at the end of conversion the falling edge of BUSY is used to activate an Interrupt Service Routine. The $\overline{\mathrm{CS}}$ and $\overline{\mathrm{RD}}$ lines are then activated in parallel to read the 12-data bits. The internal bandgap reference voltage is 2.5 V providing an analog input range of 0 V to 2.5 V , making the AD7492 a unipolar A/D. A capacitor with a minimum capacitance of 100 nF is needed at the output of the REF OUT pin as it stabilizes the internal reference value. It is recommended to perform a dummy conversion after power-up as the first conversion result could be incorrect. This also ensures that the part is in the correct mode of operation. The CONVST pin should not be floating when power is applied as a rising edge on CON VST might not wake up the part.

In Figure 5 the $V_{\text {Drive }}$ pin is tied to $D V_{D D}$, which results in logic output voltage values being either 0 V or DV DD. The voltage applied to $\mathrm{V}_{\text {dRIVe }}$ controls the voltage value of the output logic signals and the input logic signals. For example, if $\mathrm{DV}_{\text {DD }}$ is supplied by a 5 V supply and $\mathrm{V}_{\text {DRIVe }}$ by a 3 V supply, the logic output voltage levels would be either 0 V or 3 V . This feature allows the AD 7492 to interface to 3


V parts while still enabling the $A / D$ to process signals at 5 V supply.

Figure 5. Typical Connection Diagram

## AD7492

## ADC TRANSFER FUNCTION

The output coding of the AD 7492 is straight binary. The designed code transitions occur at successive integer LSB values (i.e., 1 LSB, 2 LSB, etc.). The LSB size is = (REF IN)/4096 for the AD7492. The ideal transfer characteristic for the AD7492 is shown in Figure 6.


Figure 6. Transfer Characteristic for 12 Bits

## AC ACQUISITION TIME

In ac applications it is recommended to always buffer ana$\log$ input signals. The source impedance of the drive circuitry must be kept as low as possible to minimize the acquisition time of the ADC. Large values of impedance at the VIN pin of the ADC will cause the THD to degrade at high input frequencies.

| INPUT BUFFERS | AD7492 <br> DYNAMIC <br> PERFORMANCE <br> SPECIFICATIONS |  | TYPICAL AMPLIFIER CURRENT CONSUMPTION |
| :---: | :---: | :---: | :---: |
|  | SNR <br> 500 kHz | THD <br> 500 kHz |  |
| AD8047 | 70 | 78 | 5.8 mA |
| AD9631 | 69.5 | 80 | 17 mA |
| AD8051 | 68.6 | 78 | 4.4 mA |
| AD797 | 70 | 84 | 8.2 mA |

## DC Acquisition Time

The ADC starts a new acquisition phase at the end of a conversion and ends it on the falling edge of the $\overline{\text { CONVST }}$ signal. At the end of conversion there is a settling time associated with the sampling circuit. This settling time lasts approximately 140 ns . The analog signal on $\mathrm{V}_{\text {IN }}$ is also being acquired during this settling time; therefore, the minimum acquisition time needed is approximately 140 ns.
Figure 8 shows the equivalent charging circuit for the sampling capacitor when the ADC is in its acquisition phase. R3 represents the source impedance of a buffer amplifier or resistive network, R1 is an internal switch resistance, R2 is for bandwidth control and C1 is the sampling capacitor. C2 is back-plate capacitance and switch parasitic capacitance.
During the acquisition phase the sampling capacitor must be charged to within 1 LSB of its final value.


Figure 8. EquivalentSampling Circuit

## ANALOG INPUT

Figure 9 shows the equivalent circuit of the analog input structure of the AD7492. The two diodes, D 1 and D2, provide ESD protection for the analog inputs. The capacitor C3 is typically about 4 pF and can be primarily attributed to pin capacitance. The resistor R1 is an internal switch resistance. This resistor is typically about 125 ohms. The capacitor C1 is the sampling capacitor while R2 is used for bandwidth control.


Figure 9. EquivalentAnalog Input Circuit

## Preliminary Technical Data

## PARALLEL INTERFACE

The parallel interface of the AD7492 is 12 -bits wide. The output data buffers are activated when both $\overline{\mathrm{CS}}$ and $\overline{\mathrm{RD}}$ are logic low. At this point the contents of the data register are placed onto the data bus. Figure 10 shows the timing diagram for the parallel port.
Figure 11 shows the timing diagram for the parallel port when $\overline{\mathrm{CS}}$ and $\overline{\mathrm{RD}}$ are tied permanently low. In this setup, once the BUSY line goes from high to low the conversion process is
completed. The data is available on the output bus slightly before the falling edge of BUSY.
It is important to point out that data bus cannot change state while the A/D is doing a conversion as this would have a detrimental effect on the conversion in progress. The data out lines will go three-state again when either the $\overline{\mathrm{RD}}$ or $\overline{\mathrm{CS}}$ line goes high. Thus the $\overline{\mathrm{CS}}$ can be tied low permanently, leaving the $\overline{\mathrm{RD}}$ line to control conversion result access. Please reference the $\mathrm{V}_{\text {Drive }}$ section for output voltage levels.


Figure 10. Parallel Port Timing


Figure 11. Parallel Port Timing with CS and RD Tied Low


Figure 13. Mode 2 Operation

## OPERATING MODES

The AD7492 has two possible modes of operation depending on the state of the CONVST pulse at the end of a conversion, Mode 1 and Mode 2.

## Mode 1 (High Speed Sampling)

In this mode of operation the $\overline{\text { CONVST }}$ pulse is brought high before the end of conversion i.e., before the BUSY goes low (see Figure 10). If the CONVST pin is brought from high to low while BUSY is high, the conversion is restarted. When operating in this mode a new conversion should not be initiated until 135 ns after BUSY goes low. This acquisition time allows the track/hold circuit to accurately acquire the input signal. As mentioned earlier, a read should not be done during a conversion. This mode facilitates the fastest throughput times for the AD 7492.

## Mode 2 (Partial or Full Sleep Mode)

Figure 13 shows AD 7492 in M ode 2 operation where the ADC goes into either partial or full sleep mode after conversion. The CONVST line is brought low to initiate a conversion and remains low until after the end of conversion. If CONVST goes high and low again while BUSY is high, the conversion is restarted. Once the BUSY line goes from a high to a low, the CONVST line has its status checked and, if low, the part enters a sleep mode. The type of sleep mode the AD 7492 enters depends on what ever way the $P S / \overline{F S}$ pin is hardwired. If the PS/FS pin is tied high then the AD 7492 will enter partial sleep mode. If the $\mathrm{PS} / \overline{\mathrm{FS}}$ pin is tied low the AD 7492 will enter full sleep mode.

The device wakes up again on the rising edge of the CONVST signal. From partial sleep the wake-up time is typically $1 \mu s$ after the rising edge of $\overline{\text { CONVST }}$ and before the BUSY line can go high to indicate start of conversion. From full sleep this wake-up time is typically $500 \mu \mathrm{~S}$. BUSY will only go high once CONVST goes low. The CONVST line can go from a high to a low during the wake-up time, but the conversion will still not be initiated until after the wake-up time. Superior power performance can be achieved in these modes of operation by waking up the AD 7492 only to carry out a conversion. The optimum power performance is obtained when using full sleep mode as the ADC comparator, Reference buffer and Reference
circuit is powered down. While in partial sleep mode, only the ADC comparator is powered down and the reference buffer is put into a low power mode. The 100 nF capacitor on the REF OUT pin is kept charged up by the reference buffer in partial sleep mode while in full sleep mode this capacitior slowly discharges. This explains why the wake-up time is shorter in partial sleep mode. In both sleep modes the clock oscillator circuit is powered down.

## $V_{\text {drive }}$

The $V_{\text {Drive }}$ pin is used as the voltage supply to the output drivers and is a separate supply from $A V_{D D}$ and $D V_{D D}$. The purpose of using a separate supply for the output drivers is that the user can vary the output high voltage, $\mathrm{V}_{\mathrm{OH}}$, from the $\mathrm{V}_{D D}$ supply to the $A D 7492$. For example, if $A V_{D D}$ and $D V_{D D}$ is using a 5 V supply, the $\mathrm{V}_{\text {DRIVE }}$ pin can be powered from a 3 V supply. The ADC has better dynamic performance at 5 V than at 3 V , so operating the part at 5 V , while still being able to interface to 3 V parts, pushes the AD7472 to the top bracket of high performance 12 -bit A/ Ds. Of course, the ADC can have its $V_{\text {Drive }}$ and $D_{\text {DD }}$ pins connected together and be powered from a 3 V or 5 V supply.
All outputs are powered from $\mathrm{V}_{\text {drive. }}$ These are all the data out pins and the BUSY pin.

## POWER-UP

It is recommended that the user performs a dummy conversion after power-up, as the first conversion result could be incorrect. This also ensures that the parts is in the correct mode of operation. The recommended power-up sequence is as follows:

```
l > GND 4 > Digital Inputs
2> V
3>V VRIVE
```


## Power vs. Throughput

The two modes of operation for the AD 7492 will produce different power versus throughput performances, M ode 1 and M ode 2; see Operating M odes section of the data sheet for more detailed descriptions of these modes. M ode 2 is the Sleep M ode (Partial/Full) of the part and it achieves the optimum power performance.

## Preliminary Technical Data

## Mode 1

Figure 14 shows the AD 7492 conversion sequence in M ode 1 using a throughput rate of 500 kSPS. At 5 V supply the current consumption for the part when converting is 2 mA and the quiescent current is $650 \mu \mathrm{~A}$. The conversion time of 810 ns contributes 4.05 mW to the overall power dissipation in the following way:
$(810 \mathrm{~ns} / 2 \mu \mathrm{~s}) \times(5 \times 2 \mathrm{~mA})=4.05 \mathrm{~mW}$
The contribution to the total power dissipated by the remaining $1.19 \mu \mathrm{~s}$ of the cycle is 1.93 mW .
$(1.19 \mu \mathrm{~s} / 2 \mu \mathrm{~s}) \mathrm{X}(5 \mathrm{X} 650 \mu \mathrm{~A})=1.93 \mathrm{~mW}$
Thus the power dissipated during each cycle is:

$$
4.05 \mathrm{~mW}+1.93 \mathrm{~mW}=5.98 \mathrm{~mW}
$$



Figure 14. Mode 1 Power Dissipation

## Mode 2 (Full Sleep Mode)

Figure 15 shows the AD 7492 conversion sequence in M ode 2, Full Sleep mode, using a throughput rate of approximately 1.18 kSPS. At 5 V supply the current consumption for the part when converting is 2 mA , while the full sleep current is $1 \mu \mathrm{~A}$ max. The power dissipated during this power-down is negligible and is thus not worth considering in the total power figure. During the wake-up phase, the AD 7492 will draw $650 \mu \mathrm{~A}$. Overall power dissipated is:
(810ns/550 $/ 5$ s) X ( $5 \times 2 \mathrm{~mA}$ ) $+(500 \mu \mathrm{~s} / 550 \mu \mathrm{~s}) \times(5 \mathrm{X} 650 \mu \mathrm{~A})$

$$
=2.97 \mathrm{~mW}
$$



Figure 15. Full Sleep Power Dissipation

## Mode 2 (Partial Sleep Mode)

Figure 16 shows the AD7492 conversion sequence in M ode 2, Partial Sleep mode, using a throughput rate of 500 kSPS. At 5 V supply the current consumption for the part when converting is 2 mA , while the partial sleep current is $190 \mu \mathrm{~A}$ max. During the wake-up phase, the AD 7492 will draw $650 \mu \mathrm{~A}$. Power dissipated during wakeup and conversion is :

$$
\begin{gathered}
(810 \mathrm{~ns} / 2 \mu \mathrm{~s}) \times(5 \times 2 \mathrm{~mA})+(1 \mu \mathrm{~s} / 2 \mu \mathrm{~s}) \times(5 \times 650 \mu \mathrm{~A}) \\
=5.675 \mathrm{~mW}
\end{gathered}
$$

Power dissipated during power-down is :

$$
(190 \mathrm{~ns} / 2 \mu \mathrm{~s}) \times(5 \times 190 \mu \mathrm{~A})=90.25 \mu \mathrm{~W}
$$

Overall power dissipated is :

$$
5.675 \mathrm{~mW}+90.25 \mu \mathrm{~W}=5.765 \mathrm{~mW}
$$



Figure 16. Partial Sleep Power Dissipation


## GROUNDING AND LAYOUT

The analog and digital power supplies are independent and separately pinned out to minimize coupling between analog and digital sections within the device. To complement the excellent noise performance of the AD7492 it is imperative that care be given to the PCB layout. Figure 25 shows a recommended connection diagram for the AD 7472 .
All of the AD 7492 ground pins should be soldered directly to a ground plane to minimize series inductance. The $A V_{D D}, D V_{D D}$ and $V_{\text {DRIVE }}$ pins should be decoupled to both the analog and digital ground planes. The REF OUT pin should be decoupled to the analog ground plane with a minimum capacitor value of 100 nF . This capacitor helps to stabilize the internal reference circuit. The large value capacitors will decouple low frequency noise to analog ground, the small value capacitors will decouple high frequency noise to digital ground. All digital circuitry power pins should be decoupled to the digital ground plane. The use of ground planes can physically separate sensitive analog components from the noisy digital system. The two ground planes should be joined in only one place and should not overlap so as to minimize capacitive coupling between them. If the AD 7492 is in a system where multiple devices require $A G N D$ to $D G N D$ connections, the connection should still be made at one point only, a star ground point, which should be established as close as possible to the AD7492.
Noise can be minimized by applying some simple rules to the PCB layout: analog signals should be kept away from digital signals; fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other sections of the board and clock signals should never be run near the analog inputs; avoid running digital lines under the device as these will couple noise onto the die; the power supply lines to the AD 7492 should use as large a trace as possible to provide a low impedance path and reduce the effects of glitches on the power supply line; avoid crossover of digital and analog signals and place traces that are on opposite sides of the board at right angles to each other.
$N$ oise to the analog power line can be further reduced by use of multiple decoupling capacitors as shown in Figure 25. Decoupling capacitors should be placed directly at the power inlet to the PCB and also as close as possible to the power pins of the AD7472. The same decoupling method should be used on other ICs on the PCB, with the capacitor leads as short as possible to minimize lead inductance. -12-

## POWER SUPPLIES

Separate power supplies for $A V_{D D}$ and $D V_{D D}$ are desirable but if necessary $D V_{D D}$ may share its power connection to $A V_{D D}$. The digital supply ( $D V_{D D}$ ) must not exceed the ana$\log$ supply $\left(A V_{D D}\right)$ by more than 0.3 V in normal operation.

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

## 24-Lead SOIC

(R-24)


## 24-Lead TSSOP

(RU-24)



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[^1]:    One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A. Tel: 781/329-4700 World Wide Web Site: http://www.analog.com Fax: 781/326-8703

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