Active Energy Metering IC with Serial Interface

Preliminary Technical Data — AD7756*

FEATURES

High Accuracy, supports IEC 687/1036
Less than 0.1% error over a dynamic range of 500 to 1
An On-Chip user Programmable threshold for line voltage SAG detection and PSU supervisory.
The AD7756 supplies *Sampled Waveform Data* and *Active Energy* (40 Bits).
Digital Power, Phase & Input Offset Calibration.
An On-Chip temperature sensor (±3°C typical after calibration)
A SPI compatible Serial Interface.
A pulse output with programmable frequency.
An Interrupt Request line (IRQ) and Status register provide early warning of register overflow
Proprietary ADCs and DSP provide high accuracy over large variations in environmental conditions and time.
Reference 2.5V±8% (30 ppm/°C typical) with external overdrive capability
Single 5V Supply, Low power (15mW typical)

GENERAL DESCRIPTION

The AD7756 is a high accuracy electrical power measurement IC with a serial interface and a pulse output. The AD7756 incorporates two second order sigma delta ADCs, reference circuitry, temperature sensor and all the signal processing required to perform active power and energy measurement.

The AD7756 contains a sampled waveform register and an Active Energy register capable of holding at least 5 seconds of accumulated power at full load. Data is read from the AD7756 via the serial interface. The AD7756 also provides a pulse output (CF) with a frequency which is proportional to the active power.

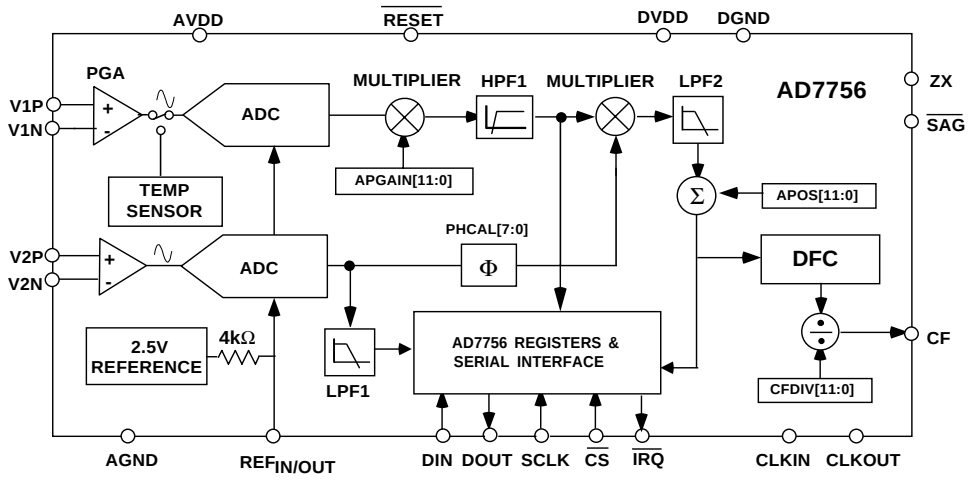
Besides real power information the AD7756 also provides system calibration features, i.e., channel offset correction, phase calibration and power calibration. The part also incorporates a detection circuit for short duration low voltage variations or sags. The voltage threshold level and the duration (no. of half line cycles) of the variation are user programmable. An open drain logic output ($\overline{SAG}$) goes active low when a sag event occurs.

A zero crossing output (ZX) produces an output which is synchronized to the zero crossing point of the line voltage. This output can be used to extract timing or frequency information from the line. The signal is also used internally to the chip in the calibration mode. This permits faster and more accurate calibration of the real power calculation. This signal is also useful for synchronization of relay switching with a voltage zero crossing, thus improving the relay life by reducing the risk of arcing.

The interrupt request output is an open drain, active low logic output. The $\overline{IRQ}$ output will become active when the accumulated real power register is half full and also when it over flows. A status register will indicate the nature of the interrupt.

The AD7756 is available in 20 pin DIP and 20 lead SSOP packages.

FUNTIONAL BLOCK DIAGRAM



*Patents Pending.

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AD7756–SPECIFICATIONS[1,3]

(AV_{DD} = DV_{DD} = 5V ± 10%, AGND = DGND = 0V, On-Chip Reference, CLKIN = 3.579545MHz XTAL, TMIN to TMAX = -40°C to +85°C)

Parameter	A Version	B Version	Units	Test Conditions/Comments
ENERGY MEASUREMENT ACCURACY				
Measuremnt Bandwidth	14	14	kHz	CLKIN = 3.579545 MHz
Measurement Error[1] on Channel 1				Channel 2 = 300mV rms/60Hz, Gain = 2
Channel 1 Range = 1V full-scale				
Gain = 1	0.2	0.1	% max	Over a dynamic range 500 to 1
Gain = 2	0.2	0.1	% max	Over a dynamic range 500 to 1
Gain = 4	0.2	0.1	% max	Over a dynamic range 500 to 1
Gain = 8	0.2	0.1	% max	Over a dynamic range 500 to 1
Gain = 16	0.2	0.1	% max	Over a dynamic range 500 to 1
Channel 1 Range = 0.5V full-scale				
Gain = 1	0.2	0.1	% max	Over a dynamic range 500 to 1
Gain = 2	0.2	0.1	% max	Over a dynamic range 500 to 1
Gain = 4	0.2	0.1	% max	Over a dynamic range 500 to 1
Gain = 8	0.2	0.1	% max	Over a dynamic range 500 to 1
Gain = 16	0.2	0.1	% max	Over a dynamic range 500 to 1
Channel 1 Range = 0.25V full-scale				
Gain = 1	0.4	0.2	% max	Over a dynamic range 500 to 1
Gain = 2	0.4	0.2	% max	Over a dynamic range 500 to 1
Gain = 4	0.4	0.2	% max	Over a dynamic range 500 to 1
Gain = 8	0.4	0.2	% max	Over a dynamic range 500 to 1
Gain = 16	0.4	0.2	% max	Over a dynamic range 500 to 1
Phase Error[1] Between Channels	±0.05	±0.05	° max	Line Frequency = 45Hz to 65Hz, HPF on
ac Power Supply Rejection[1]				AV_{DD} = DV_{DD} = 5V+175mV rms/ 60Hz
Output Frequency Variation (CF)	0.2	0.2	% typ	Channel 1 = 20mV rms, Gain = 16, Range = 0.5V Channel 2 = 300mV rms/60Hz, Gain = 2
dc Power Supply Rejection[1]				AV_{DD} = DV_{DD} = 5V ±250mV dc
Output Frequency Variation (CF)	±0.3	±0.3	% typ	Channel 1 = 20mV rms, Gain = 16, Range = 0.5V Channel 2 = 300mV rms/60Hz, Gain = 2
ANALOG INPUTS				*See Analog Inputs Section*
Maximum Signal Levels	±1	±1	V max	V1P, V1N, V2N and V2P to AGND
Input Impedance (dc)	390	390	kΩ min	CLKIN = 3.579545MHz
Bandwidth	14	14	kHz	CLKIN/256, CLKIN = 3.579545 MHz
Gain Error[1,4]				External 2.5V reference, Gain = 1 on Channel 1 & 2
Channel 1				
Range = 1V full-scale	±4	±4	% typ	V1 = 1V dc
Range = 0.5V full-scale	±4	±4	% typ	V1 = 0.5V dc
Range = 0.25V full-scale	±4	±4	% typ	V1 = 0.25V dc
Channel 2	±4	±4	% typ	V2 = 1V dc
Gain Error Match[1]				External 2.5V reference
Channel 1				
Range = 1V full-scale	±0.3	±0.3	% typ	Gain = 1, 2, 4, 8, 16
Range = 0.5V full-scale	±0.3	±0.3	% typ	Gain = 1, 2, 4, 8, 16
Range = 0.25V full-scale	±0.3	±0.3	% typ	Gain = 1, 2, 4, 8, 16
Channel 2	±0.3	±0.3	% typ	Gain = 1, 2, 4, 8, 16
Offset Error[1]				
Channel 1	±10	±10	mV max	
Channel 2	±10	±10	mV max	
WAVEFORM SAMPLING				Sampling CLKIN/128, 3.579545MHz/128 = 27.9kSPS
Channel 1				*See Channel 1 Sampling*
Signal-to-Noise plus distortion	62	62	dB typ	300mV rms/50Hz, Range = 0.5V, Gain = 2
Bandwidth (-3dB)	14	14	kHz	CLKIN = 3.579545MHz
Channel 2				*See Channel 2 Sampling*
Signal-to-Noise plus distortion	52	52	dB typ	300mV rms/50Hz, Range = 0.5V, Gain = 2
Bandwidth (-3dB)	140	140	Hz	CLKIN = 3.579545MHz

Parameter	A Version	B Version	Units	Test Conditions/Comments
REFERENCE INPUT				
$REF_{IN/OUT}$ Input Voltage Range	2.6	2.6	V max	2.4 V +8%
	2.2	2.2	V min	2.4V -8%
Input Impedance	1.7	1.7	kΩ min	
Input Capacitance	10	10	pF max	
ON-CHIP REFERENCE				Nominal 2.4V at $REF_{IN/OUT}$ pin
Reference Error	±200	±200	mV max	
Current source	10	10	µA max	
Output Impedance	6	6	kΩ min	
Temperature Coefficient	30	30	ppm/°C typ	
CLKIN				Note all specifications CLKIN of 3.579545MHz
Input Clock Frequency	4	4	MHz max	
	1	1	MHz min	
LOGIC INPUTS				
$\overline{RESET}$, DIN, SCLK, CLKIN and $\overline{CS}$				
Input High Voltage, V_{INH}	2.4	2.4	V min	DV_{DD} = 5 V ± 10%
Input Low Voltage, V_{INL}	0.8	0.8	V max	DV_{DD} = 5 V ± 10%
Input Current, I_{IN}	±3	±3	µA max	Typically 10nA, V_{IN} = 0V to DV_{DD}
Input Capacitance, C_{IN}	10	10	pF max	
LOGIC OUTPUTS[3]				
$\overline{SAG}$ & $\overline{IRQ}$				Open Drain outputs, 10kΩ pull up resistor
Output High Voltage, V_{OH}	4	4	V min	I_{SOURCE} = 200µA
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 0.8mA
ZX & DOUT				
Output High Voltage, V_{OH}	4	4	V min	I_{SOURCE} = 200µA
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 0.8mA
CF				
Output High Voltage, V_{OH}	4	4	V min	I_{SOURCE} = 10mA
Output Low Voltage, V_{OL}	1	1	V max	I_{SINK} = 10mA
POWER SUPPLY				For specified Performance
AV_{DD}	4.5	4.5	V min	5V - 10%
	5.5	5.5	V max	5V +10%
DV_{DD}	4.5	4.5	V min	5V - 10%
	5.5	5.5	V max	5V + 10%
AI_{DD}	3	3	mA max	Typically 1.5 mA
DI_{DD}	2	2	mA max	Typically 1.5 mA

NOTES:
[1]See Terminology Section for explanation of Specifications
[2]See Plots in Typical Performance Graphs
[3]Specifications subject to change without notice
[4]See Analog Inputs Section

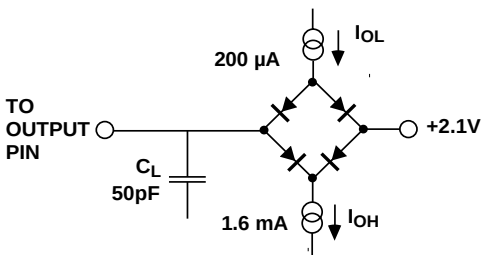


Figure 1 - Load Circuit for Timing Specifications

ODERING GUIDE

MODLE	Package Option*
AD7756AN	N-20
AD7756BN	N-20
AD7756ARS	RS-20
AD7756BRS	RS-20
EVAL-AD7756EB	AD7756 evaluation board
AD7756-REF	AD7756 Reference Design

* N = Plastic DIP; RS = Shrink Small Outline Package

AD7756 TIMING CHARACTERISTICS[1,2]

(AV_{DD} = DV_{DD} = 5V ± 10%, AGND = DGND = 0V, On-Chip Reference, CLKIN = 3.579545MHz XTAL, TMIN to TMAX = -40°C to +85°C)

Parameter	A,B Versions	Units	Test Conditions/Comments
Write timing			
t_1	20	ns (min)	$\overline{CS}$ falling edge to first SCLK falling edge
t_2	100	ns (min)	SCLK logic high pulse width
t_3	100	ns (min)	SCLK logic low pulse width
t_4	10	ns (min)	Valid Data Set up time before falling edge of SCLK
t_5	5	ns (min)	Data Hold time after SCLK falling edge
t_6	4	µs (min)	Minimum time between the end of data byte transfers.
t_7	100	ns (min)	Minimum time between byte transfers during a serial write.
t_8	100	ns (min)	$\overline{CS}$ Hold time after SCLK falling edge.
Read timing			
t_9	100	ns (min)	Minimum time between read command and data read.
t_{10}	100	ns (min)	Minimum time between data byte transfers during a multibyte read.
t_{11}[3]	30	ns (min)	Data access time after first SCLK rising edge following a write to the Communications Register
t_{12}[3]	20	ns (min)	Data access time after subsequent SCLK rising edges following a write to the Communications Register
t_{13}[4]	100	ns (max)	Bus relinquish time after falling edge of SCLK.
	10	ns (min)	
t_{14}[4]	100	ns (max)	Bus relinquish time after rising edge of $\overline{CS}$.
	10	ns (min)	
t_{15}	4	µs (min)	Minimum time between end of a write transfer and the start of a read transfer (i.e., write to communications register)

NOTES

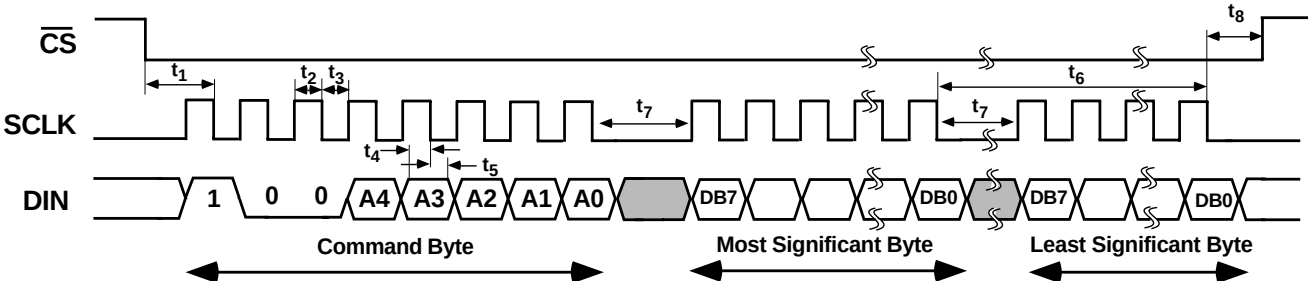
[1] Sample tested during initial release and after any redesign or process change that may affect this parameter. All input signals are specified with tr = tf = 5ns (10% to 90%) and timed from a voltage level of 1.6V.

[2] See timing diagram below and Serial Interface section of this data sheet.

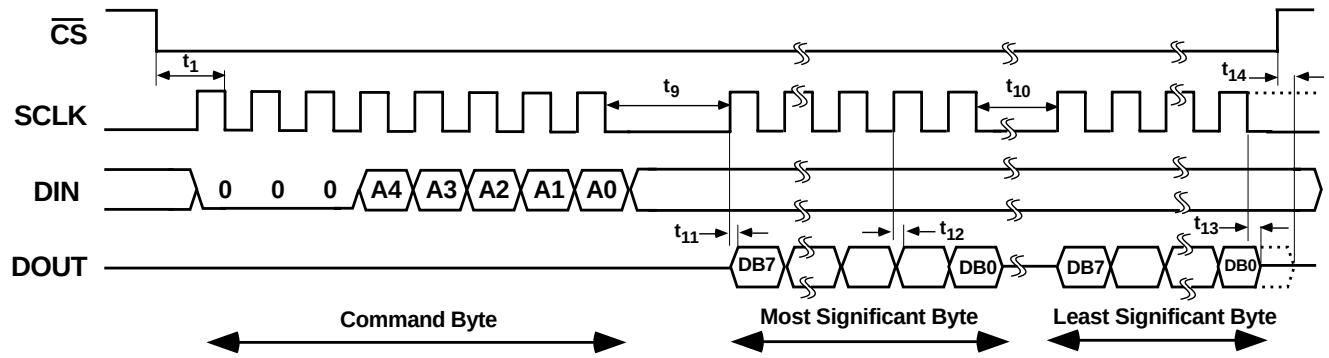
[3] Measured with the load circuit in Figure 1 and defined as the time required for the output to cross 0.8V or 2.4V.

[4] Derived from the measured time taken by the data outputs to change 0.5V when loaded with the circuit in Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50pF capacitor. This means that the time quoted in the timing characteristics is the true bus relinquish time of the part and is independant of the bus loading.

Serial Write Timing



Serial Read Timing



ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

AV_{DD} to AGND ..... –0.3 V to +7 V
DV_{DD} to DGND ..... –0.3 V to +7 V
DV_{DD} toAV_{DD} ..... –0.3 V to +0.3 V
Analog Input Voltage to AGND
V_{1P}, V_{1N}, V_{2P} and V_{2N} ..... -6V to +6V
Reference Input Voltage to AGND .. –0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to DGND ... –0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to DGND .. –0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range
Industrial (A,B Versions) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
20 Pin Plastic DIP, Power Dissipation ..... 450 mW
θ_{JA} Thermal Impedance ..... 105°C/W
Lead Temperature, (Soldering 10 sec) ..... +260°C
20 Pin SSOP, Power Dissipation ..... 450 mW
θ_{JA} Thermal Impedance ..... 112°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7756 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Terminology

MEASUREMENT ERROR

The error associated with the energy measurement made by the AD7756 is defined by the following formula:

$$\text{Percentage Error} = \left(\frac{\text{Energy registered by AD7756 - True Energy}}{\text{True Energy}} \times 100\%\right)$$

PHASE ERROR BETWEEN CHANNELS

The HPF (High Pass Filter) in Channel 1 has a phase lead response. To offset this phase response and equalize the phase response between channels a phase correction network is also placed in Channel 1. The phase correction network ensures a phase match between Channel 1 (current) and Channel 2 (voltage) to within ±0.1° over a range of 45Hz to 65Hz and ±0.2° over a range 40Hz to 1kHz.

POWER SUPPLY REJECTION

This quantifies the AD7756 measurement error as a percentage of reading when the power supplies are varied.
For the AC PSR measurement a reading at nominal supplies (5V) is taken. A second reading is obtained with the same input signal levels when an ac (175mV rms/100Hz) signal is introduced onto the supplies. Any error introduced by this ac signal is expressed as a percentage of reading—see Measurement Error definition above.
For the DC PSR measurement a reading at nominal supplies (5V) is taken. A second reading is obtained with the same input signal levels when the supplies are varied ±5%. Any error introduced is again expressed as a percentage of reading.

ADC OFFSET ERROR

This refers to the DC offset associated with the analog inputs to the ADCs. It means that with the analog inputs connected to AGND the ADCs still see a dc analog input signal. The magnitude of the offset depends on the gain and input range selection - see characteristic curves. However, when HPF1 is switched on the offset is removed from Channel 1 (current) and the power calculation is not affected by this offset. The offsets may be removed by performing an offset calibration - see Analog Inputs.

GAIN ERROR

The gain error in the AD7756 ADCs, is defined as the difference between the measured ADC output code (minus the offset) and the ideal output code - see Channel 1 ADC & Channel 2 ADC. It is measured for each of the input ranges on Channel 1 (1V, 0.5V and 0.25V). The difference is expressed as a percentage of the ideal code.

GAIN ERROR MATCH

The Gain Error Match is defined as the gain error (minus the offset) obtained when switching between a gain of 1 (for each of the input ranges) and a gain of 2, 4, 8, or 16. It is expressed as a percentage of the output ADC code obtained under a gain of 1. This gives the gain error observed when the gain selection is changed from 1 to 2, 4, 8 or 16.

Characteristic Curves

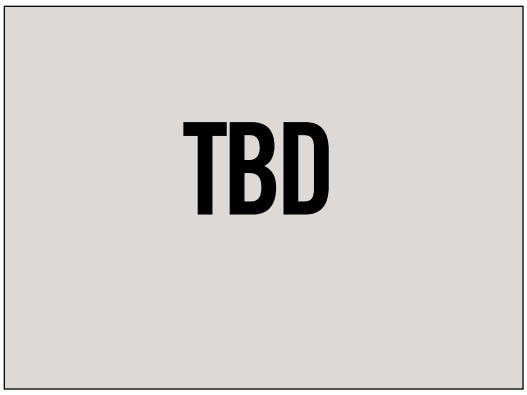


Figure 2. AD7756 Error as a % of Reading (Gain = 1)

Figure 3. AD7756 Error as a % of Reading (Gain = 2)

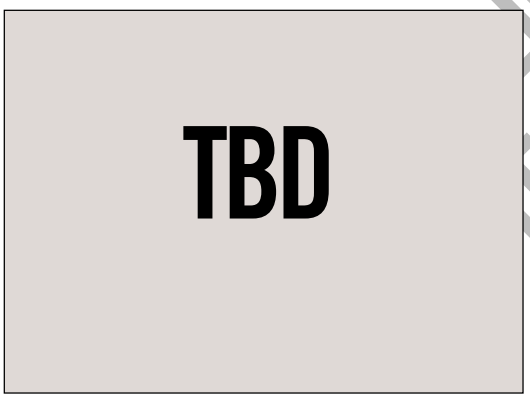


Figure 4. AD7756 Error as a % of Reading (Gain = 8)

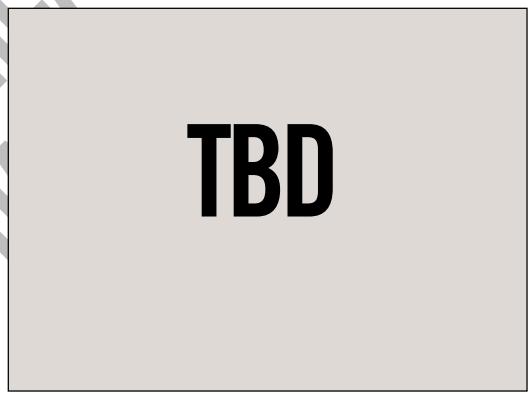


Figure 5. AD7756 Error as a % of Reading (Gain = 16)

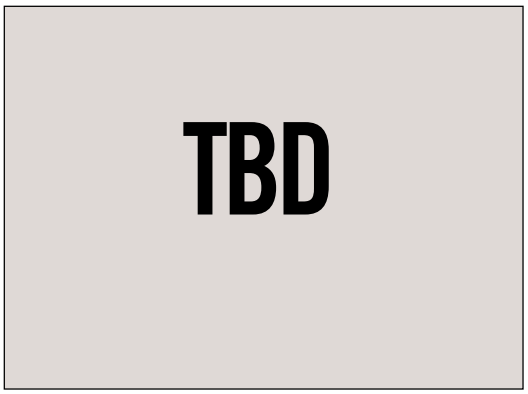


Figure 6. AC PSRR as a function of power supply ripple (Gain = 1)

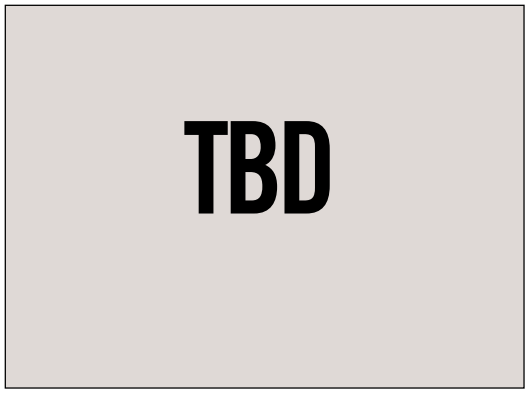


Figure 7. AC PSRR as a function of power supply ripple (Gain = 2)

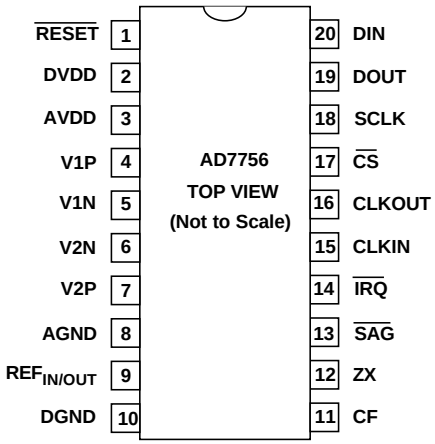
PIN FUNCTION DESCRIPTION

Pin No.	MNEMONIC	DESCRIPTION
1	$\overline{\text{RESET}}$	Reset pin for the AD7756. A logic low on this pin will hold the ADCs and digital circuitry (including the Serial Interface) in a reset condition.
2	DV_{DD}	Digital power supply. This pin provides the supply voltage for the digital circuitry in the AD7756. The supply voltage should be maintained at 5V ± 10% for specified operation. This pin should be decoupled to AGND with a 10µF capacitor in parallel with a ceramic 100nF capacitor.
3	AV_{DD}	Analog power supply. This pin provides the supply voltage for the analog circuitry in the AD7756. The supply should be maintained at 5V ± 10% for specified operation. Every effort should be made to minimize power supply ripple and noise at this pin by the use of proper decoupling. The typical performance graphs in this data sheet show the power supply rejection performance. This pin should be decoupled to AGND with a 10µF capacitor in parallel with a ceramic 100nF capacitor.
4,5	V1P, V1N	Analog inputs for Channel 1. This channel is intended for use with the current transducer. These inputs are fully differential voltage inputs with maximum differential input signal levels of ±1V, ±0.5V and ±0.25V, depending on the full scale selection - See *Analog Inputs*. Channel 1 also has PGA with gain selections of 1, 2, 4, 8 or 16. The maximum signal level at these pins with respect to AGND is ±1V . Both inputs have internal ESD protection circuitry and in addition an overvoltage of ±6V can be sustained on these inputs without risk of permanent damage.
6,7	V2N, V2P	Analog inputs for Channel 2. This channel is intended for use with the voltage transducer. These inputs are fully differential voltage inputs with a maximum differential signal level of ±1V. Channel 2 also has PGA with gain selections of 1, 2, 4, 8 or 16. The maximum signal level at these pins with respect to AGND is ±1V. Both inputs have internal ESD protection circuitry and in addition an overvoltage of ±6V can be sustained on these inputs without risk of permanent damage.
8	AGND	This pin provides the ground reference for the analog circuitry in the AD7756, i.e. ADCs and reference. This pin should be tied to the analog ground plane or the quietest ground reference in the system. This quiet ground reference should be used for all analog circuitry, e.g. anti aliasing filters, current and voltage transducers etc. In order to keep ground noise around the AD7756 to a minimum, the quiet ground plane should only connected to the digital ground plane at one point. It is acceptable to place the entire device on the analog ground plane - see Applications Information.
9	$REF_{IN/OUT}$	This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 2.4V ± 8% and a typical temperature coefficient of 30ppm/°C. An external reference source may also be connected at this pin. In either case this pin should be decoupled to AGND with a 1µF ceramic capacitor.
10	DGND	This provides the ground reference for the digital circuitry in the AD7756, i.e. multiplier, filters and digital-to-frequency converter. Because the digital return currents in the AD7756 are small, it is acceptable to connect this pin to the analog ground plane of the system - see Applications Information. However high bus capacitance on the DOUT pin may result in noisy digital current which could affect performance.
11	CF	Calibration Frequency logic output. The CF logic output gives Active Power information. This output is intended to be used for operational and calibration purposes. The full-scale output frequency can be adjusted by writing to the CFDIV Register—see *Energy To Frequency Conversion*.
12	ZX	Voltage waveform (Channel 2) zero crossing output. This output toggles logic high and low at the zero crossing of the differential signal on channel 2—see *Zero Crossing Detection*.
13	$\overline{\text{SAG}}$	This open drain logic output goes active low when either no zero crossings are detected or a low voltage threshold (Channel 2) is crossed for a specified duration. See *Line Voltage Sag Detection*.
14	$\overline{\text{IRQ}}$	Interrupt Request Output. This is an active low open drain logic output. Maskable interrupts include: Active Energy Register roll-over, Active Energy Register at half level, and waveform sampling up to 28kSPS. See *AD7756 Interrupts*.

Pin No.	MNEMONIC	DESCRIPTION
15	CLKIN	Master clock for ADCs and digital signal processing. An external clock can be provided at this logic input. Alternatively, a parallel resonant AT crystal can be connected across CLKIN and CLKOUT to provide a clock source for the AD7756. The clock frequency for specified operation is 3.579545MHz. Ceramic load capacitors of between 22pF and 33pF should be used with the gate oscillator circuit. Refer to crystal manufacturers data sheet for load capacitance requirements.
16	CLKOUT	A crystal can be connected across this pin and CLKIN as described above to provide a clock source for the AD7756. The CLKOUT pin can drive one CMOS load when either an external clock is supplied at CLKIN or a crystal is being used.
17	$\overline{CS}$	Chip Select. Part of the four wire Serial Interface. This active low logic input allows the AD7756 to share the serial bus with several other devices. See *AD7756 Serial Interface*.
18	SCLK	Serial Clock Input for the synchronous serial interface. All Serial data transfers are synchronized to this clock—see *AD7756 Serial Interface*. The SCLK has a schmitt-trigger Input for used with a clock source which has a slow edge transition time, e.g., opto-isolator outputs etc.
19	DOUT	Data Output for the Serial Interface. Data is shifted out at this pin on the rising edge of SCLK. This logic output is normally in a high impedance state unless it is driving data onto the serial data bus—see *AD7756 Serial Interface*..
20	DIN	Data Input for the Serial Interface. Data is shifted in at this pin on the falling edge of SCLK—see *AD7756 Serial Interface*..

PIN CONFIGURATION

DIP & SSOP Packages



ANALOG INPUTS

The AD7756 has two fully differential voltage input channels. The maximum differential input voltage for each input pair (V1P/V1N and V2P/V2N) is ±1V. In addition, the maximum signal level on each analog input (V1P, V1N, V2P and V2N) is also ±1V with respect to AGND.

Each analog input channel has a PGA (Programmable Gain Amplifier) with possible gain selections of 1, 2, 4, 8 and 16. The gain selections are made by writing to the Gain register—see Figure 9. Bits 0 to 2 select the gain for the PGA in Channel 1 and the gain selection for the PGA in Channel 2 is made via bits 5 to 7. Figure 8 shows how a gain selection for Channel 1 is made using the Gain register.

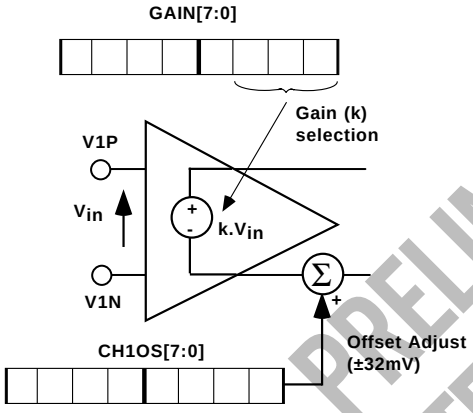


Figure 8— PGA in Channel 1

In addition to the PGA, Channel 1 also has a full scale input range selection for the ADC. The ADC analog input range selection is also made using the Gain register—see Figure 9. As mentioned previously the maximum differential input voltage is 1V. However by using bits 3 and 4 in the Gain register the maximum ADC input voltage can be set to 1V, 0.5V or 0.25V. This is achieved by adjusting the ADC reference—see AD7756 Reference Circuit. Table I below summarizes the maximum differential input signal level on Channel 1 for the various ADC range and gain selections.

Table I

Maximum input signal levels for Channel 1

Max Signal Channel 1	ADC Input Range Selection 1V	0.5V	0.25V
1V	Gain = 1	—	—
0.5V	Gain = 2	Gain = 1	—
0.25V	Gain = 4	Gain = 2	Gain = 1
0.125V	Gain = 8	Gain = 4	Gain = 2
0.0625V	Gain = 16	Gain = 8	Gain = 4
0.0313V	—	Gain = 16	Gain = 8
0.0156V	—	—	Gain = 16

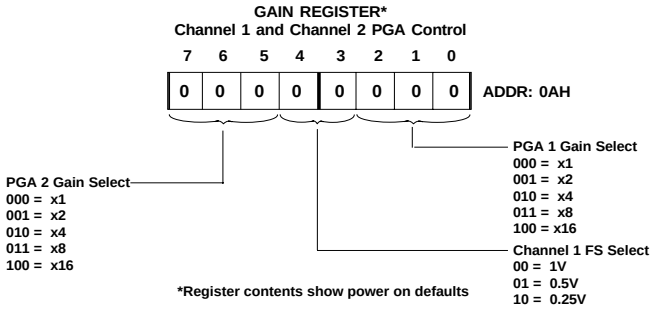


Figure 9— AD7756 Analog Gain register

It is also possible to adjust offset errors on Channel 1 and Channel 2 by writing to the Offset Correction Registers (CH1OS and CH2OS respectively). These registers allow channel offsets in the range ±20mV to ±60mV (depending on the gain setting) to be removed. Note that it is not necessary to perform an offset correction in an Energy measurement application if HPF1 in Channel 1 is switched on. Figure 10 shows the effect of offsets on the real power calculation. As can be seen from Figure 10 an offset on Channel 1 and Channel 2 will contribute a dc component after multiplication. Since this dc component is extracted by LPF2 to generate the Active (Real) Power information, the offsets will have contributed an error to the Active Power calculation. This problem is easily avoided by enabling HPF1 in Channel 1. By removing the offset from at least one channel, no error component can be generated at dc by the multiplication. Error terms at Cos(ω.t) are removed by LPF2 and by integration of the Active Power signal in the Active Energy register (AENERGY[39:0]) – see *Energy Calculation*.

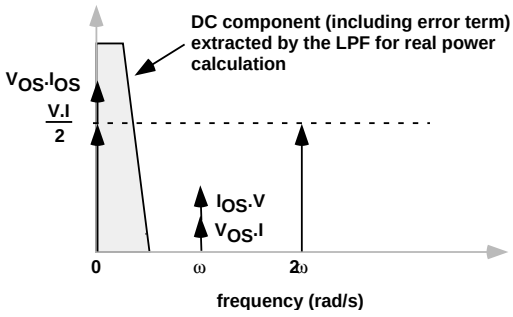


Figure 10— Effect of channel offsets on the real power calculation

The contents of the Offset Correction registers are 6-Bit, sign and magnitude coded. The weighting of the LSB size depends on the gain setting, i.e., 1, 2, 4, 8 or 16. Table II below shows the correctable offset span for each of the gain settings and the LSB weight (mV) for the Offset Correction registers. The maximum value which can be written to the offset correction registers is ±31 decimal — see Figure 11.

Table II

Offset Correction range

Gain	Correctable Span	LSB Size
1	±60mV	1.88mV/LSB
2	±40mV	1.25mV/LSB
4	±25mV	0.78mV/LSB
8	±23mV	0.72mV/LSB
16	±20mV	0.63mV/LSB

Figure 11 shows the relationship between the Offset Correction register contents and the offset (mV) on the analog inputs for a gain setting of one. In order to perform an offset adjustment, The analog inputs should be first connected to AGND. There should be no signal on either Channel 1 or Channel 2. A read from Channel 1 or Channel 2 will give an indication of the offset in the channel. This offset can be canceled by writing an equal and opposite offset value to the relevant offset register. The offset correction can be confirmed by performing another read. Note when adjusting the offset of Channel 1 ensure the HPF has been disabled in the Mode register.

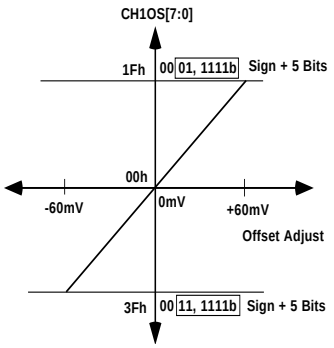


Figure 11– Channel Offset Correction Range (Gain = 1)

ZERO CROSSING DETECTION

The AD7756 has a zero crossing detection circuit on Channel 2. This zero crossing is used to produce an external zero cross signal (ZX) and it is also used in the calibration mode - see *Energy Calibration*. The zero crossing signal is also used to initiate a temperature measurement on the AD7756 - see *Temperature Measurement*.

Figure 12 shows how the zero cross signal is generated from the output of LPF1.

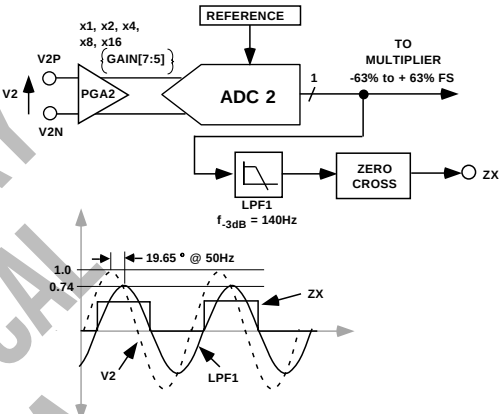


Figure 12– Zero cross detection on Channel 2

The ZX signal will go logic high on a positive going zero crossing and logic low on a negative going zero crossing on Channel 2. The zero crossing signal ZX is generated from the output of LPF1. LPF1 has a single pole at 140Hz (CLKIN = 3.579545MHz). As a result there will be a phase lag between the analog input signal V2 and the output of LPF1. The phase response of this filter is shown in the Channel 2 Sampling section of this data sheet. The phase lag response of LPF1 results in a time delay of approximately 1.1ms (@ 50Hz) between the zero crossing on the analog inputs of Channel 2 and the rising or falling edge of ZX.

The zero crossing detection also has an associated time-out register ZXTOUT. This unsigned, 16 bit register is decremented (1 LSB) every 64/CLKIN seconds. The register is reset to its user programmed full scale value every time a zero crossing on Channel 2 is detected. The default power on value in this register is FFFFh. If the register decrements to zero before a zero crossing is detected and the DISSAG bit in the Mode register is logic zero, the $\overline{\text{SAG}}$ pin will go active low. The absence of a zero crossing is also indicated on the $\overline{\text{IRQ}}$ output if the SAG enable bit in the Interrupt Enable register is set to logic one. Irrespective of the enable bit setting, the SAG flag in the Interrupt Status register is always set when the ZXTOUT register is decremented to zero - see *AD7756 Interrupts*.

The Zerocross Time-out register can be written/read by the user and has an address of 0Eh - see *Serial Interface* section. The resolution of the register is 64/CLKIN seconds per LSB. Thus the maximum delay for an interrupt is 1.2 seconds (64/CLKIN x 2^{16}).

LINE VOLTAGE SAG DETECTION

In addition to the detection of the loss of the line voltage signal (zero crossing), the AD7756 can also be programmed to detect when the absolute value of the line voltage drops below a certain peak value, for a number of half cycles. This condition is illustrated in Figure 13 below.

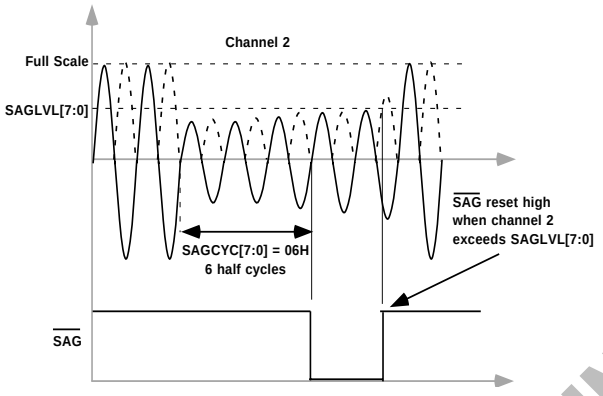


Figure 13– AD7756 Sag detection

Figure 13 shows the line voltage fall below a threshold which is set in the Sag Level register (SAGLVL[7:0]) for nine half cycles. Since the Sag Cycle register (SAGCYC[7:0]) contains 06h the $\overline{SAG}$ pin will go active low at the end of the sixth half cycle, if the DISSAG bit in the Mode register is logic zero. As is the case when zero-crossings are no longer detected, the sag event is also recorded by setting the SAG flag in the Interrupt Status register. If the SAG enable bit is set to logic one, the $\overline{IRQ}$ logic output will go active low - see *AD7756 Interrupts*. The $\overline{SAG}$ pin will go logic high again when the absolute value of the signal on Channel 2 exceeds the sag level set in the Sag Level register . This is shown in Figure 13 when the $\overline{SAG}$ pin goes high during the tenth half cycle from the time when the signal on Channel 2 first dropped below the threshold level.

Sag Level Set

The contents of the Sag Level register (1 byte) are compared to the absolute value of the most significant byte output from LFP1, after it is shifted left by one bit. Thus for example the nominal maximum code from LFP1 with a full scale signal on Channel 2 is 1C396h or (0001, 1100, 0011, 1001, 0110b)—see Channel 2 sampling. Shifting one bit left will give 0011,1000,0111,0010,1100b or 3872Ch. Therefore writing 38h to the Sag Level register will put the sag detection level at full scale. Writing 00h will put the sag detection level at zero. The Sag Level register is compared to the most significant byte of a waveform sample after the shift left.

POWER SUPPLY MONITOR

The AD7756 also contains an on-chip power supply monitor. The Analog Supply (AV_{DD}) is continuously monitored by the AD7756. If the supply is less than 4V ± 5% then the AD7755 will be reset. This is useful to ensure correct device operation at power up and during power down. The power supply monitor has built-in hysteresis and filtering. This gives a high degree of immunity to false triggering due to noisy supplies.

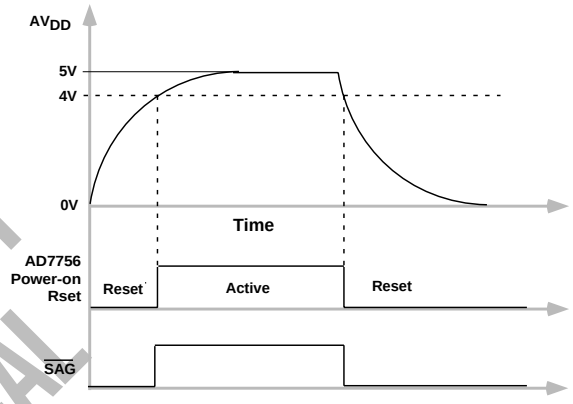


Figure 14 - On-Chip power supply monitor

As can be seen from Figure 14 the trigger level is nominally set at 4V. The tolerance on this trigger level is about ±5%. The $\overline{SAG}$ pin can also be used as a power supply monitor input to the MCU. The $\overline{SAG}$ pin will go logic low when the AD7756 is reset. The power supply and decoupling for the part should be such that the ripple at AV_{DD} does not exceed 5V±10% as specified for normal operation.

AD7756 INTERRUPTS

AD7756 Interrupts are managed through the Interrupt Status register (STATUS[7:0]) and the Interrupt Enable register (INTEN[7:0]). When an interrupt event occurs in the AD7756, the corresponding flag in the Status register is set to a logic one - see Interrupt Status register. If the enable bit for this interrupt in the Interrupt Enable register is logic one, then the $\overline{IRQ}$ logic output goes active low. The flag bits in the Status register are set irrespective of the state of the enable bits.

In order to determine the source of the interrupt, the system master (MCU) should perform a read from the Status register with reset. This is achieved by carrying out a read from address 05h. The $\overline{IRQ}$ output will go logic high on completion of the Interrupt Status register read command—see *Interrupt timing*. When carrying out a read with reset the AD7756 is designed to ensure that no interrupt events are missed. If an interrupt event occurs just as the Status register is being read, the event will not be lost and the $\overline{IRQ}$ logic output is guaranteed to go high for the duration of the Interrupt Status register data transfer before going logic low again to indicate the pending interrupt. See the next section for a more detailed description.

Using the AD7756 Interrupts with an MCU

Shown in Figure 15 is a timing diagram which shows a suggested implementation of AD7756 interrupt management using an MCU. At time t_1 the $\overline{IRQ}$ line will go active low indicating that one or more interrupt events have occurred in the AD7756. The $\overline{IRQ}$ logic output should be tied to a negative edge triggered external interrupt on the MCU. On detection of the negative edge, the MCU should be configured to start executing its Interrupt Service Routine (ISR). On entering the ISR, all interrupts should be disabled using the global interrupt enable bit. At this point the MCU external interrupt flag can be cleared in order to capture interrupt events which occur during the current ISR. When the MCU interrupt flag is cleared a read from the Status register with reset is carried out. This will cause the $\overline{IRQ}$ line to be reset logic high (t_2)—see *Interrupt timing*. The Status register contents are used to determine the source of the interrupt(s) and hence the appropriate action to be taken. If a subsequent interrupt event occurs during the ISR (t_3), that event will be recorded by the MCU external interrupt flag being set again. On returning from the ISR, the global interrupt mask will be cleared (same instruction cycle) and the external interrupt flag will cause the MCU to jump to its ISR once again. This will ensure that the MCU does not miss any external interrupts.

Interrupt timing

The *AD7756 Serial Interface* section should be reviewed first before reviewing the interrupt timing. As previously described, when the $\overline{IRQ}$ output goes low the MCU ISR must read the Interrupt Status register in order to determine the source of the interrupt. When reading the Status register contents, the $\overline{IRQ}$ output is set high on the last falling edge of SCLK of the first byte transfer (read Interrupt Status register command). The $\overline{IRQ}$ output is held high until the last bit of the next 8-bit transfer is shifted out (Interrupt Status register contents). See Figure 16. If an interrupt is pending at this time, the $\overline{IRQ}$ output will go low again. If no interrupt is pending the $\overline{IRQ}$ output will stay high.

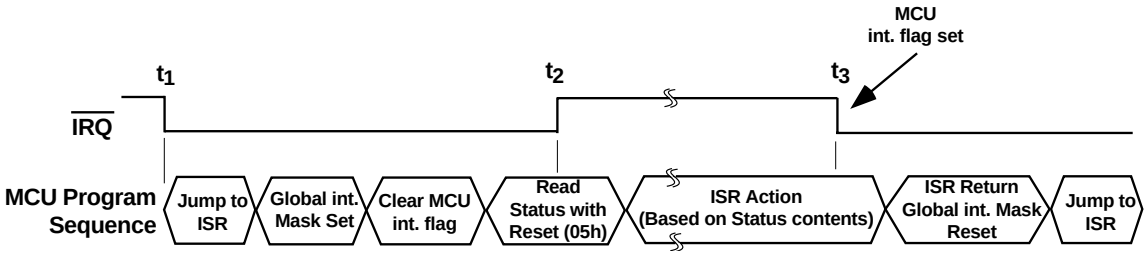


Figure 15– AD7756 interrupt management

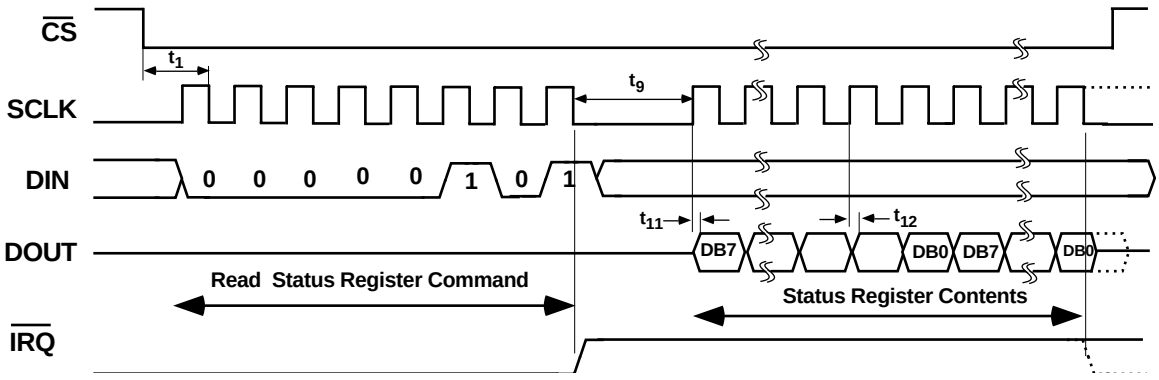


Figure 16– AD7756 interrupt timing

TEMPERATURE MEASUREMENT

The AD7756 also includes an on-chip temperature sensor. A temperature measurement can be made by setting bit 5 in the Mode register. When bit 5 is set logic high in the Mode register, the AD7756 will initiate a temperature measurement on the next zero crossing. When the zero crossing on Channel 2 is detected the voltage output from the temperature sensing circuit is connected to ADC1 (Channel 1) for digitizing. The resultant code is processed and placed in the Temperature register (TEMP[7:0]) approximately 26µs later (24 CLKIN cycles). If enabled in the Interrupt Enable register (bit 5), the $\overline{IRQ}$ output will go active low when the temperature conversion is finished.

The contents of the Temperature register are signed (2's complement) with a resolution of 1 LSB/°C. The temperature register will produce a code of 00h when the abient temperature is approximately 70°C—see Figure 17. The temperature measurement is uncalibrated in the AD7756 and has an offset tolerance of approximately ±5°C.

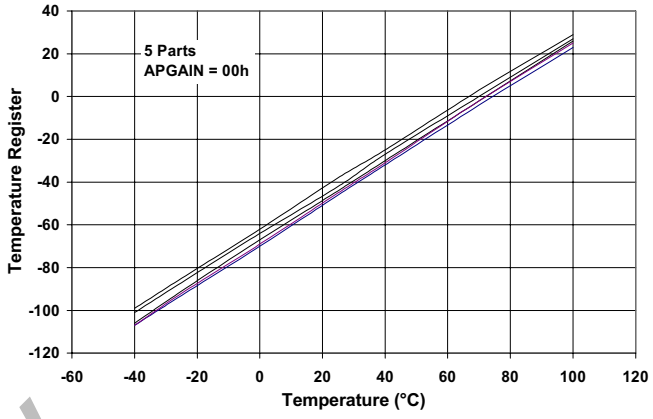


Figure 17– Temperature Register

AD7756 ANALOG TO DIGITAL CONVERSION

The analog-to-digital conversion in the AD7756 is carried out using two second order sigma-delta ADCs. The block diagram in Figure 18 shows a first order (for simplicity) sigma-delta ADC. The converter is made up of two parts, first the sigma-delta modulator and secondly the digital low pass filter.

A sigma-delta modulator converts the input signal into a continuous serial stream of 1's and 0's at a rate determined by the sampling clock. In the AD7756 the sampling clock is equal to CLKIN/4. The 1-bit DAC in the feedback loop is driven by the serial data stream. The DAC output is subtracted from the input signal. If the loop gain is high enough the average value of the DAC output (and therefore the bit stream) will approach that of the input signal level. For any given input value in a single sampling interval, the data from the 1-bit ADC is virtually meaningless. Only when a large number of samples are averaged, will a meaningful result be obtained. This averaging is carried out in the second part of the ADC, the digital low pass filter. By averaging a large number of bits from the modulator the low pass filter can produce 20 bit data words which are proportional to the input signal level.

The sigma-delta converter uses two techniques to achieve high resolution from what is essentially a 1-bit conversion technique. The first is over-sampling. By over sampling we mean that the signal is sampled at a rate (frequency) which is many times higher than the bandwidth of interest. For example the sampling rate in the AD7756 is CLKIN/4 (894kHz) and the band of interest is 40Hz to 2kHz. Oversampling has the effect of spreading the quantization noise (noise due to sampling) over a wider bandwidth. With the noise spread more thinly over a wider bandwidth, the quantization noise in the band of interest is lowered—see Figure 19. However oversampling alone is not an efficient enough method to improve the signal to noise ratio (SNR) in the band of interest. For example, an oversampling ratio of 4 is required just to increase the SNR by only 6dB (1-Bit). To keep the oversampling ratio at a reasonable level, it is possible to shape the quantization noise so that the majority of the noise lies at the higher frequencies. This is what happens in the sigma-delta modulator, the noise is shaped by the integrator which has a high pass type response for the quantization noise. The result is that most of the noise is at the higher frequencies where it can be removed by the digital low pass filter. This noise shaping is also shown in Figure 19.

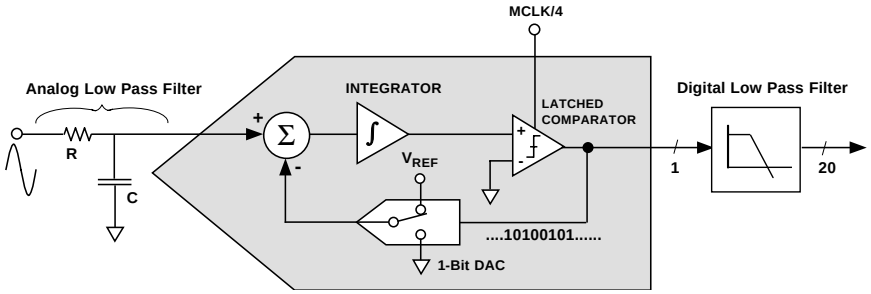


Figure 18– First Order Sigma-Delta (Σ–Δ) ADC

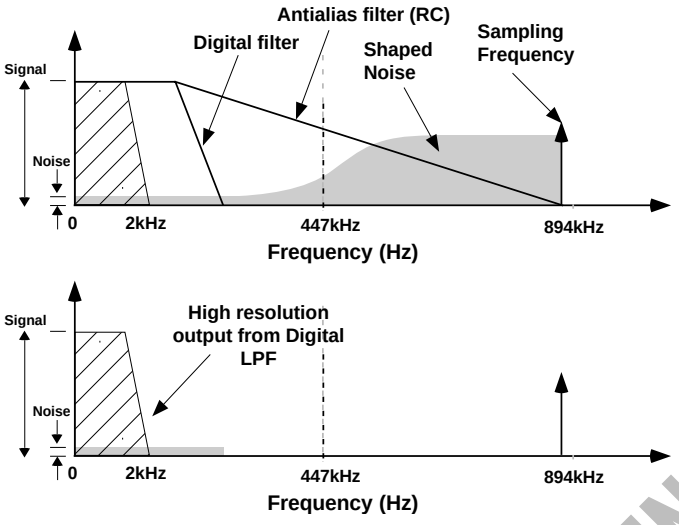


Figure 19– Noise reduction due to Oversampling & Noise shaping in the analog modulator

Antialias Filter

Figure 18 also shows an analog low pass filter (RC) on the input to the modulator. This filter is present to prevent aliasing. Aliasing is an artifact of all sampled systems. Basically it means that frequency components in the input signal to the ADC which are higher than half the sampling rate of the ADC will appear in the sampled signal at a frequency below half the sampling rate. Figure 20 illustrates the effect, frequency components (arrows shown in black) above half the sampling frequency (also know as the Nyquist frequency, i.e., 447kHz) get imaged or folded back down below 447kHz (arrows shown in grey). This will happen with all ADCs no matter what the architecture. In the example shown it can be seen that only frequencies near the sampling frequency, i.e., 894kHz, will move into the band of interest for metering, i.e, 40Hz - 2kHz. This fact will allow us to use a very simple LPF (Low Pass Filter) to attenuate these high frequencies (near 900kHz) and so prevent distortion in the band of interest. A simple RC filter (single pole) with a corner frequency of 10kHz will produce an attenuation of approximately 40dBs at 894kHz—see Figure 19. This is sufficient to eliminate the effects of aliasing.

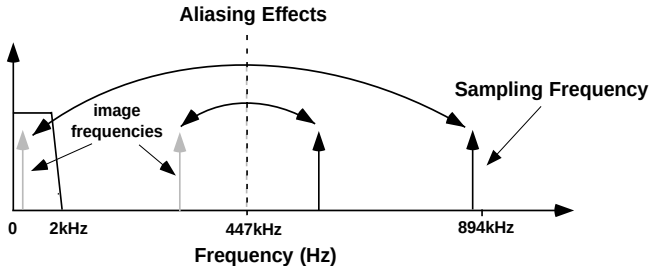


Figure 20 —ADC and signal processing in Channel 1

ADC transfer function

Below is an expression which relates the output of the LPF in the sigma-delta ADC to the analog input signal level. Both ADCs in the AD7756 are designed to produce the same output code for the same input signal level.

$$\text{Code (ADC)} = 1.512 \times \frac{V_{in}}{V_{REF}} \times 262{,}144$$

Therefore with a full scale signal on the input of 1V and an internal reference of 2.4V, the ADC output code is nominally 165,151 or 2851Fh. The maximum code from the ADC is ±262,144, this is equivalent to an input signal level of ±1.6V. However for specified performance it is not recommended that the maximum input signal level be exceeded.

AD7756 Reference circuit

Shown below in Figure 21 is a simplified version of the reference output circuitry. The nominal reference voltage at the $REF_{IN/OUT}$ pin is 2.42V. This is the reference voltage used for the ADCs in the AD7756. However Channel 1 has three input range selections which are selected by dividing down the reference value used for the ADC in Channel 1. The reference value used for Channel 1 is divided down to ½ and ¼ of the nominal value by using a resistor divider as shown in Figure 21.

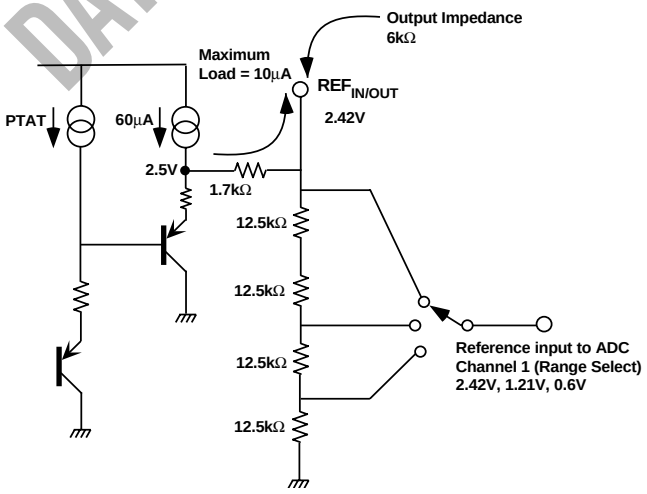


Figure 21 —AD7756 Reference Circuit Ouput

The $REF_{IN/OUT}$ pin can be overdriven by an external source, e.g., an external 2.5V reference. Note that the nominal reference value supplied to the ADCs is now 2.5V not 2.42V. This has the effect of increasing the nominal analog input signal range by 2.5/2.42 x 100% = 3% or from 1V to 1.03V.

CHANNEL 1 ADC

Figure 22 shows the ADC and signal processing chain for Channel 1. In waveform sampling mode the ADC outputs a signed 2's Complement 20 Bit data word at a maximum of 27.9kSPS (3.579545MHz/128). The output of the ADC can be scaled by ±50% to perform an overall power calibration or to calibrate the ADC output. While the ADC outputs a 20 bit 2's complement value the maximum full-scale positive value from the ADC is limited to 40000h (+262,144 Decimal). The maximum full-scale negative value is limited to C0000h (-262,144 Decimal). If the analog inputs are over-ranged, the ADC output code will clamp at these values. With the specified full scale analog input signal of 1V (or 0.5V or 0.25V – see *Analog Inputs* section) the ADC will produce an output code which is approximately 63% of its full-scale value. This is illustrated in Figure 22. The diagram in Figure 22 shows a full-scale voltage signal being applied to the differential inputs V1P and V1N. The ADC output swings between D7AE1h (-165,151) and 2851Fh (+165,151). This is approximately 63% of the full-scale value 40000h (262,144). Over-ranging the analog inputs with more than 1V differential (0.5 or 0.25, depending on Channel 1 full scale selection) will cause the ADC outputs to increase towards its full scale value. However for specified operation the differential signal on the analog inputs should not exceed the recommended value.

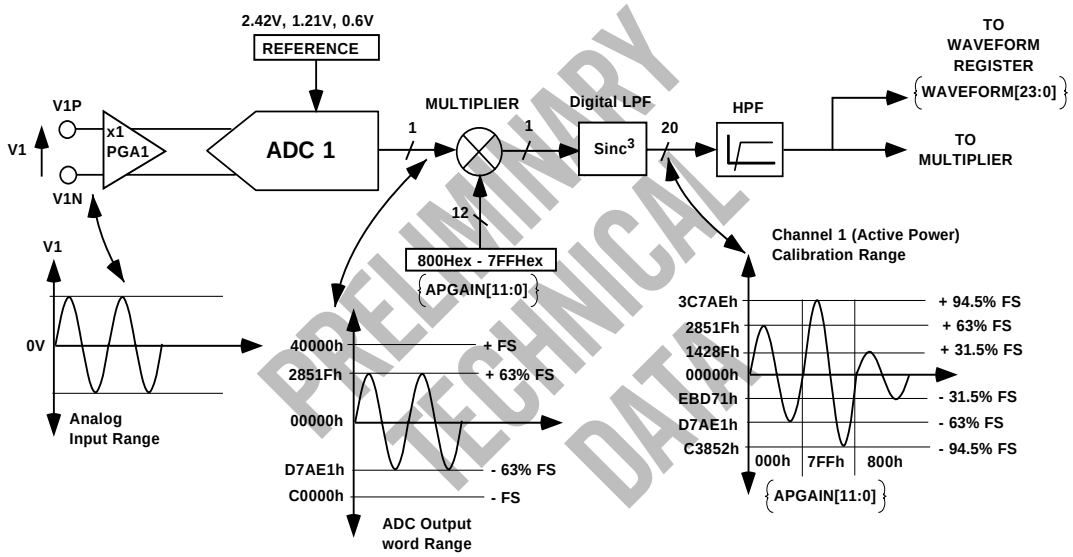


Figure 22 —ADC and signal processing in Channel 1

Channel 1 ADC Gain Adjust

The ADC gain in Channel 1 can be adjusted by using the multiplier and Active Power Gain register (APGAIN[11:0]). The gain of the ADC is adjusted by writing a 2's complement 12 bit word to the Active Power Gain register. Below is the expression that shows how the gain adjustment is related to the contents of the Active Power Gain register.

$$\text{Code} = \left(\text{ADC} \times \left\{1 + \frac{\text{APGAIN}}{2^{12}}\right\}\right)$$

For example when 7FFh is written to the Active Power Gain register the ADC output is scaled up by 50%. 7FFh = 2047 Dec,
$2047/2^{12}$ = 0.5. Similarly, 800h = -2047 Dec (signed 2's Complement) and ADC output is scaled by –50%. These two examples are illustrated graphically in Figure 22.

Channel 1 Sampling

The waveform samples may also be routed to the WAVEFORM register (MODE[14:13] = 1,0) to be read by the system master (MCU). In waveform sampling mode the WSMP bit in the Interrupt Enable register must also be set to logic one. The Active Power and Energy calculation will remain uninterrupted during waveform sampling. When in waveform sample mode, one of four output sample rates may be chosen by using bits 11 and 12 of the Mode register. The output sample rate may be 27.9kSPS, 14kSPS, 7kSPS or 3.5kSPS—see Mode register. The interrupt request output $\overline{\text{IRQ}}$ signals a new sample availability by going active low. The timing is shown in Figure 32. The 20 bit waveform samples are transferred from the AD7756 one byte (8-bits) at a time, with the most significant byte shifted out first. The 20 bit data word is right justified and sign extended to 24 bits (three bytes) - see *AD7756 Serial Interface*.

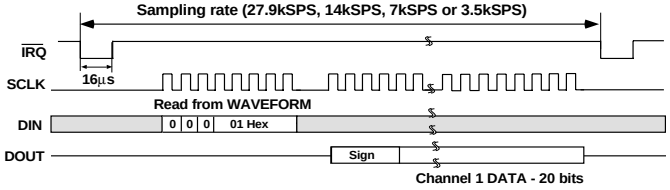


Figure 23 – Waveform sampling Channel 1

CHANNEL 2 ADC

Channel 2 Sampling

In Channel 2 waveform sampling mode (MODE[14:13] = 1,1 and WSEL = 1) the ADC output code scaling for Channel 2 is the same as Channel 1, i.e., the output swings between D7AE1h (-165,151) and 2851Fh (+165,151) – see *ADC Channel 1*. However before being passed to the Waveform register, the ADC output is passed through a single pole, low pass filter with a cutoff frequency of 140Hz. The plots in Figure 24 shows the magnitude and phase response of this filter.

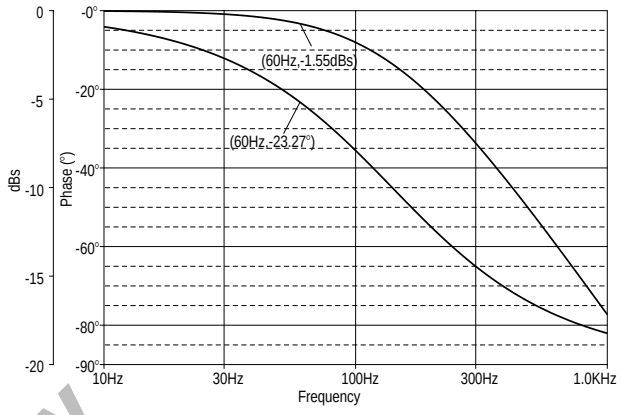


Figure 24 – Magnitude & Phase response of LPF1

This has the effect of attenuating the signal. For example if the line frequency is 60Hz, then the signal at the output of LPF1 will be attenuated by 30%.

$$\left|H(f)\right| = \frac{1}{1 + 60\text{Hz}/140\text{Hz}} = 0.7 = -1.55\text{dBs}$$

Note LPF1 does not effect the power calculation. The signal processing chain in Channel 2 is illustrated in Figure 25. Unlike Channel 1, Channel 2 has only one analog input range (1V differential). However like Channel 1, Channel 2 does have a PGA with gain selections of 1, 2, 4, 8 and 16. For energy measurement, the output of the ADC is passed directly to the multiplier and is not filtered. A HPF is not required to remove any DC offset since it is only required to remove the offset from one channel to eliminate errors due to offsets in the power calculation. When in waveform sample mode, one of four output sample rates can be chosen by using bits 11 and 12 of the Mode register. The available output sample rates are 27.9kSPS, 14kSPS, 7kSPS or 3.5kSPS. The interrupt request output $\overline{\text{IRQ}}$ signals a new sample availability by going active low. The timing is the same as that for Channel 1 and is shown in Figure 23.

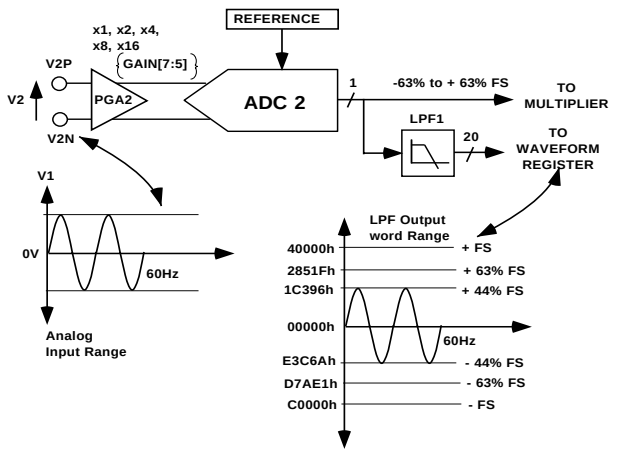


Figure 25 – ADC and Signal Processing in Channel 2

PHASE COMPENSATION

When the HPF is disabled the phase error between Channel 1 and Channel 2 is zero from DC to 3.5kHz. When HPF1 is enabled, Channel 1 has a phase response illustrated in Figure 27a & 27b. Also shown in Figure 27c is the magnitude response of the filter. As can be seen from the plots, the phase response is almost zero from 45Hz to 1kHz, This is all that is required in typical energy measurement applications.

However despite being internally phase compensated the AD7756 must work with transducers which may have inherent phase errors. For example a phase error of 0.1° to 0.3° is not uncommon for a CT (Current Transformer). These phase errors can vary from part to part and they must be corrected in order to perform accurate power calculations. The errors associated with phase mismatch are particularly noticeable at low power factors. The AD7756 provides a means of digitally calibrating these small phase errors. The AD7756 allows a small time delay or time advance to be introduced into the signal processing chain in order to compensate for small phase errors. Because the compensation is in time, this technique should only be used for small phase errors in the range of 0.1° to 0.5°. Correcting large phase errors using a time shift technique can introduce significant phase errors at higher harmonics.

The Phase Calibration register (PHCAL[7:0]) is a 2's complement 6-bit signed register which can vary the time delay in the Channel 2 signal path from –143µs to +143µs (CLKIN = 3.579545MHz). One LSB is equivalent to 4.47µs. With a line frequency of 50Hz this gives a phase resolution of 0.08° at the fundamental (i.e., 360° x 4.47µs x 50Hz). Figure 26 illustrates how the phase compensation is used to remove a 0.091° phase lead in channel 1 due to some external transducer. In order to cancel the lead (0.091°) in Channel 1, a phase lead must also be introduced into Channel 2. The resolution of the phase adjustment allows the introduction of a phase lead of 0.08°. The phase lead is achieved by introducing a time advance into Channel 2. A time advance of 4.47µs is made by writing -1 (3Fh) to the time delay block, thus reducing the amount of time delay by 4.47µs.

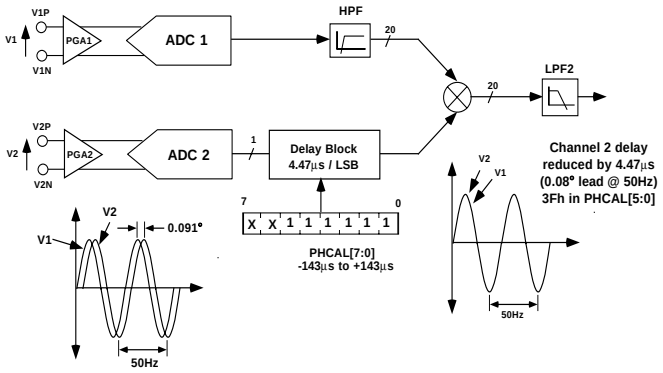
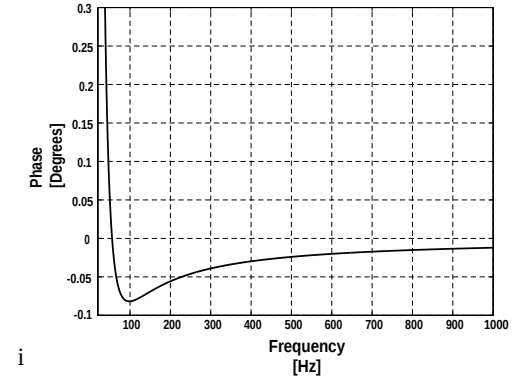


Figure 26 – Phase Calibration



i

Figure 27a – Phase response of the HPF & Phase Compensation (10Hz to 1kHz)

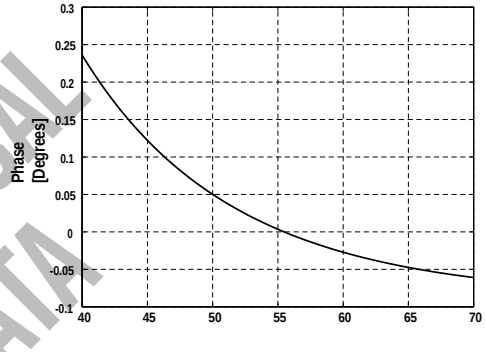


Figure 27b – Phase response of the HPF & Phase Compensation (40Hz to 70Hz)

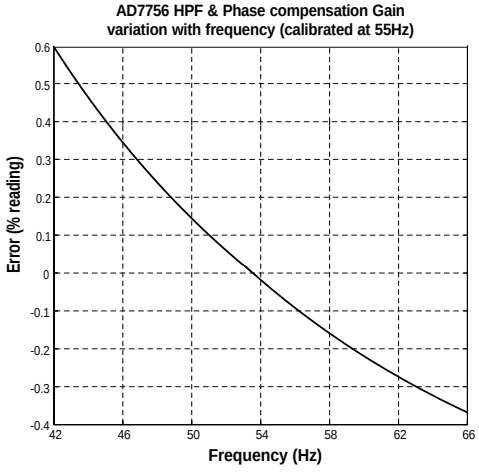


Figure 27c – Gain response of HPF & Phase Compensation (deviation of Gain as % of Gain at 54Hz)

ACTIVE POWER CALCULATION

Electrical power is defined as the rate of energy flow from source to load. It is given by the product of the voltage and current waveforms. The resulting waveform is called the instantaneous power signal and it is equal to the rate of energy flow at every instant of time. The unit of power is the watt or joules/sec. Equation 3 gives an expression for the instantaneous power signal in an ac system.

$$v(t) = \sqrt{2}V\sin(\omega t) \quad (1)$$

$$i(t) = \sqrt{2}I\sin(\omega t) \quad (2)$$

where V = rms voltage,
I = rms current.

$$p(t) = v(t) \times i(t)$$

$$p(t) = VI - VI\cos(2\omega t) \quad (3)$$

The average power over an integral number of line cycles (n) is given by the expression in Equation 4.

$$P = \frac{1}{nT}\int_0^{nT} p(t)dt = VI \quad (4)$$

where T is the line cycle period.
P is referred to as the Active or Real Power. Note that the active power is equal to the dc component of the instantaneous power signal $p(t)$ in Equation 3 , i.e., VI. This is the relationship used to calculate active power in the AD7756. The instantaneous power signal $p(t)$ is generated by multiplying the current and voltage signals. The dc component of the instantaneous power signal is then extracted by LPF2 (Low Pass Filter) to obtain the active power information. This process is illustrated graphically in Figure 28. Since LPF2 does not have an ideal "brick wall" frequency response—see Figure 29, the Active Power signal will have some ripple due to the instantaneous power signal. This ripple is sinusoidal and has a frequency equal to twice the line frequency. Since the ripple is sinusoidal in nature it will be removed when the Active Power signal is integrated to calculate Energy – see *Energy Calculation*.

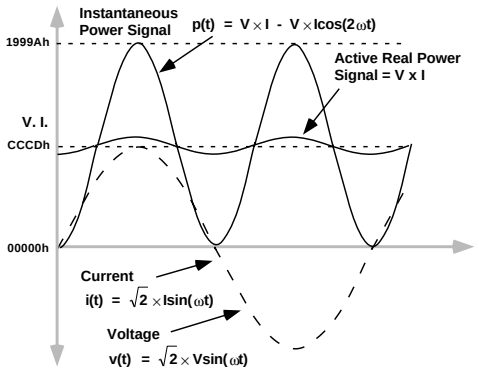


Figure 28– Active Power Calculation

Figure 30 shows the signal processing chain for the Active Power calculation in the AD7756. As explained, the Active Power is calculated by low pass filtering the instantaneous power signal.

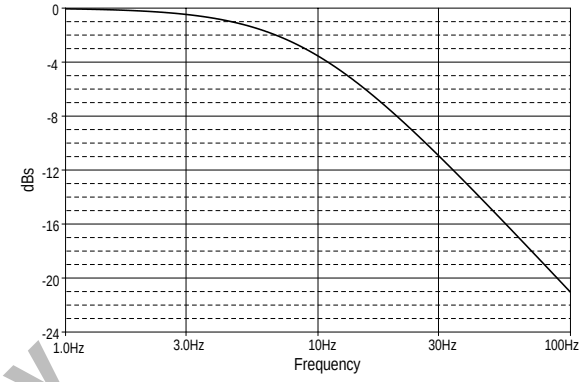


Figure 29 —Frequency Response of LPF2

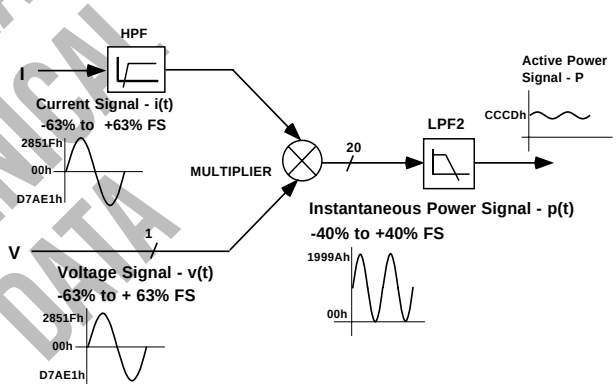


Figure 30– Active Power Signal Processing

Shown in Figure 31 is the maximum code (Hexadecimal) output range for the Active Power signal (LPF2). Note that the output range changes depending on the contents of the Active Power Gain register – see *Channel 1 ADC*. The minimum output range is given when the Active Power Gain register contents are equal to 800h and the maximum range is given by writing 7FFh to the Active Power Gain register. This can be used to calibrate the Active Power (or Energy) calculation in the AD7756.

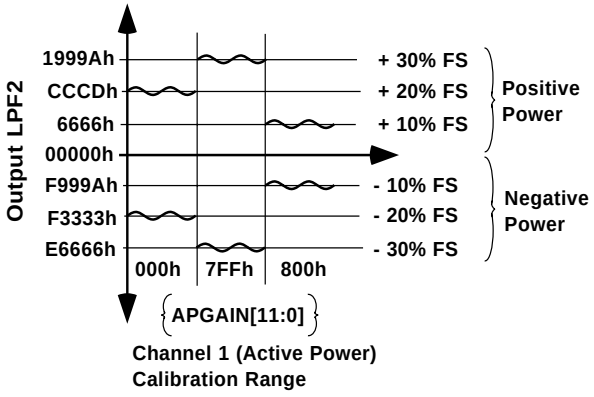


Figure 31 – Active Power Calculation Output Range

ENERGY CALCULATION

As stated earlier, power is defined as the rate of energy flow. This relationship can be expressed mathematically as Equation 5.

$$P = \frac{dE}{dt} \quad (5)$$

Where P = Power and E = Energy.
Conversely Energy is given as the integral of Power.

$$E = \int P dt \quad (6)$$

The AD7756 achieves the integration of the Active Power signal by continuously accumulating the Active Power signal in the 40-bit Active Energy register (AENERGY[39:0]). This discrete time accumulation or summation is equivalent to integration in continuous time. Equation 7 below expresses the relationship

$$E = \int p(t)dt = \lim_{T \to 0} \left\{ \sum_{n=0}^{\infty} p(nT) \times T \right\} \quad (7)$$

Where n is the discrete time sample number and T is the sample period.
The discrete time sample period (T) for the accumulation register in the AD7756 is 1.1µs (4/3.579545MHz). As well as calculating the Energy this integration removes any sinusoidal components which may be in the Active Power signal.
Figure 32 shows a graphical representation of this discrete time integration or accumulation. The Active Power signal in the Waveform register is continuously added to the Active Energy register. This addition is a signed addition, therefore negative energy will be subtracted from the Active Energy contents.

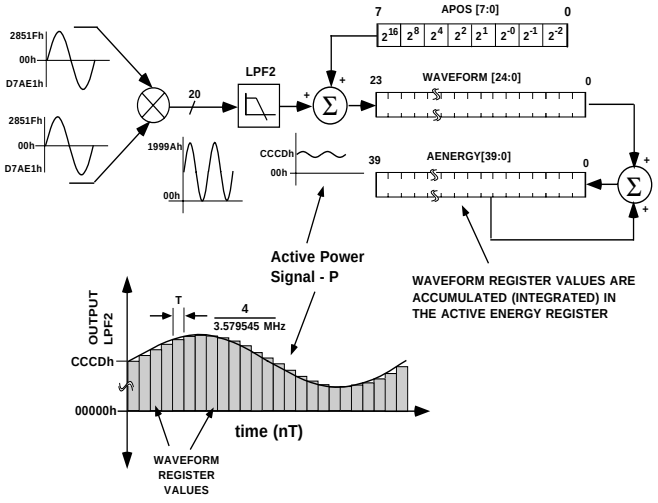


Figure 32 – AD7756 Energy Calculation

As shown in Figure 32, the Active Power signal is accumulated in a 40-bit signed register (AENERGY[39:0]). The Active Power signal can be read from the Waveform register by setting MODE[14:13] = 0,0 and setting the WSEL bit in the interrupt enable register to 1. Like the Channel 1 and Channel 2 waveform sampling modes the waveform date is available at sample rates of 27.9kSPS, 14kSPS, 7kSPS or 3.5kSPS—see Figure 23.
Figure 33 shows this energy accumulation for full scale signals (sinusoidal) on the analog inputs. The three curves displayed, illustrate the minimum time it takes the energy register to roll-over when the Active Power Gain register contents are 3FFh, 000h and 800h. The Active Power Gain register is used to carry out a power calibration in the AD7756. As shown, the fastest integration time will occur when the Active Power Gain register is set to maximum full scale, i.e., 3FFh.

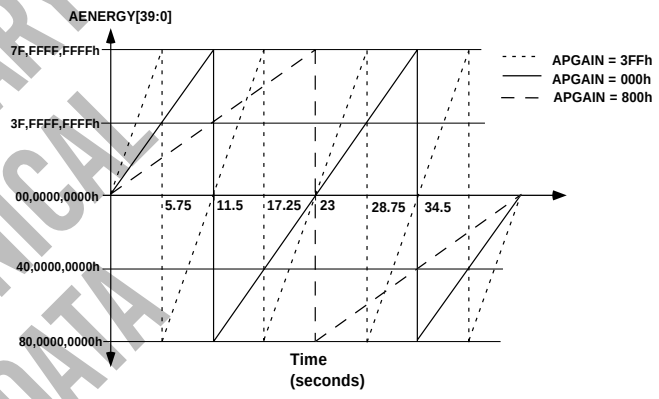


Figure 33 - Energy register roll-over time for full-scale power (Minimum & Maximum Power Gain)

Note that the energy register contents will roll over to full-scale negative (80,0000,0000h) and continue increasing in value when the power or energy flow is positive - see Figure 33. Conversely if the power is negative the energy register would under flow to full scale positive (7F,FFFF, FFFFh) and continue decreasing in value.
By using the Interrupt Enable register, the AD7756 can be configured to issues an interrupt ($\overline{IRQ}$) when the Active Energy register is half full (positive or negative) or when an over/under flow occurs.

Integration times under steady load

As mentioned in the last section, the discrete time sample period (T) for the accumulation register is 1.1µs (4/CLKIN). With full-scale sinusoidal signals on the analog inputs and the Active Power Gain register set to 000h, the average word value from LPF2 is CCCDh - see figures 28 and 31. The maximum value which can be stored in the Active Energy register before it over flows is 2^{39} or 7F,FFFF,FFFFh. Therefore the integration time under these conditions is calculated as follows:

$$\text{Time} = \frac{7F,FFFF,FFFFh}{CCCDh} \times 1.1\mu s = 11.53 \text{ seconds}$$

POWER OFFSET CALIBRATION

The AD7756 also incorporates an Active Power Offset register (APOS[7:0]). This is a signed 2's complement 8-bit register which can be used to remove offsets in the active power calculation—see Figure 32. An offset may exist in the power calculation due to cross talk between channels on the PCB or in the IC itself. The offset calibration will allow the contents of the Active Power register to be maintained at zero when no power is being consumed.

Four LSBs written to the Active Power Offset register are equivalent to 1 LSB in the Waveform Sample register. Assuming the average value from LPF2 is CCCDh (52,429) with full ac scale inputs on Channel 1 and Channel 2 , then 1 LSB in the Waveform register is equivalent to 1.9% of measurement error at -60dB down on full scale.

That is at -60dB (1,000) down on full scale the average word value from LPF2 is 52.429 (52,429/1,000). One LSB is equivalent to 1/52.429 x 100% = 1.9% of the measured value. The Active Power Offset register has a resolution equal to 1/16 LSB of the Waveform register, hence the power offset correction resolution is 0.12% (1.9%/16) at -60dB.

ENERGY TO FREQUENCY CONVERSION

The AD7756 also provides energy to frequency conversion for calibration purposes. After initial calibration at manufacture, the manufacturer or end customer will often verify the energy meter calibration. One convenient way to verify the meter calibration is for the manufacturer to provide an output frequency which is proportional to the energy or active power under steady load conditions. This output frequency can provide a simple, single wire, optically isolated interface to external calibration equipment. Figure 34 illustrates the Energy-to-Frequency conversion in the AD7756.

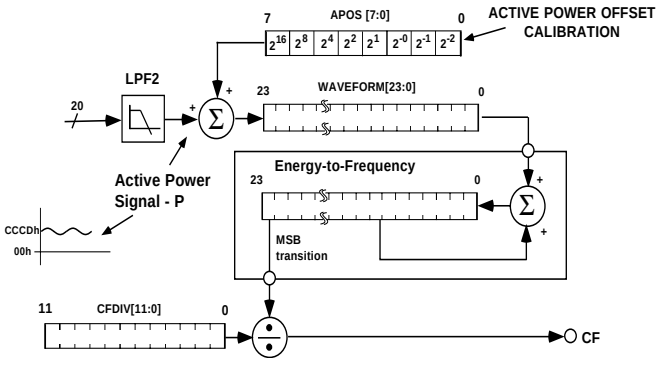


Figure 34– AD7756 Energy to Frequency Conversion

The Energy-to-Frequency conversion is accomplished by accumulating the Active power signal in a 24-bit register. An output pulse is generated when there is a zero to one transition on the MSB (most significant bit) of the register. Under steady load conditions the output frequency is proportional to the Active Power.

The maximum output frequency (CFDIV = 000h & APGAIN = 000h) with full scale ac signals on Channel 1 and Channel 2 is approximately 5.593kHz. This can be calculated as follows:

With the Active Power Gain register set to 000h, the average value of the instantaneous power signal (output of LPF2) is CCCDh or 52,429 decimal. An output frequency is generated on CF when the MSB in the digital to frequency register (24 bits) toggles, i.e., when the register accumulates 2^{23}. This means the register is updated 2^{23}/CCCDh times (or 159.999 times). Since the update rate is 4/CLKIN or 1.1175µs, the time between MSB toggles (CF pulses) is given as

$159.999 \times 1.1175\mu s = 1.78799 \times 10^{-4} s = 5592.86Hz$. Equation 8 gives an expression for the output frequency at CF with the Calibration Frequency Division register = 0.

$$CF\ (Hz) = \frac{\text{Average LPF2 ouput} \times CLKIN}{2^{25}} \qquad (8)$$

This output frequency is easily scaled by the Calibration Frequency Division register (CFDIV[11:0]). This frequency scaling register is a 12-bit register which can scale the output frequency by 1 to 2^{12}. The output frequency is given by the expression below.

$$\text{Frequency} = \frac{\text{Frequency } (CFDIV = 0)}{CFDIV + 1} \qquad (9)$$

For example if the output frequency is 5.59286kHz while the contents of CFDIV are zero (000h), then the output frequency can be set to 5.4618Hz by writing 3FFh Hex (1023 Decimal) to the CFDIV register. The power up default value in CFDVD is 3Fh.

The output frequency will have a have a slight ripple at a frequency equal to twice the line frequency. This is due to imperfect filtering of the instantaneous power signal to generate the Active Power signal – see *ACTIVE POWER CALCULATION*. Equation 3 gives an expression for the instantaneous power signal. This is filtered by LPF2 which has a magnitude response given by Equation 10.

$$|H(f)| = \frac{1}{1 + f / 8.9Hz} \qquad (10)$$

The Active Power signal (output of LPF2) can be rewritten as.

$$p(t) = VI - \left\{\frac{VI}{1 + 2f_l / 8.9Hz}\right\}\cos(4.\pi.f_l.t) \qquad (11)$$

where f_l is the line frequency (e.g., 60Hz)

From Equation 6

$$E(t) = VIt - \left\{\frac{VI}{4.\pi.f_l(1 + 2f_l / 8.9Hz)}\right\}\sin(4.\pi.f_l.t) \qquad (12)$$

From Equation 12 it can be seen that there is a small ripple in the energy calculation due to a sin(2ωt) component. This is shown graphically in Figure 35. The Active Energy calculation is shown by the dashed straight line and is equal to V.I.t. The sinusoidal ripple in the Active Energy calculation is also shown. Since the average value of a sinusoid is zero, this ripple will contribute nothing to the energy calculation over time. However the ripple can be observed in the frequency output, especially at higher output frequencies. The ripple will get larger as a percentage of the frequency at larger loads and higher output frequencies. The reason is simply that at higher output frequencies the integration or averaging time in the Energy-to-Frequency conversion process is shorter. As a consequence some of the sinusoidal ripple is observable in the frequency output. Choosing a lower output frequency at CF for calibration can significantly reduce the ripple. Also averaging the output frequency by using a longer gate time for the counter will achieve the same results.

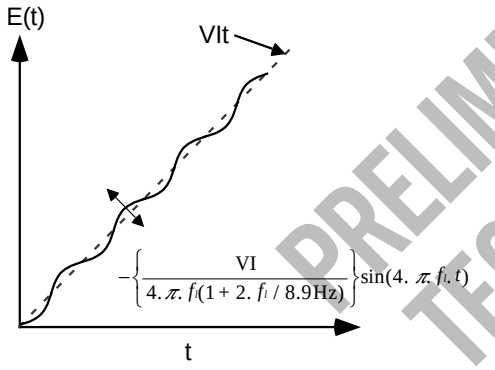


Figure 35 – Output frequency ripple

ENERGY CALIBRATION

By using the on-chip zero-crossing detection on Channel 2 the energy calibration can be greatly simplified and the time required to calibrate the meter can be significantly reduced. To use the zero-cross detection the AD7756 is placed in calibration mode by setting bit 7 (CMODE) in the Mode register. In Calibration Mode the AD7756 accumulates the Active Power signal in the Active Energy register for an integral number of half cycles. This is shown in Figure 36. The number of half line cycles is specified in the Sag Cycle register. The AD7756 can accumulate Active Power for up to 255 half cycles. Because the Active Power is integrated on an integral number of line cycles the sinusoidal component is reduced to zero. This eliminates any ripple in the energy calculation. Energy is calculated more accurately and in a shorter time because integration period can be shortened. At the end of an energy calibration cycle the SAG flag in the Interrupt Status register is set, this will cause the $\overline{SAG}$ output to go active low. If the SAG enable bit in the Interrupt Enable register is enabled, the $\overline{IRQ}$ output will also go active low. Thus the $\overline{IRQ}$ line can be used to signal the end of a calibration also. Another calibration cycle will start as long as the CMODE bit in the Mode register is set. Note that the result of the first calibration is invalid and must be ignored. The result of all subsequent calibration cycles is correct.

From equations 5 and 11.

$$E(t) = \int_0^{nT} VIdt - \left\{\frac{VI}{1+f/8.9Hz}\right\}\int_0^{nT}\cos(2\omega t)dt \quad (13)$$

where n is a integer and T is the line cycle period.

Since the sinusoidal component is integrated over a integer number of line cycles its value is always zero.

Therefore:

$$E(t) = \int_0^{nT} VIdt + 0 \quad (14)$$

$$E(t) = VInT \quad (15)$$

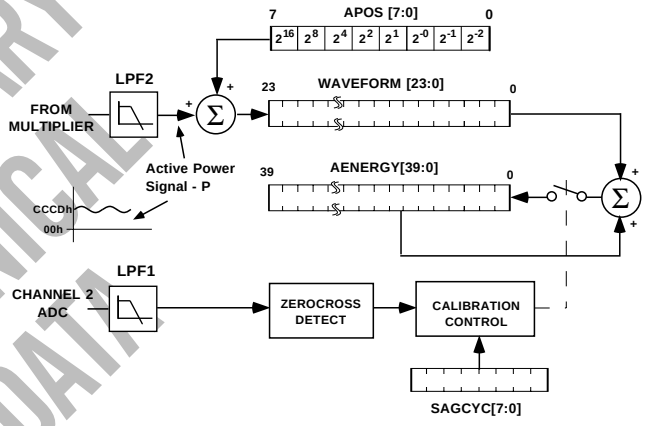


Figure 36 – AD7756 Energy Calibration

CALIBRATING THE ENERGY METER

Calculating the Average Active Power

When calibrating the AD7756, the first step is to calibrate the frequency on CF to some required meter constant, e.g., 3200 imp/kWh.

In order to determine the output frequency on CF, the average value of the Active Power signal (output of LPF2) must first be determined. One convenient way to do this is to use the calibration mode. When the CMODE (bit 7) bit in the Mode register is set to a logic one, energy is accumulated over an integer number of half line cycles as described in the last section.

Since the line frequency is fixed at, say 60Hz and the number of half cycles of integration is specified, the total integration time is given as :

$$\frac{1}{2\times 60\text{Hz}} \times \text{no. of half cycles}$$

For 255 half cycles this would give a total integration time of 2.125 seconds. This would mean the energy register was updated 2.125 / 1.1175µs (4/CLKIN) times. The average output value of LPF2 is given as :

$$\text{Average word (LPF2)} = \frac{\text{AENERGY[39:0]}\times 8\times f_l}{\text{SAGCYC[7:0]}\times \text{CLKIN}} \quad (16)$$

where f_l is the line frequency.

Calibrating the Frequency at CF

Once the average Active Power signal is calculated it can be used to determine the frequency at CF before calibration. When the frequency before calibration is know the Calibration Frequency Divider register (CFDVD) and the Active Power Gain register (APGAIN) can be adjusted so as to produce the required frequency on CF. In this example a meter constant of 3200 imp/kWh is chosen as an appropriate constant. This means that under a steady load of 1kW, the output frequency on CF would be,

$$\text{Frequency (CF)} = \frac{3200\text{ imp/kWh}}{60\text{min}\times 60\text{sec}} = \frac{3200}{3600} = 0.8888\text{Hz}$$

Assuming the meter is set up with a test current (basic current) of 20A and a line voltage of 220V for calibration, the load is calculated as 220V x 20A = 4.4kW. Therefore the expected output frequency on CF under this steady load condition would be 4.4 x 0.8888Hz = 3.9111Hz. Under these load conditions the transducers on Channel 1 and Channel 2 should be selected such that the signal on the voltage channel should see approximately half scale and the signal on the current channel about 1/6 of full scale (assuming a maximum current of 80A). The average value from LPF2 is calculated as 4,335.21 decimal using the calibration mode as described above. Then using Equation 8 (Energy to Frequency Conversion), the frequency under this load is calculated as:

$$\text{CF (Hz)} = \frac{4335.21\times 3.579545\text{MHz}}{2^{25}} = 462.475\text{Hz}$$

However this is the frequency with the contents of the CFDVD and APGAIN registers equal to 000h. The desired frequency out is 3.9111Hz. Therefore the CF frequency must be divided by 462.475/3.9111Hz or 118.2465 decimal. This is achieved by loading the CF Divide register with 117 (or 75h)—NOTE the CF frequency is divided by the contents of CFDVD + 1.

The fine adjustment of the output frequency can be made using the Active Power Gain register. This register has a fine gain adjustment of 0.0244% / LSB. With the CF Divide register contents equal to 75h, the output frequency is given as 462.475Hz / 118 = 3.91928Hz. This setting has an error of +0.21%. This error can be further reduced by witting -(0.21/0.0244) or -9 to APGAIN[11:0] i.e., FF7h.

Calibrating CF is made easy by using the Calibration mode on the AD7756. The only critical part of the set up is that the line frequency be exactly known. If this is not possible if could be measured by using the ZX output of the AD7756.

Eenrgy Meter Display

Besides the pulse output which is used to verify calibration, a solid state energy meter will very often require some form of display. The display should display the amount of energy consumed in kWh (Kilo-Watt Hours). One convenient and simple way to interface the AD7756 to a display or energy register (e.g., MCU with nonvolatile memory) is to use CF. For example the CF frequency could be calibrated to 1,000 imp/kWhr. The MCU would count pulses from CF. Every pulse would be equivalent to 1 watt-hour. If more resolution is required the CF frequency could be set to say 10,000 imp/kWh.

If more flexibility is required when monitoring energy usage the Active Energy register (AENERGY) can be used to calculate energy. A full description of this register can be found in the *Energy Calculation* section. The AENERGY register gives the user both sign and magnitude information regarding energy consumption. On completion of the CF frequency output calibration, i.e., after the Active Power Gain (APGAIN) register has been adjusted a second calibration sequence can be initiated. The purpose of this second calibration routine is to determine a kWh/LSB coefficient for the AENERGY register. Once the coefficient has been calculated the MCU can determine the energy consumption at any time by reading the AENERGY contents and multiplying by the coefficient to calculate kWh.

AD7756 SERIAL INTERFACE

All AD7756 functionality is accessible via several on-chip registers – see Figure 37. The contents of these registers can be updated or read using the on-chip serial interface. After power-on or toggling the $\overline{\text{RESET}}$ pin low or a falling edge on $\overline{\text{CS}}$, the AD7756 is placed in communications mode. In communications mode the AD7756 expects a write to its Communications register. The data written to the communications register determines whether the next data transfer operation will be read or a write and also which register is accessed. Therefore all data transfer operations with the AD7756, whether a read or a write, must begin with a write to the Communications register.

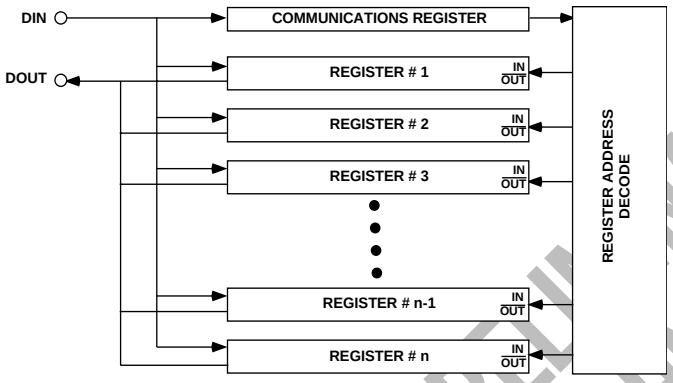


Figure 37 – Addressing AD7756 Registers via the Communications Register

The Communications register is an eight bit wide register. The MSB determines whether the next data transfer operation is a read or a write. The 5 LSBs contain the address of the register to be accessed. See *AD7756 Communications Register* for a more detailed description.

Figure 38 and Figure 39 show the data transfer sequences for a read and write operation respectively.

On completion of a data transfer (read or write) the AD7756 once again enters communications mode.

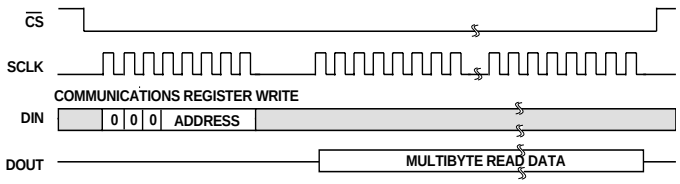


Figure 38 – Reading data from the AD7756 via the serial interface

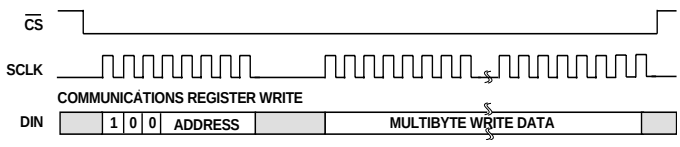


Figure 39. – Writing data to the AD7756 via the serial interface

A data transfer is complete when the LSB of the AD7756 register being addressed (for a write or a read) is transferred to or from the AD7756.

The Serial Interface of the AD7756 is made up of four signals SCLK, DIN, DOUT and $\overline{\text{CS}}$. The serial clock for a data transfer is applied at the SCLK logic input. This logic input has a schmitt-trigger input structure, which allows slow rising (and falling) clock edges to be used. All data transfer operations are synchronized to the serial clock. Data is shifted into the AD7756 at the DIN logic input on the falling edge of SCLK. Data is shifted out of the AD7756 at the DOUT logic output on a rising edge of SCLK. The $\overline{\text{CS}}$ logic input is the chip select input. This input is used when multiple devices share the serial bus. A falling edge on $\overline{\text{CS}}$ also resets the serial interface and places the AD7756 in communications mode. The $\overline{\text{CS}}$ input should be driven low for the entire data transfer operation. Bringing $\overline{\text{CS}}$ high during a data transfer operation will abort the transfer and place the serial bus in a high impedance state. The $\overline{\text{CS}}$ logic input may be tied low if the AD7756 is the only device on the serial bus. However with $\overline{\text{CS}}$ tied low, all initiated data transfer operations must be fully completed, i.e., the LSB of each register must be transferred as there is no other way of bringing the AD7756 back into communications mode without resetting the entire device, i.e., using $\overline{\text{RESET}}$.

AD7756 Serial Write Operation

The serial write sequence takes place as follows. With the AD7756 in communications mode and the $\overline{\text{CS}}$ input logic low, a write to the communications register first takes place. The MSB of this byte transfer is a 1, indicating that the data transfer operation is a write. The LSBs of this byte contain the address of the register to be written to. The AD7756 starts shifting in the register data on the next falling edge of SCLK. All remaining bits of register data are shifted in on the falling edge of subsequent SCLK pulses – see Figure 40.

As explained earlier the data write is initiated by a write to the communications register followed by the data. During a data write operation to the AD7756, data is transferred to all on-chip registers one byte at a time. After a byte is transferred into the serial port, there is a finite time before it is transferred to one of the AD7756 on-chip registers. Although another byte transfer to the serial port can start while the previous byte is being transferred to an on-chip register, this second byte transfer should not finish until at least 5µs after the end of the previous byte transfer. This functionality is expressed in the timing specification t_6 - see Figure 40. If a write operation is aborted during a byte transfer ($\overline{\text{CS}}$ brought high), then that byte will not be written to the destination register.

Destination registers may be up to 3 bytes wide – see *AD7756 Register Descriptions*. Hence the first byte shifted into the serial port at DIN is transferred to the MSB (Most significant Byte) of the destination register. If the addressed register is 12 bits wide for example, a two-byte data transfer must take place. The data is always assumed to be right justified, therefore in this case, the four MSBs of the first byte would be ignored and the 4 LSBs of the first byte written to the AD7756 would be the 4MSBs of the 12-bit word. Figure 41 illustrates this example.

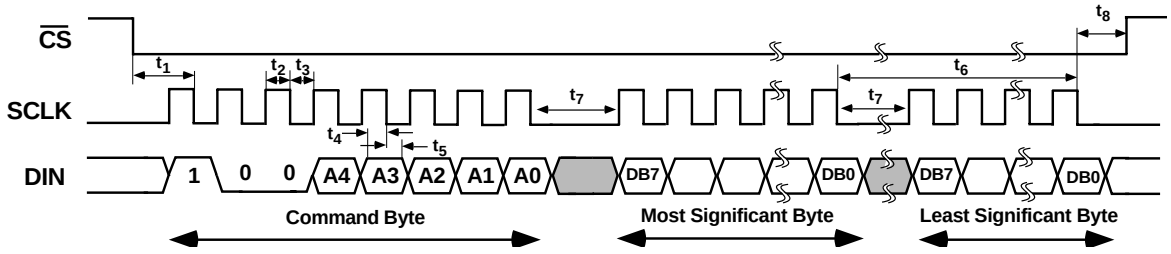


Figure 40 – Serial Interface Write Timing Diagram

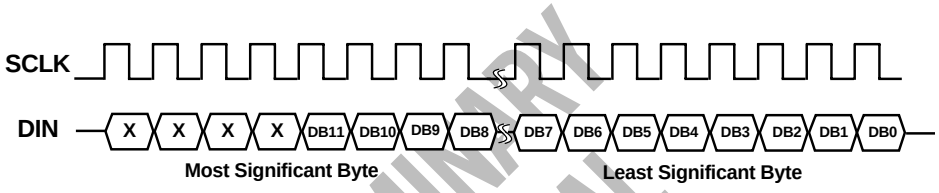


Figure 41 —12 bit Serial Write Operation

AD7756 Serial Read Operation

During a data read operation from the AD7756 data is shifted out at the DOUT logic output on the rising edge of SCLK. As was the case with the data write operation, a data read must be preceded with a write to the Communications register. With the AD7756 in communications mode and $\overline{CS}$ logic low an eight bit write to the Communications register first takes place. The MSB of this byte transfer is a 0, indicating that the next data transfer operation is a read. The LSBs of this byte contain the address of the register which is to be read. The AD7756 starts shifting out of the register data on the next rising edge of SCLK – see Figure 42. At this point the DOUT logic output leaves its high impedance state and starts driving the data bus. All remaining bits of register data are shifted out on subsequent SCLK rising edges. The serial interface also enters communications mode again as soon as the read has been completed. At this point the DOUT logic output enters a high impedance state on the falling edge of the last SCLK pulse. The read operation may be aborted by bringing the $\overline{CS}$ logic input high before the data transfer is complete. The DOUT output enters a high impedance state on the rising edge of $\overline{CS}$.

When an AD7756 register is addressed for a read operation, the entire contents of that register are transferred to the Serial port. This allows the AD7756 to modify its on-chip registers without the risk of corrupting data during a multi byte transfer.

Note when a read operation follows a write operation, the read command (i.e., write to communications register) should not happen for at least 4µs after the end of the write operation. If the read command is sent within 4µs of the write operation, the last byte of the write operation may be lost. The is given as timing specification t_{15}.

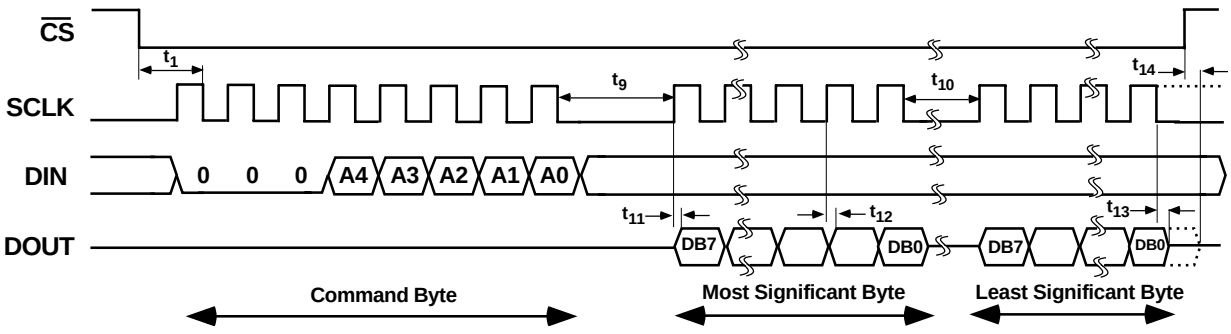


Figure 42 – Serial Interface Read Timing Diagram

Table III. AD7756 REGISTER LIST

A4	A3	A2	A1	A0	Hex	Name	Description
0	0	0	0	0	00H	Not Used	No Operation
0	0	0	0	1	01H	WAVEFORM	The Waveform register is a 24 bit read-only register. This register contains the sampled waveform data form either Channel 1, Channel 2 or the Active Power signal. The data source is selected by data bits 14 and 13 in the Mode Register - see *Channel 1 & 2 Sampling*.
0	0	0	1	0	02H	AENERGY	The Active Energy register. Active Power is accumulated (Integrated) over time in this 40 bit, read-only register. The energy register can hold a minimum of 6 seconds of Active Energy information with full scale analog inputs before it overflows - see *Energy Calculation*.
0	0	0	1	1	03H	RSTENERGY	Same as the Active Energy register except that the register is reset to zero following a read operation
0	0	1	0	0	04H	STATUS	The Interrupt Status register. This is an eight bit read-only register. The Status Register contains information regarding the source of AD7756 interrupts - see *AD7756 Interrupts*.
0	0	1	0	1	05H	RSTSTATUS	Same as the Iterrupt Status register except that the register contents are reset to zero (all flags cleared) after a read operation.
0	0	1	1	0	06H	MODE	The Mode register. This is a 16 bit register through which most of the AD7756 functionality is accessed. Signal sample rates, filter enabling and calibration modes are selected by writing to this register. The contents may be read at any time—see *Mode Register*.
0	0	1	1	1	07H	CFDIV	The Frequency Divider register. This is a twelve bit read/write register. The output frequency on the CF pin is adjusted by writing to this register – see *Energy to Frequency Conversion*
0	1	0	0	0	08H	CH1OS	Channel 1 Offset Adjust. Writing to this 6-bit register allows any offsets on Channel 1 to be removed- see *Analog Inputs*.
0	1	0	0	1	09H	CH2OS	Channel 2 Offset Adjust. Writing to this 6-bit register allows any offsets on Channel 2 to be removed - see *Analog Inputs*.
0	1	0	1	0	0AH	GAIN	PGA Gain Adjust. This 8-bit register is used to adjust the gain selection for the PGA in Channel 1 and Channel 2 - see *Analog Inputs*.
0	1	0	1	1	0BH	APGAIN	Active Power Gain Adjust. This is a 12-bit register. The Active Power calculation can be calibrated by writing to this register. The calibration range is ±50% of the nominal full scale active power. The resolution of the gain adjust is 0.0244% / LSB—see *Channel 1 ADC Gain Adjust*.
0	1	1	0	0	0CH	PHCAL	Phase Calibration Register. The phase relationship between Channel 1 and Channel 2 can be adjusted by writing to this 8-bit register. The adjustment range is approximately ±2.5° at 50Hz in 0.02° steps—see *Phase Compensation*.
0	1	1	0	1	0DH	APOS	Active Power Offset Correction. This 8-bit register allows any offsets in the Active Power Calculation to be removed – see *ActivePower Calculation*.
0	1	1	1	0	0EH	ZXTOUT	Zero-cross Time Out. If no zero crossings are detected on Channel 2 within a time period specified by this register the interrupt request line ($\overline{\text{IRQ}}$) will be activated. The maximum time-out period is 2.3 seconds - see *Zero Crossing Detection* .
0	1	1	1	1	0FH	SAGCYC	Sag line Cycle register. Specifies the number of consecutive half line cycles the signal on Channel 2 must be below SAGLVL before the $\overline{\text{SAG}}$ output is activated - see Voltage Sag Detection. It is also used during calibration mode to set the number of line cycles Active power is accumulated for Energy calibration - see *Energy Calibration*.

A4	A3	A2	A1	A0	Hex	Name	Description
1	0	0	0	0	10H	IRQEN	Interrupt Enable register. AD7756 interrupts may be deactivated at any time by writing the Enable register. A logic zero disenables an interrupt. The Status register will continue to register an interrupt event even if disabled, however the $\overline{IRQ}$ output will not be activated—see *AD7756 Interrupts*.
1	0	0	0	1	11H	SAGLVL	Sag Voltage Level. An eight bit write to this register determines at what peak signal level on Channel 2 the SAG pin will become active. The signal must remain low for the number of cycles specified in the SAGCYC register before the SAG pin is activated—see *Line Voltage Sag Detection*.
1	0	0	1	0	12H	TEMP	Temperature Register. This is an 8-bit register which contains the result of the latest temperature conversion. A full description of this register's contents can be found in the *Temperature Measurement* section of this data sheet.

AD7756 REGISTER DESCRIPTIONS

All AD7756 functionality is accessed via the on-chip registers. Each register is accessed by first writing to the communications register and then transferring the register data. A full description of the serial interface protocol is given in the Serial Interface section of this data sheet.

Communications Register

The Communications register is an eight bit, write-only register which controls the serial data transfer between the AD7756 and the host processor. All data transfer operations must begin with a write to the communications register. The data written to the communications register determines wheather the next operation is a read or a write and which register is being accessed. Table IV below outlines the bit designations for the Communications register.

Table IV. Communications Register

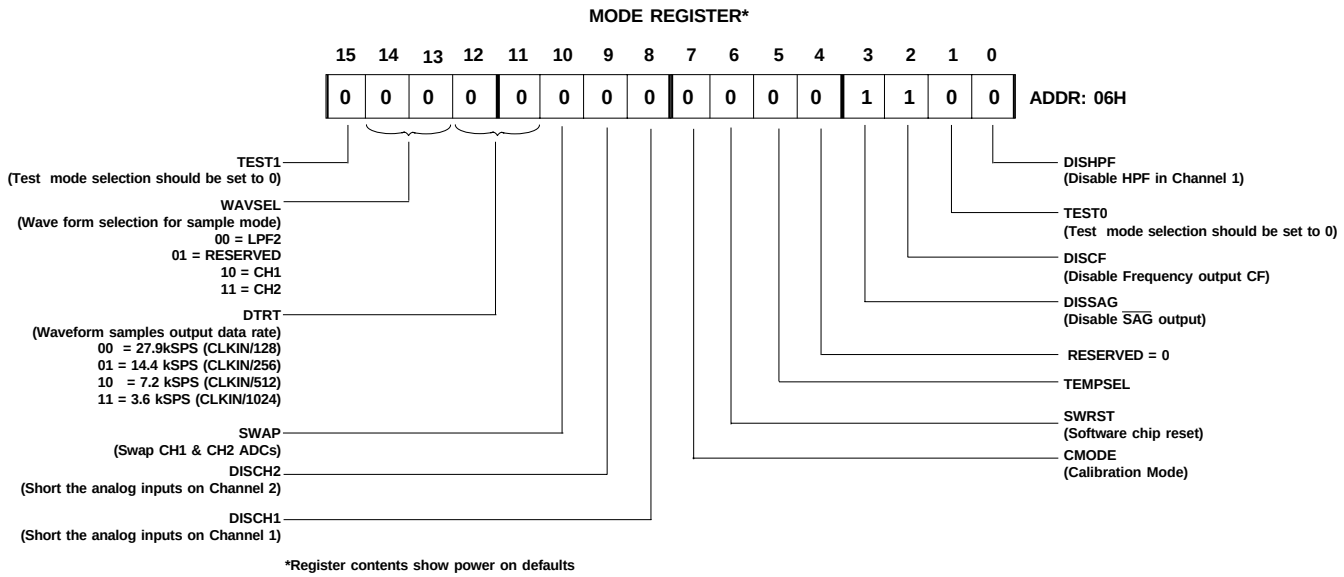
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W/$\overline{R}$	0	0	A4	A3	A2	A1	A0

Bit Location	Bit Mnemonic	Description
0 to 4	A0 to A4	The five LSBs of the Communications register specify the register for the data transfer operation. Table III lists the address of each AD7756 on-chip register.
5 to 6	RESERVED	These bits are unused and should be set to zero.
7	W/$\overline{R}$	When this bit is a logic one the data transfer operation immediately following the write to the Communications register will be interpreted as a write to the AD7756. When this bit is a logic zero the data transfer operation immediately following the write to the Communications register will be interpreted as a read operation.

Mode Register (06H)

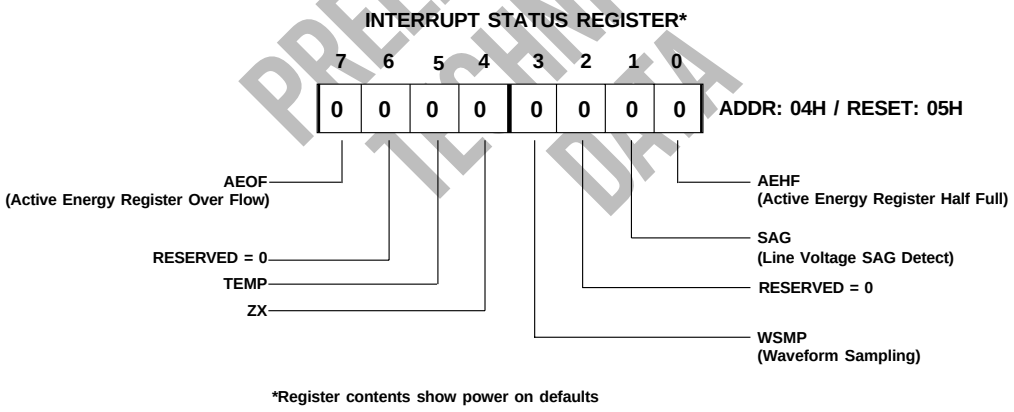
The AD7756 functionality is configured by writing to the MODE register. Table IV below summarizes the functionality of each bit in the MODE register .

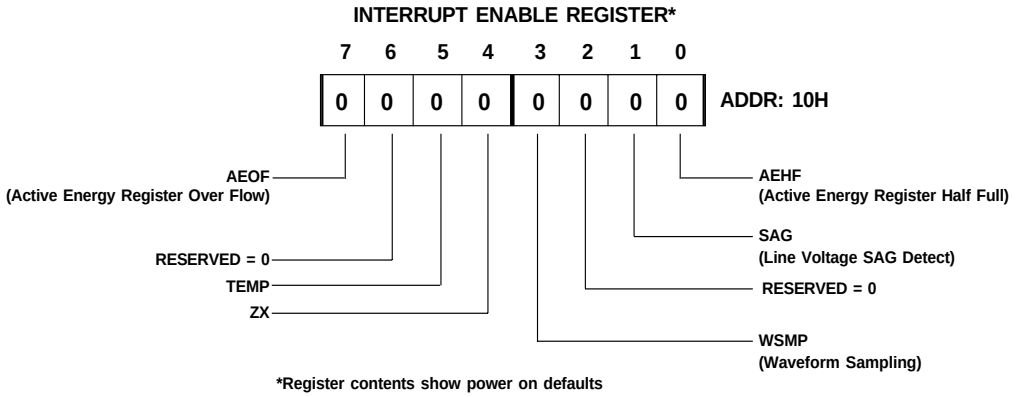
Bit Location	Bit Mnemonic	Description
0	DISHPF	The HFP (High Pass Filter) in Channel 1 is disabled when this bit is set.
1	TEST0	This is intended for factory testing only and should be left at zero.
2	DISCF	The Frequency output CF is disabled when this bit is set
3	DISSAG	The line voltage Sag detection is disabled when this bit is set
4,5	RESERVED	These bits should be left at logic zero
6	SWRST	Software chip reset. A data transfer should not take place to the AD7756 for at least 18µs after a software reset.
7	CMODE	Setting this bit to a logic one places the chip in calibration mode.
8	DISCH1	ADC 1 (Channel 1) inputs are internally shorted together.
9	DISCH2	ADC 2 (Channel 2) inputs are internally shorted together.
10	SWAP	By setting this bit to logic 1 the analog input V2P and V2N are connected to ADC 1 and the analog inputs V1P and V1N are connected to ADC 2.
12, 11	DTRT1,0	These bits are used to select the Waveform Register update rate DTRT 1 DTRT0 Update Rate 0 0 27.9kSPS (CLKIN/128) 0 1 14kSPS (CLKIN/256) 1 0 7kSPS (CLKIN/512) 1 1 3.5kSPS (CLKIN/1024)
14, 13	WAVSEL1,0	These bits are used to select the source of the sampled data for the Waveform Register WAVSEL1 WAVSEL0 Source 0 0 Active Power signal (output of LPF2) 0 1 RESERVED 1 0 Channel 1 1 1 Channel 2
15	TEST1	Writing a logic one to this bit position places the AD7756 in test mode. This is intended for factory testing only and should be left at zero.



Interrupt Status Register (04H) / Reset Interrupt Status Register (05H)
The Status Register is used by the MCU to determine the source of an interrupt request ($\overline{IRQ}$). When an interrupt event occurs in the AD7756, the corresponding flag in the Interrupt Status register is set logic high. If the enable bit for this flag is logic one in the Interrupt Enable register, the $\overline{IRQ}$ logic output goes active low. When the MCU services the interrupt it must first carry out a read from the Interrupt Status Register to determine the source of the interrupt.

Bit Location	Interrupt Flag	Description
0	AEHF	Indicates that an interrupt was caused by the 0 to 1 transition of the MSB of the Active Energy register
1	SAG	Indicates that an interrupt was caused by a SAG on the line voltage or no zero crossing were detected. In calibration mode this flag is also used to indicate the end of an integration over an interger number of half line cycles—see *Energy Calibration*
3	WFSM	Indicates that new data is present in the Waveform Register.
4	ZX	This status bit reflects the status of the ZX logic ouput—*Zero Cossing Detection*
5	TEMP	Indicates that a temperature conversion result is available in the Temperature Register.
7	AEOF	Indicates that the Active Energy register has overflowed

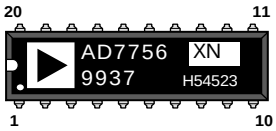




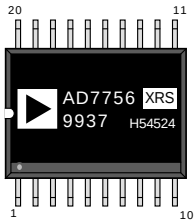
AD7756 SAMPLES (REV 1.1)

Samples of this version of the silicon can be identified from the branding on the top face of the package (PDIP & SSOP). The latest version available is rev. 1.2. Evaluation should be conducted with rev. 1.2. The branding for rev 1.1 is shown below:

PDIP



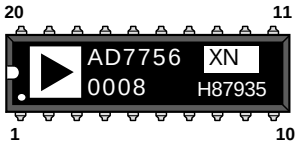
SSOP



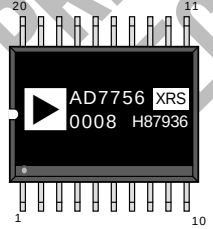
AD7756 ERRATA (REV 1.2)

The following is a list of known issues with the first revision of the AD7756 silicon (rev. 1.2). Samples of this version of the silicon can be identified from the branding on the top face of the package (PDIP & SSOP). The branding is shown below:

PDIP



SSOP



ERRATA

1. Noisy Temperature Measurement

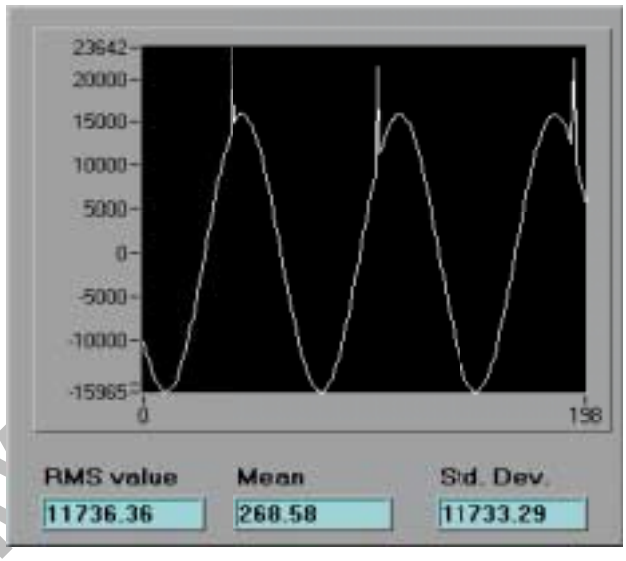
With the APGAIN register set to an non zero value, the temperature measurement could produce noisy results. The measurement becomes more noisy the larger the contents of the APGAIN register.

2. Serial Clock (SCLK) Speed

Using a serial clock frequency which is less than 250kHz (16/CLKIN) will cause unpredicable results when reading from the Active Energy register with a reset. There is also the possibility of missing an interrupt event when readin the Interrupt Status register with a reset.

3. Waveform Sampling Channel 1

Samples collected from channel 1 during a waveform sampling sequence are very noisy when the contents of the Active Power Gain register (APGAIN) is non zero. An example of a noisy reading is shown below. This noise in the waveform samples does not effect the accuracy of the energy measuremnt.



4. Offset Error at Light Load

At high gain (Gain=16), there is a small offset in the active energy calculation, and it can lead to large error at light load. The Active Power Offset register (APOS) can be used to reduce the error on application with current dynamic range closed to 500 to 1. An additional calibration point at light load is needed to determine the optimal values for this register. The graph below shows the accuracy of AD7756 with offset adjustment using the APOS register.