ANALOG DEVICES

High Performance 4/8 Channel Fault-Protected Analog Multiplexers

ADG438F/ADG439F*

FEATURES
Fast Switching Times
t_{ON} 250 ns max
t_{OFF} 150 ns max
Fault and Overvoltage Protection (–40 V, +55 V)
All Switches OFF with Power Supply OFF
Analog Output of ON Channel Clamped Within Power Supplies If an Overvoltage Occurs
Latch-Up Proof Construction
Break Before Make Construction
TTL and CMOS Compatible Inputs

APPLICATIONS
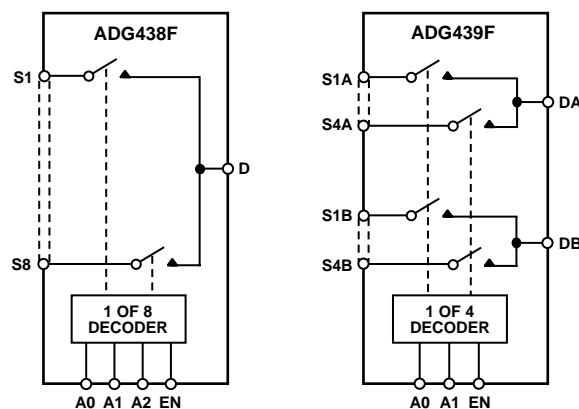**Data Acquisition Systems**
Industrial and Process Control Systems
Avionics Test Equipment
Signal Routing Between Systems
High Reliability Control Systems

FUNCTIONAL BLOCK DIAGRAMS

GENERAL DESCRIPTION
The ADG438F/ADG439F are CMOS analog multiplexers, the ADG438F comprising 8 single channels and the ADG439F comprising four differential channels. These multiplexers provide fault protection. Using a series n-channel, p-channel, n-channel MOSFET structure, both device and signal source protection is provided in the event of an overvoltage or power loss. The multiplexer can withstand continuous overvoltage inputs from –40 V to +55 V. During fault conditions, the multiplexer input (or output) appears as an open circuit and only a few nanoamperes of leakage current will flow. This protects not only the multiplexer and the circuitry driven by the multiplexer, but also protects the sensors or signal sources which drive the multiplexer.

The ADG438F switches one of eight inputs to a common output as determined by the 3-bit binary address lines A0, A1 and A2. The ADG439F switches one of four differential inputs to a common differential output as determined by the 2-bit binary address lines A0 and A1. An EN input on each device is used to enable or disable the device. When disabled, all channels are switched OFF.

PRODUCT HIGHLIGHTS
1. Fault Protection.
   The ADG438F/ADG439F can withstand continuous voltage inputs up to –40 V or +55 V. When a fault occurs due to the power supplies being turned off, all the channels are turned off and only a leakage current of a few nano-amperes flows.

2. ON channel turns OFF while fault exists.

3. Low R_{ON}.

4. Fast Switching Times.

5. Break-Before-Make Switching.
   Switches are guaranteed break-before-make so that input signals are protected against momentary shorting.

6. Trench Isolation Eliminates Latch-up.
   A dielectric trench separates the p- and n-channel MOSFETs thereby preventing latch-up.

7. Improved OFF Isolation.
   Trench isolation enhances the channel-to-channel isolation of the ADG438F/ADG439F.

*Patent Pending.

REV. D

Dual Supply (V_{DD} = +15 V, V_{SS} = –15 V, GND = 0 V, unless otherwise noted)

Parameter	+25°C	B Version −40°C to +85°C	−40°C to +105°C	Units	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range		V_{SS} + 1.2	V_{SS} + 1.2	V min	
		V_{DD} – 0.8	V_{DD} – 0.8	V max	
R_{ON}		400	400	Ω max	−10 V ≤ V_S ≤ +10 V, I_S = 1 mA;
ΔR_{ON}		5	5	% max	−5 V ≤ V_S ≤ +5 V, I_S = 1 mA;
R_{ON} Drift	0.6			%/°C typ	V_S = 0 V, I_S = 1 mA
R_{ON} Match	3	3	3	% max	V_S = ±10 V, I_S = 1 mA
LEAKAGE CURRENTS					
Source OFF Leakage I_S (OFF)	±0.01			nA typ	V_D = ±10 V, V_S = ∓10 V;
	±0.5	±2	±5	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.01			nA typ	V_D = ±10 V, V_S = ∓10 V;
ADG438F	±0.5	±5	±30	nA max	Test Circuit 3
ADG439F	±0.5	±5	±15	nA max	
Channel ON Leakage I_D, I_S (ON)	±0.01			nA typ	V_S = V_D = ±10 V;
ADG438F	±0.5	±5	±30	nA max	Test Circuit 4
ADG439F	±0.5	±5	±15	nA max	
FAULT					
Output Leakage Current	±0.02			nA typ	V_S = –33 V, +33 V or +50 V, V_D = 0 V, Test Circuit 3
(With Overvoltage)	±0.1	±2	±10	µA max	
Input Leakage Current	±0.005			µA typ	V_S = ±25 V, V_D = ∓10 V, Test Circuit 5
(With Overvoltage)	±0.1	±1	±2	µA max	
Input Leakage Current	±0.001			µA typ	V_S = ±25 V, V_D = V_{EN} = A0, A1, A2 = 0 V
(With Power Supplies OFF)	±0.1	±1	±4	µA max	Test Circuit 6
DIGITAL INPUTS					
Input High Voltage, V_{INH}		2.4	2.4	V min	
Input Low Voltage, V_{INL}		0.8	0.8	V max	
Input Current					
I_{INL} or I_{INH}		±1	±1	µA max	V_{IN} = 0 or V_{DD}
C_{IN}, Digital Input Capacitance	5			pF typ	
DYNAMIC CHARACTERISTICS[2]					
$t_{TRANSITION}$	170			ns typ	R_L = 1 MΩ, C_L = 35 pF;
	220	300	320	ns max	V_{S1} = ±10 V, V_{S8} = ∓10 V; Test Circuit 7
t_{OPEN}	10	10	10	ns min	R_L = 1 kΩ, C_L = 35 pF;
					V_S = +5 V; Test Circuit 8
t_{ON} (EN)	200			ns typ	R_L = 1 kΩ, C_L = 35 pF;
	250	300	300	ns max	V_S = +5 V; Test Circuit 9
t_{OFF} (EN)	110			ns typ	R_L = 1 kΩ, C_L = 35 pF;
	150	180	180	ns max	V_S = +5 V; Test Circuit 9
t_{SETT}, Settling Time					R_L = 1 kΩ, C_L = 35 pF;
0.1%		0.5	0.5	µs typ	V_S = +5 V
0.01%		1.7	1.7	µs typ	
Charge Injection	4			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; Test Circuit 10
OFF Isolation	80			dB typ	R_L = 1 kΩ, C_L = 15 pF, f = 100 kHz;
					V_S = 7 V rms; Test Circuit 11
Channel-to-Channel Crosstalk	85			dB typ	R_L = 1 kΩ, C_L = 15 pF, f = 100 kHz;
					V_S = 7 V rms; Test Circuit 12
C_S (OFF)	5			pF typ	
C_D (OFF)					
ADG438F	50			pF typ	
ADG439F	25			pF typ	
POWER REQUIREMENTS					
I_{DD}	0.05			mA typ	V_{IN} = 0 V or 5 V
	0.15	0.25	0.25	mA max	
I_{SS}	0.01			mA typ	
	0.02	0.04	0.04	mA max	

NOTES
[1]Temperature range is as follows: B Version: –40°C to +105°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to V_{SS} .... +44 V
V_{DD} to GND .... –0.3 V to +25 V
V_{SS} to GND .... +0.3 V to –25 V
V_{EN}, V_A Digital Input .... – 0.3 V to V_{DD} + 2 V or 20 mA,
Whichever Occurs First
V_S, Analog Input Overvoltage with Power ON ..... V_{SS} – 25 V
to V_{DD} + 40 V
V_S, Analog Input Overvoltage with Power OFF
.... –40 V to +55 V
Continuous Current, S or D .... 20 mA
Peak Current, S or D
(Pulsed at 1 ms, 10% Duty Cycle max) .... 40 mA
Operating Temperature Range
Industrial (B Version) .... –40°C to +105°C
Storage Temperature Range .... –65°C to +150°C
Junction Temperature .... +150°C
Plastic Package
θ_{JA}, Thermal Impedance .... 117°C/W
Lead Temperature, Soldering (10 sec) .... +260°C
SOIC Package
θ_{JA}, Thermal Impedance
Narrow Body .... 125°C/W
Wide Body .... 90°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) .... +215°C
Infrared (15 sec) .... +220°C

*Stresses above those listed under Absolute Maximum Ratings may cause perma-nent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADG438FBN	–40°C to +105°C	N-16
ADG438FBR	–40°C to +105°C	R-16N
ADG439FBN	–40°C to +105°C	N-16
ADG439FBR	–40°C to +105°C	R-16N
ADG439FBRW	–40°C to +105°C	R-16W

*N = Plastic DIP; R-16N = 0.15" Small Outline IC (SOIC); R-16W = 0.3"
Small Outline IC (SOIC).

Table I. ADG438F Truth Table

A2	A1	A0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

X = Don't Care

Table II. ADG439F Truth Table

A1	A0	EN	ON SWITCH PAIR
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

X = Don't Care

ADG438F/ADG439F PIN CONFIGURATIONS

DIP/SOIC

DIP/SOIC
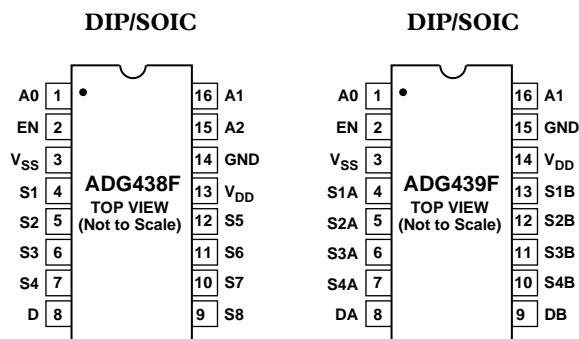
ADG438F/ADG439F

TERMINOLOGY

V_{DD}	Most positive power supply potential.
V_{SS}	Most negative power supply potential.
GND	Ground (0 V) reference.
R_{ON}	Ohmic resistance between D and S.
ΔR_{ON}	R_{ON} variation due to a change in the analog input voltage with a constant load current.
R_{ON} Drift	Change in R_{ON} when temperature changes by one degree Celsius.
R_{ON} Match	Difference between the R_{ON} of any two channels.
I_S (OFF)	Source leakage current when the switch is off.
I_D (OFF)	Drain leakage current when the switch is off.
I_D, I_S (ON)	Channel leakage current when the switch is on.
V_D (V_S)	Analog voltage on terminals D, S.
C_S (OFF)	Channel input capacitance for "OFF" condition.
C_D (OFF)	Channel output capacitance for "OFF" condition.
C_D, C_S (ON)	"ON" switch capacitance.
C_{IN}	Digital input capacitance.
t_{ON} (EN)	Delay time between the 50% and 90% points of the digital input and switch "ON" condition.
t_{OFF} (EN)	Delay time between the 50% and 90% points of the digital input and switch "OFF" condition.
$t_{TRANSITION}$	Delay time between the 50% and 90% points of the digital inputs and the switch "ON" condition when switching from one address state to another.
t_{OPEN}	"OFF" time measured between 80% points of both switches when switching from one address state to another.
V_{INL}	Maximum input voltage for Logic "0".
V_{INH}	Minimum input voltage for Logic "1".
I_{INL} (I_{INH})	Input current of the digital input.
Off Isolation	A measure of unwanted signal coupling through an "OFF" channel.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
I_{DD}	Positive supply current.
I_{SS}	Negative supply current.

Typical Performance Graphs
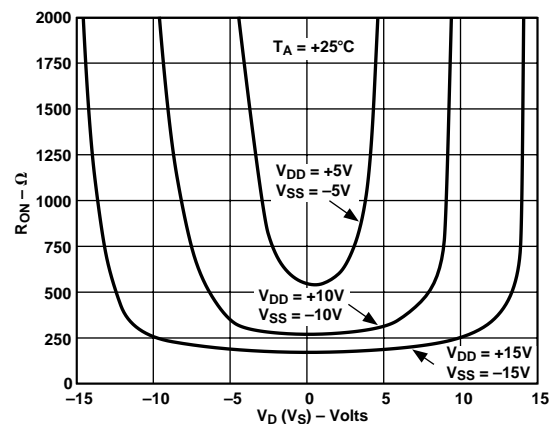
Figure 1. On Resistance as a Function of V_D (V_S)
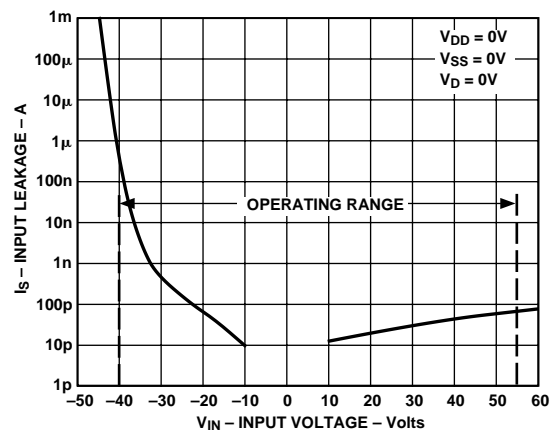
Figure 2. Input Leakage Current as a Function of V_S (Power Supplies OFF) During Overvoltage Conditions
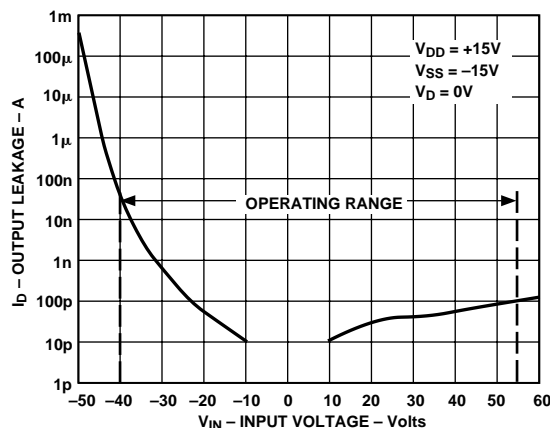
Figure 3. Output Leakage Current as a Function of V_S (Power Supplies ON) During Overvoltage Conditions
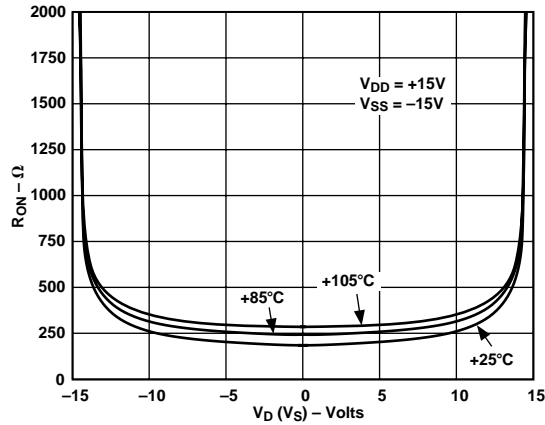
Figure 4. On Resistance as a Function of V_D (V_S) for Different Temperatures
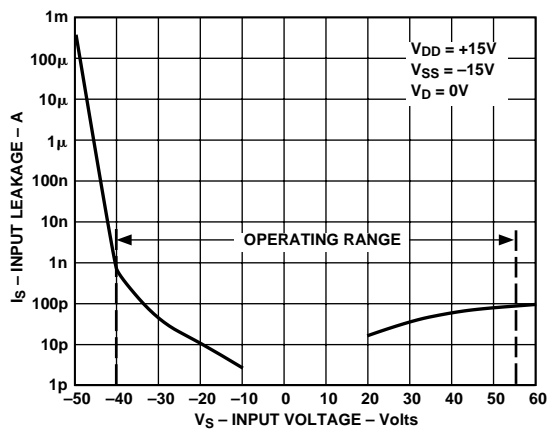

Figure 5. Input Leakage Current as a Function of V_S (Power Supplies ON) During Overvoltage Conditions

Figure 6. Leakage Currents as a Function of V_D (V_S)
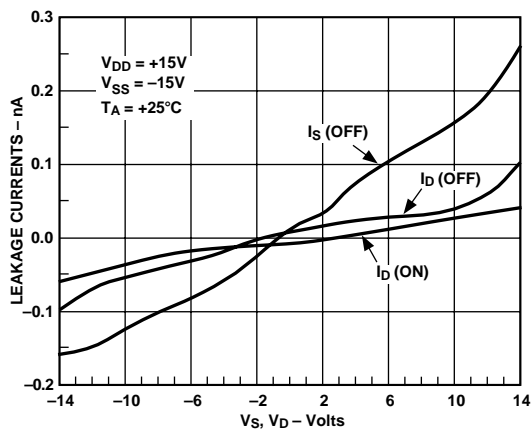

Figure 7. Leakage Currents as a Function of Temperature

Figure 8. Switching Time vs. Power Supply
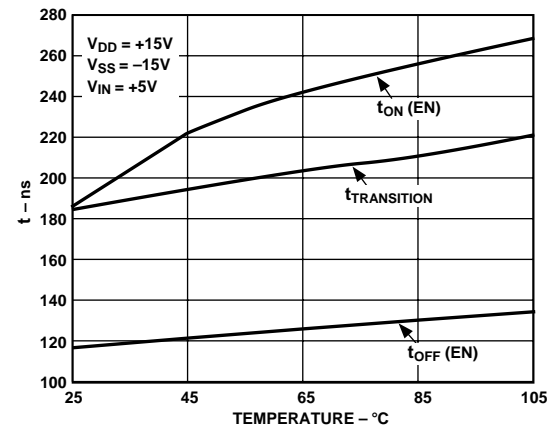
Figure 9. Switching Time vs. Temperature

ADG438F/ADG439F

THEORY OF OPERATION

The ADG438F/ADG439F multiplexers are capable of withstanding overvoltages from –40 V to +55 V, irrespective of whether the power supplies are present or not. Each channel of the multiplexer consists of an n-channel MOSFET, a p-channel MOSFET and an n-channel MOSFET, connected in series. When the analog input exceeds the power supplies, one of the MOSFETs will switch off, limiting the current to sub-microamp levels, thereby preventing the overvoltage from damaging any circuitry following the multiplexer. Figure 12 illustrates the channel architecture that enables these multiplexers to withstand continuous overvoltages.

When an analog input of V_{SS} + 1.2 V to V_{DD} – 0.8 V is applied to the ADG438F/ADG439F, the multiplexer behaves as a standard multiplexer, with specifications similar to a standard multiplexer, for example, the on-resistance is 180 Ω typically. However, when an overvoltage is applied to the device, one of the three MOSFETs will turn off.

Figures 10 to 13 show the conditions of the three MOSFETs for the various overvoltage situations. When the analog input applied to an ON channel approaches the positive power supply line, the n-channel MOSFET turns OFF since the voltage on the analog input exceeds the difference between V_{DD} and the

n-channel threshold voltage (V_{TN}). When a voltage more negative than V_{SS} is applied to the multiplexer, the p-channel MOSFET will turn off since the analog input is more negative than the difference between V_{SS} and the p-channel threshold voltage (V_{TP}).

When the power supplies are present but the channel is off, again either the p-channel MOSFET or one of the n-channel MOSFETs will remain off when an overvoltage occurs.

Finally, when the power supplies are off, the gate of each MOSFET will be at ground. A negative overvoltage switches on the first n-channel MOSFET but the bias produced by the overvoltage causes the p-channel MOSFET to remain turned off. With a positive overvoltage, the first MOSFET in the series will remain off since the gate to source voltage applied to this MOSFET is negative.

During fault conditions, the leakage current into and out of the ADG438F/ADG439F is limited to a few microamps. This protects the multiplexer and succeeding circuitry from over stresses as well as protecting the signal sources which drive the multiplexer. Also, the other channels of the multiplexer will be undisturbed by the overvoltage and will continue to operate normally.
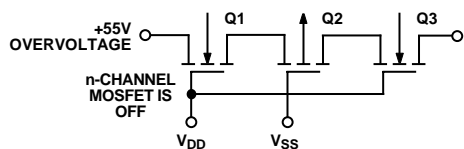

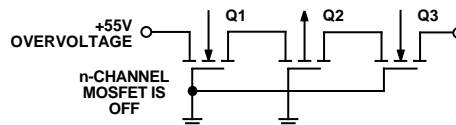Figure 10. +55 V Overvoltage Input to the ON Channel

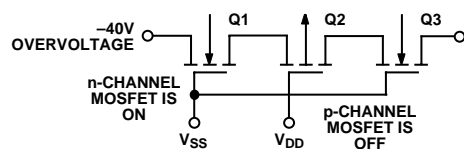Figure 12. +55 V Overvoltage with Power OFF

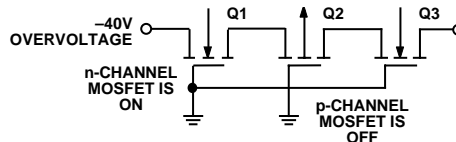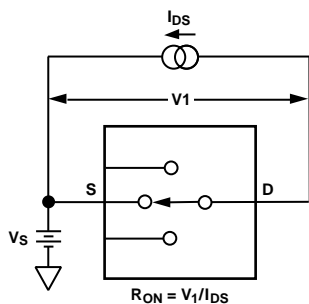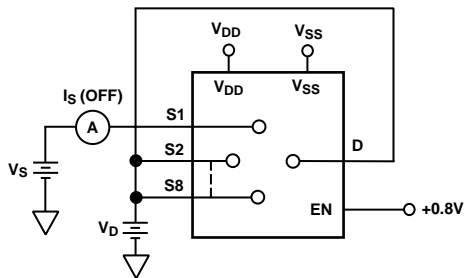Figure 11. –40 V Overvoltage on an OFF Channel with Multiplexer Power ON
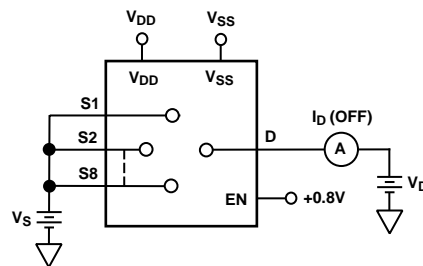

Figure 13. –40 V Overvoltage with Power OFF
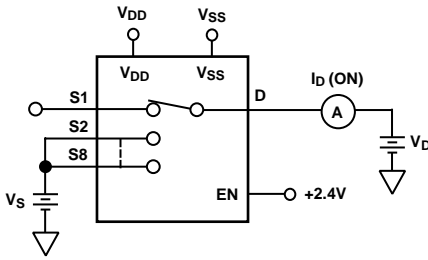
Test Circuits

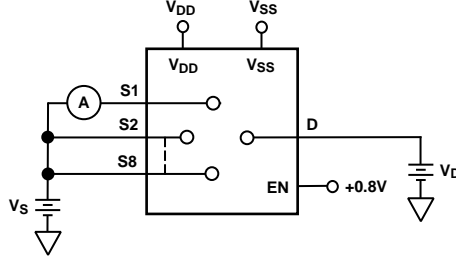Test Circuit 1. On Resistance
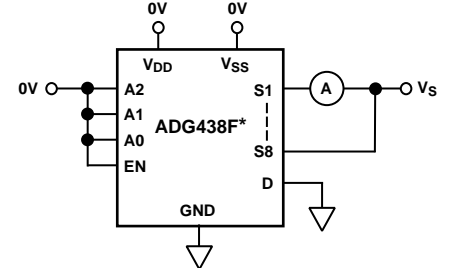

Test Circuit 2. I_S (OFF)
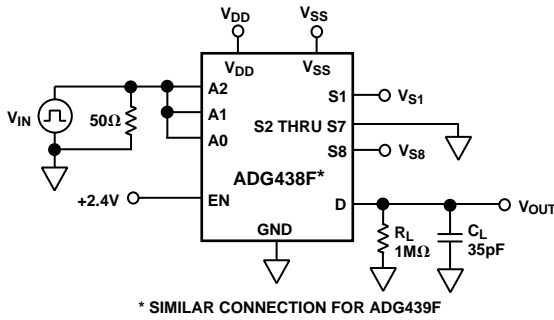

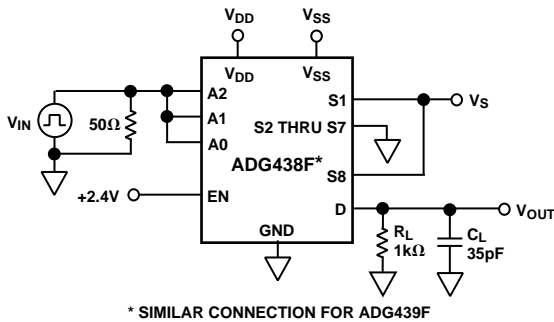Test Circuit 3. I_D (OFF)
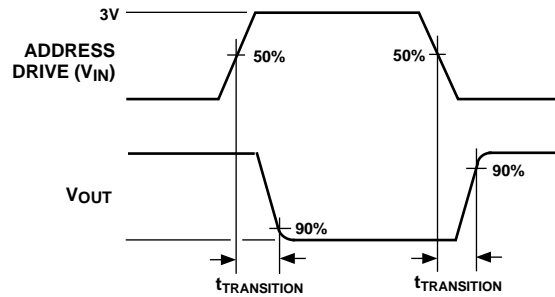
Test Circuit 4. I_D (ON)

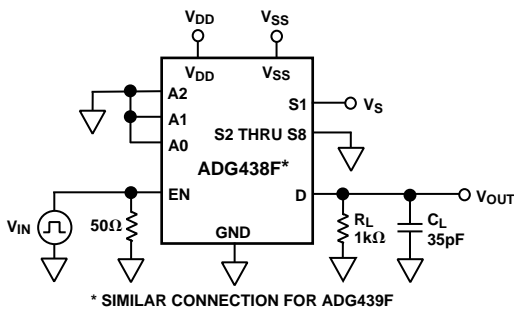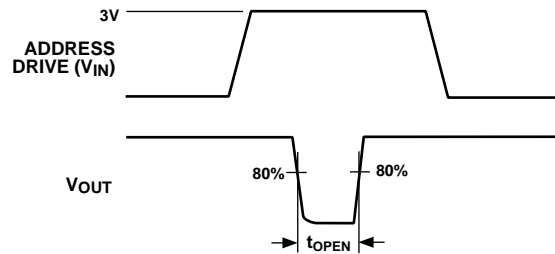Test Circuit 5. Input Leakage Current (with Overvoltage)

* SIMILAR CONNECTION FOR ADG439F

Test Circuit 6. Input Leakage Current (with Power Supplies OFF)

* SIMILAR CONNECTION FOR ADG439F

Test Circuit 7. Switching Time of Multiplexer, $t_{TRANSITION}$

* SIMILAR CONNECTION FOR ADG439F

Test Circuit 8. Break-Before-Make Delay, t_{OPEN}

* SIMILAR CONNECTION FOR ADG439F

Test Circuit 9. Enable Delay, t_{ON} (EN), t_{OFF} (EN)
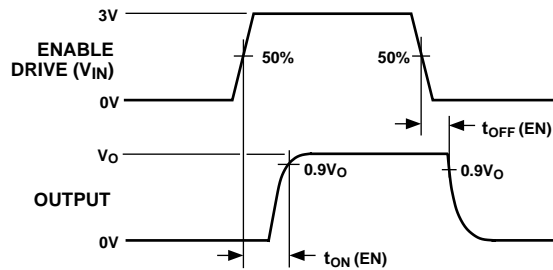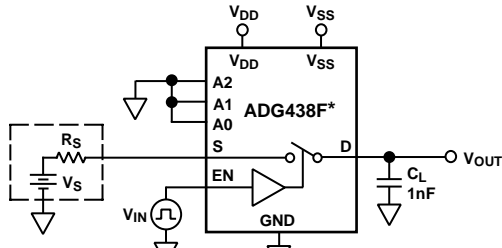
ADG438F/ADG439F

Test Circuit 10. Charge Injection

Test Circuit 11. OFF Isolation
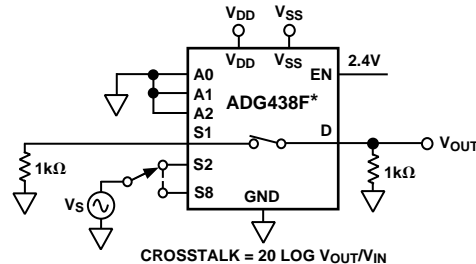
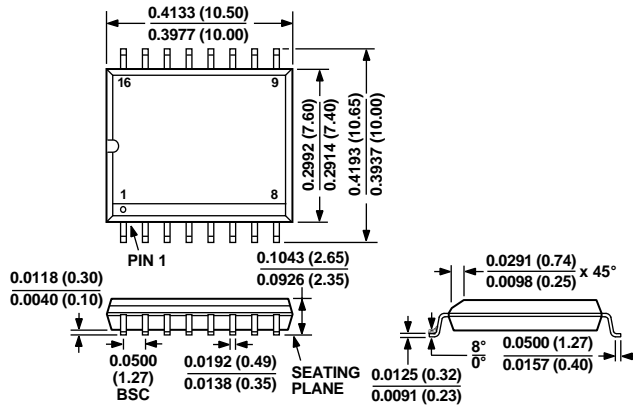Test Circuit 12. Channel-to-Channel Crosstalk

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OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).

16-Lead Plastic (N-16)
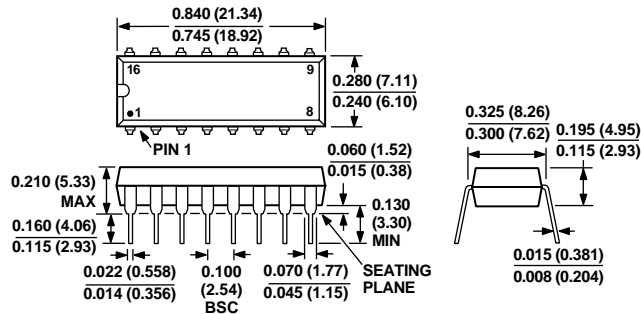
16-Lead SOIC (R-16W)
(Wide Body)

16-Lead SOIC (R-16N)
(Narrow Body)

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